HELMHOLTZ
GEMEINSCHAFT

SEI Studiengruppe für
Elektronische Instrumentierung
der Helmholtz-Zentren

107. Tagung der Studiengruppe elektronische Instrumentierung im Frühjahr 2016

in Darmstadt vom 4. April - 6. April 2016

an der

GSI
Helmholtzzentrum für Schwerionenforschung

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107. Tagung der Studiengruppe elektronische Instrumentierung im Frühjahr 2016

SEI - Studiengruppe elektronische Instrumentierung
der Helmholtz-Zentren
GSI (Darmstadt), 4. April - 6. April 2016

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Allgemeines und Zusammenfassendes

Vorträge

Workshop

Peter Göttlicher
DESY-FEB
23. Juli 2016

Eröffnung

Eine jährliche Tagung der Studiengruppe ¨Elektronische Instrumentierung der Helmholtz-Zentren¨ , SEI, bieten für die Mitarbeiter und Mitarbeiterinnen ein Forum zum Austausch über die Entwicklung der Elektronik und der angeschlossenene Datenverarbeitung. Die Tagung richtet sich an Techniker/innen, Ingenieure/innen und Wissenschaftler/innen, die sich mit Elektronik und deren Programmierung im Forschungsumfeld beschäftigen. Sie steht auch nicht an den Helmholtz-Zentren Tätigen offen zu aktiver und passiver Teilnahme. Dieses Jahr nahmen 74 Personen teil. Neben den Helmholtz-Zentren DESY, FZJ, GSI, HZB, HZG, HZDR und KIT waren weitere Forschungs-Zentren, Universitäten und spezialisierte Industriebetriebe vertreten.

Die Vortragsanmeldungen umfassten ein breites Spektren des Arbeitsfeldes moderner Elektronik. Es beteiligten sich alle Forschungszentren und einige Universitten, so dass ein breiter Austausch erreicht wurde. Bei der Programmgestaltung kristallisierte sich eine Gliederung heraus:

– Schnelle Datenaufnahme, -verarbeitung und -transmission

– Geräte und Computer

– Software und Slow-Control

– Bau von Instrumenten, Detektoren und Systemen

– Synergien in der Zusammenarbeit mit spezialisierten Industriepartnern

Mit Führungen auf dem Forschungsgelände der gastgebenden GSI wurde uns die instrumentelle Experimenteausrüstung und die Höchstleistungsrechentechnik mit deren Anforderungen an energiesparende Infrastruktur nähergebracht. .

Das Tagungsprogramm ist auf dem Internet einzusehen:
https://indico.desy.de/conferenceDisplay.py?confId=10959 oder
https://indico.desy.de//event/SEI_2016
Die Homepage der Studiengruppe ist auf http://sei.desy.de/ zu finden.

Im Anschluss an die Tagung haben sich viele Teilnehmer noch zu einem halbtägigen Workshop zusammengesetzt, um sich über den den Einsatz von Kontrollsystemen auszutauschen, Synergien und Spezialisierung der verschiedenen Zentren oder Forschungsfelder kennenzulernen.

Ausblick

Die nächste Tagung wird für das Frühjahr 2017 am KIT in Karlsruhe geplant.

SEI-Tagung, Frühjahr 2016, GSI Darmstadt

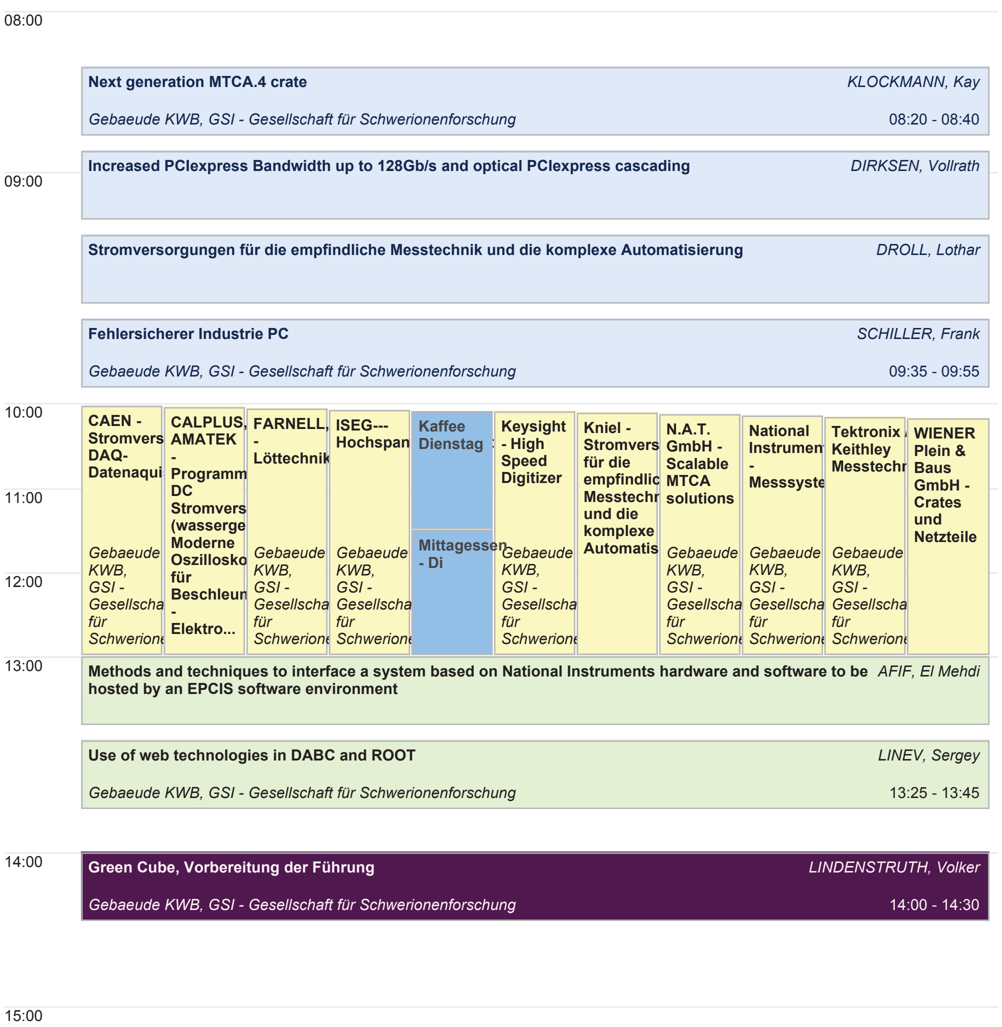
Teilnehmer an der SEI-Tagung 2016 an der GSI , Darmstadt.

Tagungsprogramm

Mon 04/04

13:00	**Eroeffnung**	*GOETTLICHER, peter*	*Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung*	13:00 - 13:10
	Instrumentation and the NUSTAR physics Program in FAIR phase-0	*HAIK, Simon*	*Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung*	13:10 - 13:55
14:00	**Aktuelle Projekte der Gruppe EE-Digitalelektronik**	*HEGGEN, Henning*	*Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung*	13:55 - 14:15
	Ethernet-basierte Datenaufnahme jenseits 10 GBit/s	*LANGE, Bert*	*Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung*	14:20 - 14:40
15:00	**The Big Data Problem in DAQ Systems**	*KOPMANN, Andreas*	*Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung*	14:45 - 15:05
	Entwicklungsstrategien bei der Einführung neuer komplexer Technologien im Bereich High-Speed Datenübertragung	*KRIVAN, Frantisek*		
	Kaffee_Mo		*Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung*	15:35 - 16:00
16:00	**Towards a generic front-end readout architecture in scientific detector systems**	*DEGENHARDT, Carsten*		
	An Ultra-fast Linear Array Detector for MHz Line Repetition Rate Spectroscopy	*ROTA, Lorenzo*	*Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung*	16:25 - 16:45
17:00	**MicroTCA.4 based RF and Laser Cavity Requlation Including Piezo Controls**	*PRZYGODA, konrad*	*Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung*	16:50 - 17:15
	FPGA implementation for data acquisition system with gigabit serial link and PCIe interface	*MINAMI, Shizu*		
18:00				

Tue 05/04



08:00

Next generation MTCA.4 crate *KLOCKMANN, Kay*
Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung 08:20 - 08:40

09:00

Increased PCIexpress Bandwidth up to 128Gb/s and optical PCIexpress cascading *DIRKSEN, Vollrath*

Stromversorgungen für die empfindliche Messtechnik und die komplexe Automatisierung *DROLL, Lothar*

Fehlersicherer Industrie PC *SCHILLER, Frank*
Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung 09:35 - 09:55

10:00

11:00

12:00

CAEN - Stromvers DAQ- Datenaqui *Gebaeude KWB, GSI - Gesellscha für Schwerione*

CALPLUS, AMATEK - Programm DC Stromvers (wasserge Moderne Oszillosko für Beschleun - Elektro...

FARNELL, - Löttechnik *Gebaeude KWB, GSI - Gesellscha für Schwerione*

ISEG--- Hochspan *Gebaeude KWB, GSI - Gesellscha für Schwerione*

Kaffee Dienstag

Mittagessen - Di

Keysight - High Speed Digitizer *Gebaeude KWB, GSI - Gesellscha für Schwerione*

Kniel - Stromvers für die empfindlic Messtechr und die komplexe Automatis

N.A.T. GmbH - Scalable MTCA solutions *Gebaeude KWB, GSI - Gesellscha für Schwerione*

National Instrumen - Messsyste *Gebaeude KWB, GSI - Gesellscha für Schwerione*

Tektronix Keithley Messtechr *Gebaeude KWB, GSI - Gesellscha für Schwerione*

WIENER Plein & Baus GmbH - Crates und Netzteile

13:00

Methods and techniques to interface a system based on National Instruments hardware and software to be hosted by an EPCIS software environment *AFIF, El Mehdi*

Use of web technologies in DABC and ROOT *LINEV, Sergey*
Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung 13:25 - 13:45

14:00

Green Cube, Vorbereitung der Führung *LINDENSTRUTH, Volker*
Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung 14:00 - 14:30

15:00

Wed 06/04

08:00

EPICS @ GSI & FAIR - ein Überblick *ZUMBRUCH, Peter*
Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung 08:30 - 08:50

09:00 **CS++ - The Actor based Successor of the CS Framework** *BRAND, Holger*
Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung 08:55 - 09:15

Synchronised fast shutter control with adaptive phase shift compensation in an EtherCAT motion control system *GAHL, Thomas*

10:00 **Präzise Spannungsversorgung für die SiMPs eines Tscherenkow-Teleskops an der Antarktis** *ZANTIS, Franz Peter*

Kaffee Mi-I
Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung 10:10 - 10:40

Entwicklung einer Multikanal-Auswertehardware für Delayline-Neutronendetektoren *JACOBSEN, Christian*

11:00 **Silicon Photonic Data Transmission for Detector Instrumentation** *KARNICK, Djorn*
Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung 11:05 - 11:25

EMV Betrachtung des Instruments Maria am FRM2 *VEHRES, Guido*
Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung 11:30 - 11:50

12:00 **Quench Detektoren für FAIR** *AYET SAN ANDRES, Samuel*
Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung 11:55 - 12:15

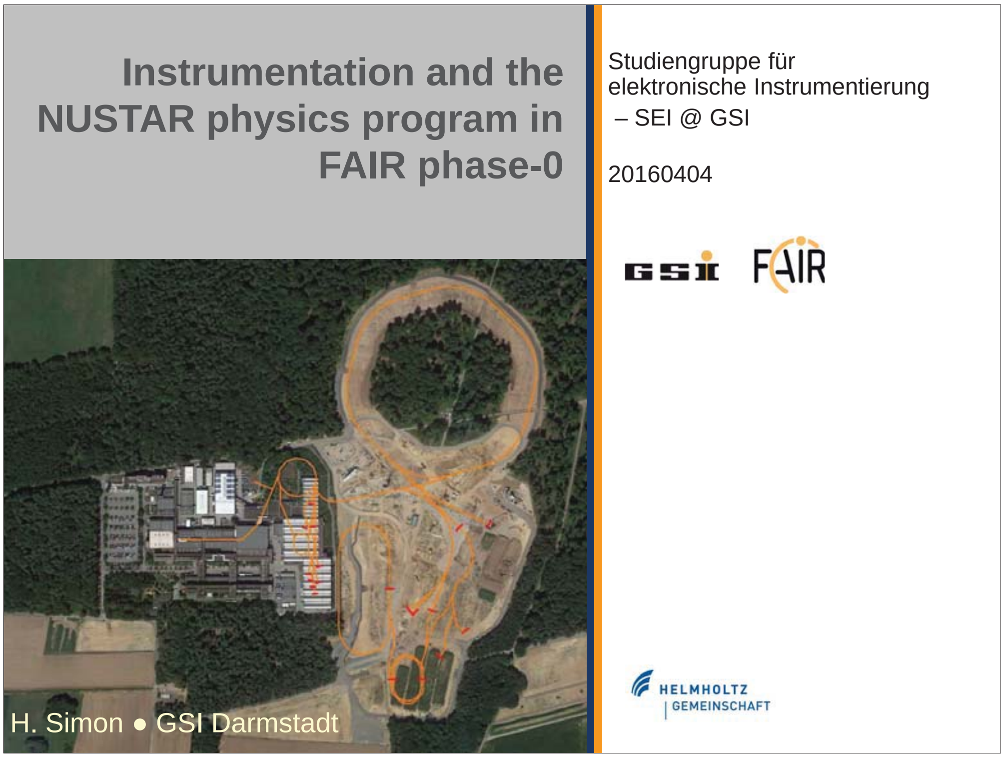
Optimierte Ausleuchtung und in-situ Kalibration von high-gain Antennen für die Detektion von ausgedehnten kosmischen Luftschauern *EISENBLäTTER, Lars*

Abschluss und Ausblick *GOETTLICHER, Peter*
Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung 12:45 - 13:00

13:00 **Mittagessen Mi**
Gebaeude KWB, GSI - Gesellschaft für Schwerionenforschung 13:00 - 14:00

14:00

15:00

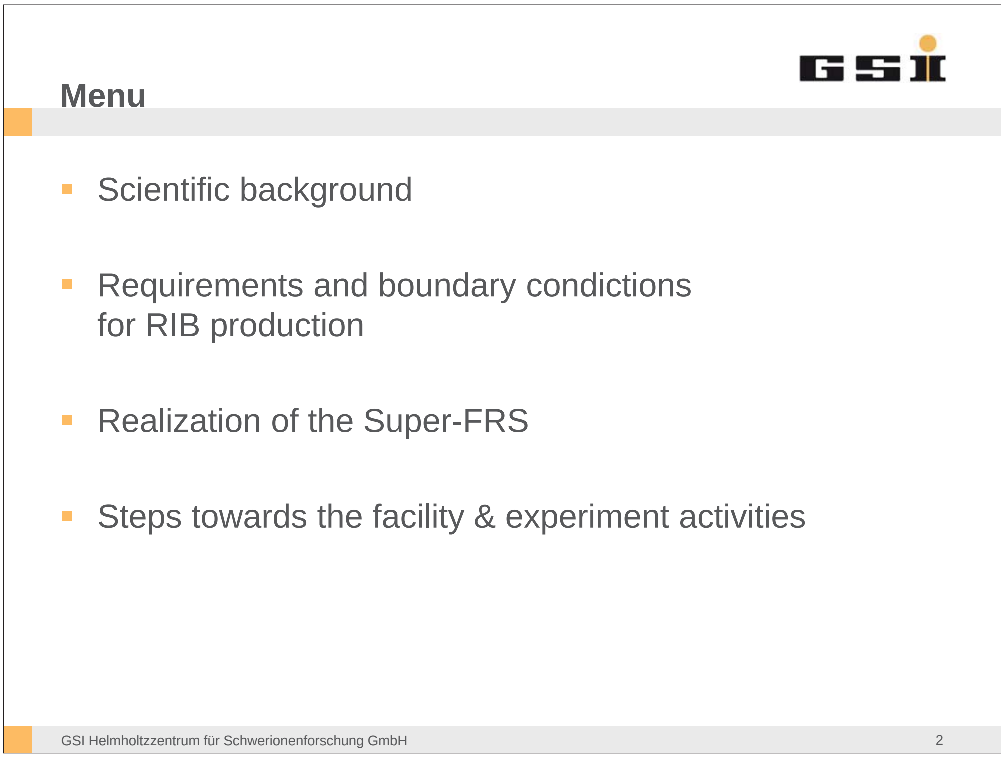


Instrumentation and the NUSTAR physics program in FAIR phase-0

H. Simon ● GSI Darmstadt

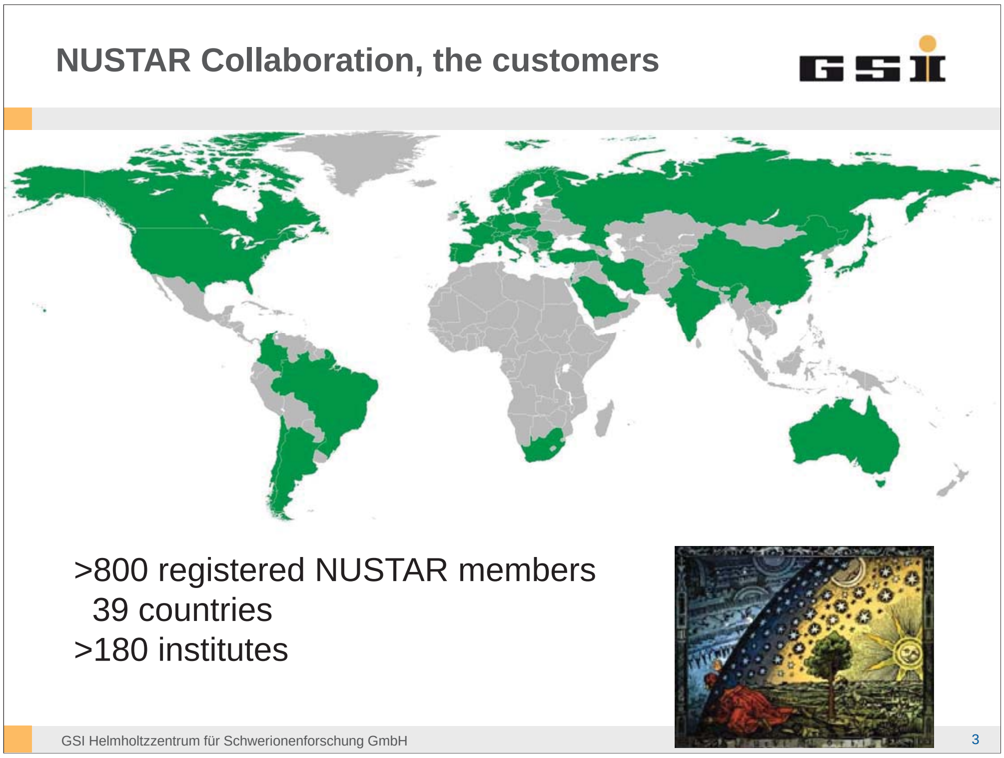
Studiengruppe für
elektronische Instrumentierung
– SEI @ GSI

20160404



Menu

- Scientific background
- Requirements and boundary conditions for RIB production
- Realization of the Super-FRS
- Steps towards the facility & experiment activities



NUSTAR Collaboration, the customers

>800 registered NUSTAR members
39 countries
>180 institutes

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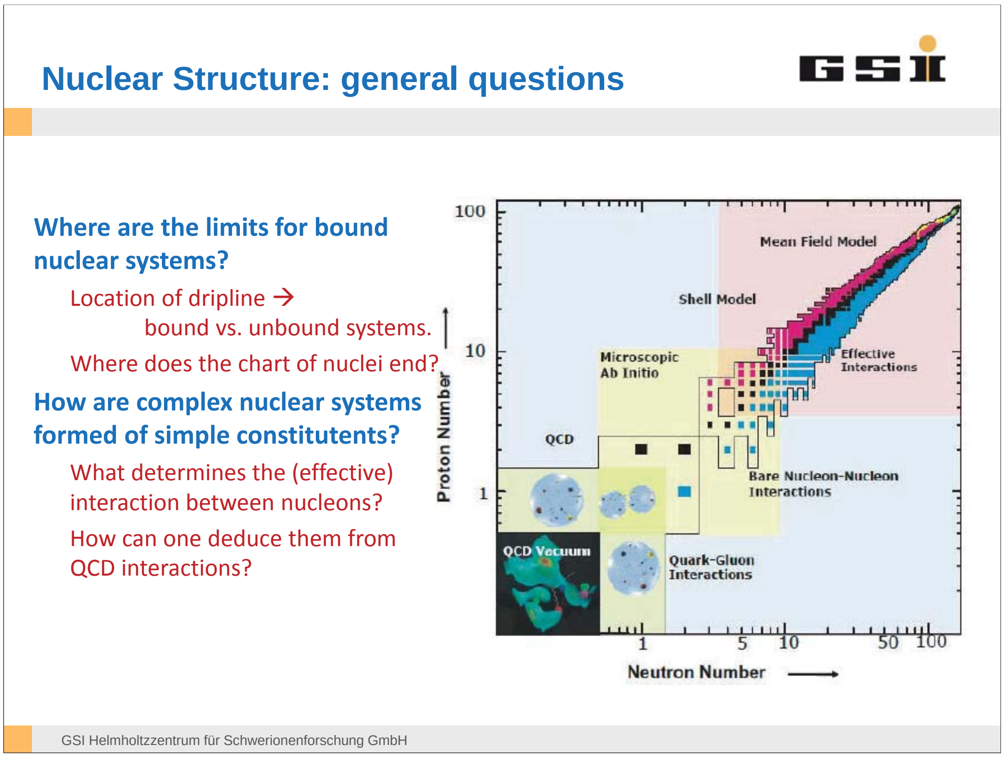

Nuclear Structure: general questions

Where are the limits for bound nuclear systems?

Location of dripline →
bound vs. unbound systems.

Where does the chart of nuclei end?

How are complex nuclear systems formed of simple constitutents?

What determines the (effective) interaction between nucleons?

How can one deduce them from QCD interactions?

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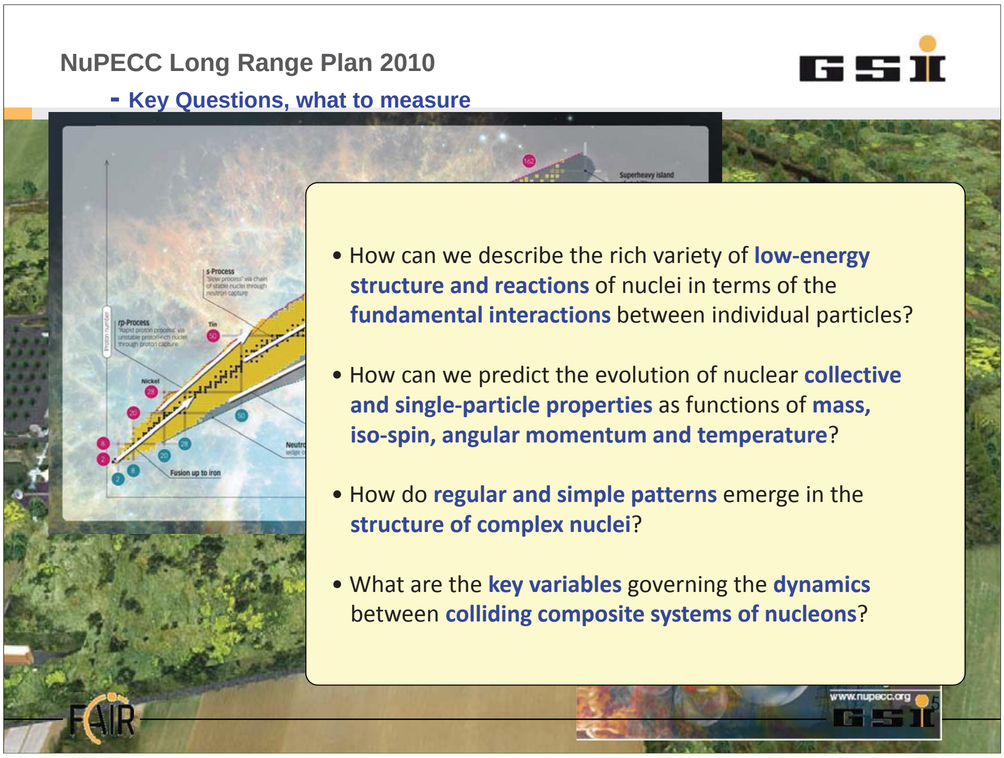
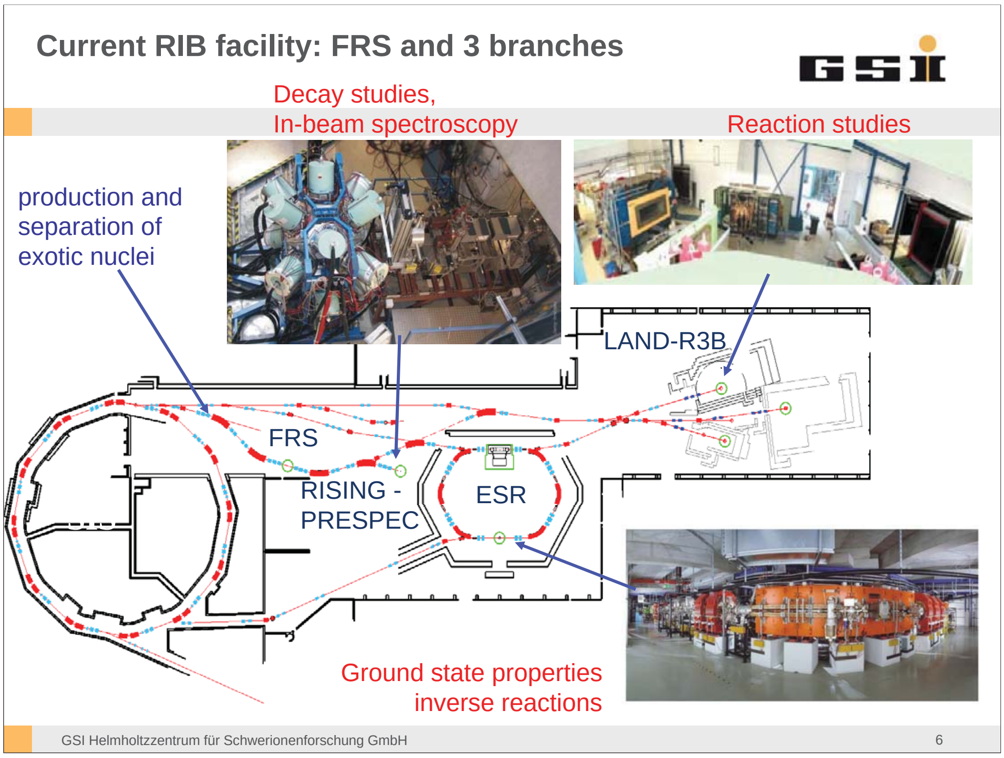


NuPECC Long Range Plan 2010

- Key Questions, what to measure

- How can we describe the rich variety of **low-energy structure and reactions** of nuclei in terms of the **fundamental interactions** between individual particles?
- How can we predict the evolution of nuclear **collective and single-particle properties** as functions of **mass, iso-spin, angular momentum and temperature**?
- How do **regular and simple patterns** emerge in the **structure of complex nuclei**?
- What are the **key variables** governing the **dynamics** between **colliding composite systems of nucleons**?



Current RIB facility: FRS and 3 branches

Decay studies,
In-beam spectroscopy

Reaction studies

production and separation of exotic nuclei

LAND-R3B

FRS

RISING - PRESPEC

ESR

Ground state properties
inverse reactions

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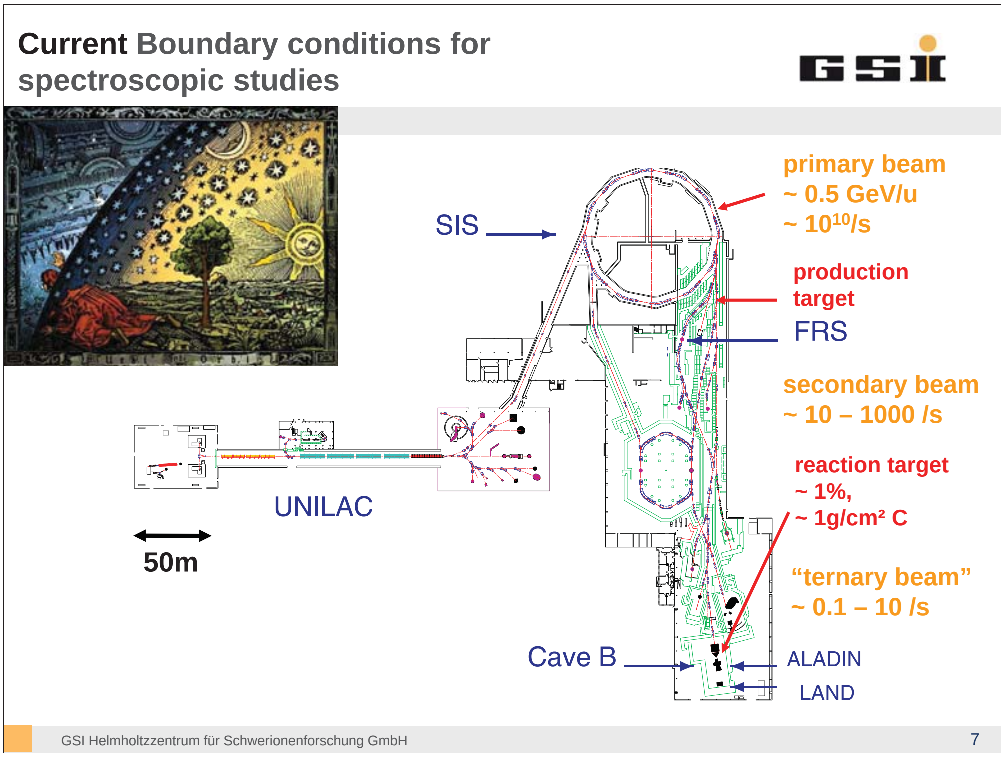

Current Boundary conditions for spectroscopic studies

SIS

primary beam
~ 0.5 GeV/u
~ 10^{10}/s

production target

FRS

secondary beam
~ 10 – 1000 /s

reaction target
~ 1%,
~ 1g/cm² C

“ternary beam”
~ 0.1 – 10 /s

Cave B

ALADIN

LAND

UNILAC

50m

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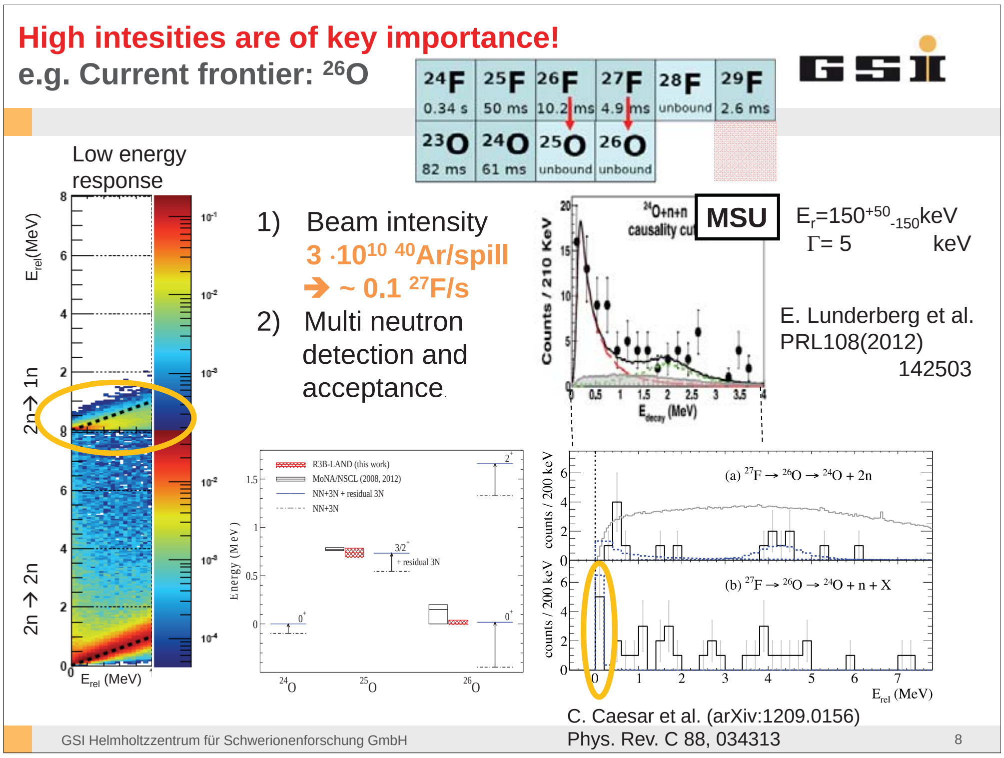

High intesities are of key importance!

e.g. Current frontier: ^{26}O

^{24}F 0.34 s	^{25}F 50 ms	^{26}F 10.2 ms	^{27}F 4.9 ms	^{28}F unbound	^{29}F 2.6 ms
^{23}O 82 ms	^{24}O 61 ms	^{25}O unbound	^{26}O unbound		

Low energy response

1) Beam intensity
3 ·10^{10} ^{40}Ar/spill
➔ ~ 0.1 ^{27}F/s

2) Multi neutron detection and acceptance.

MSU

E_r=150$^{+50}_{-150}$keV
Γ= 5 keV

E. Lunderberg et al.
PRL108(2012) 142503

C. Caesar et al. (arXiv:1209.0156)
Phys. Rev. C 88, 034313

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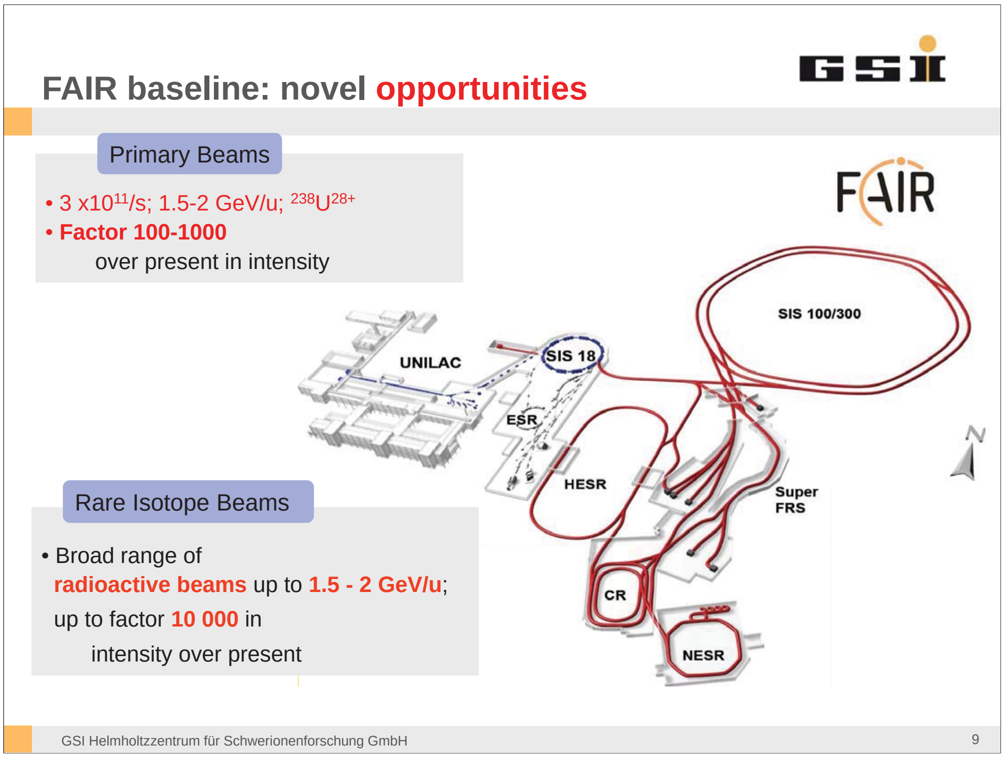


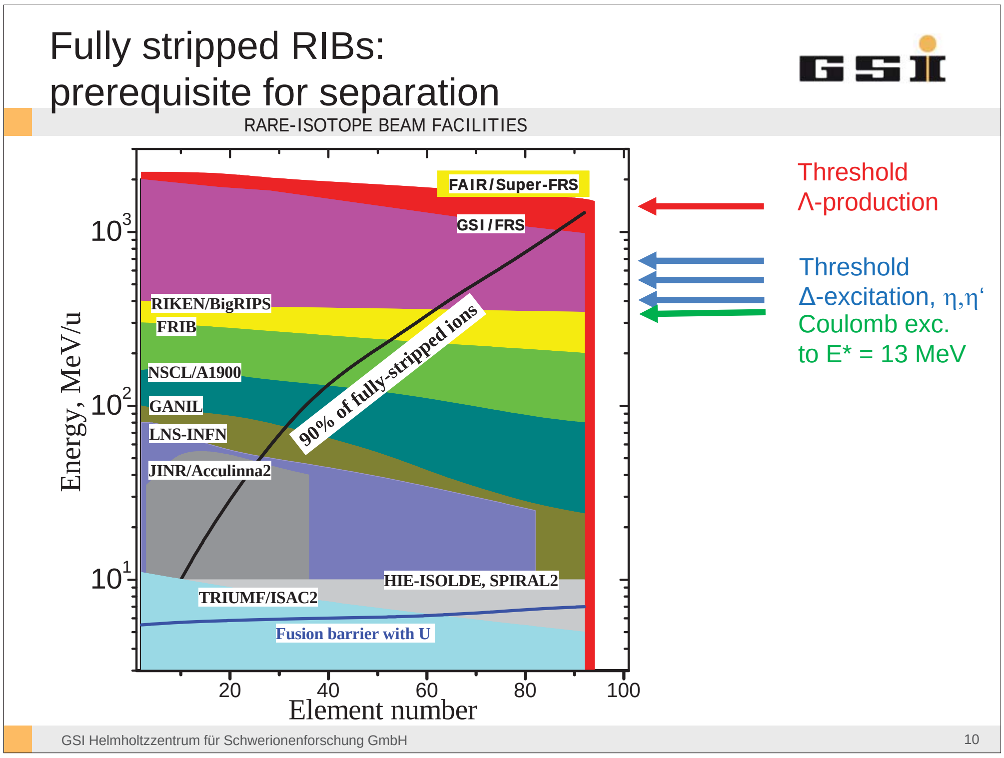
FAIR baseline: novel opportunities

Primary Beams

- 3 x10^{11}/s; 1.5-2 GeV/u; $^{238}U^{28+}$
- **Factor 100-1000** over present in intensity

Rare Isotope Beams

- Broad range of **radioactive beams** up to **1.5 - 2 GeV/u**; up to factor **10 000** in intensity over present



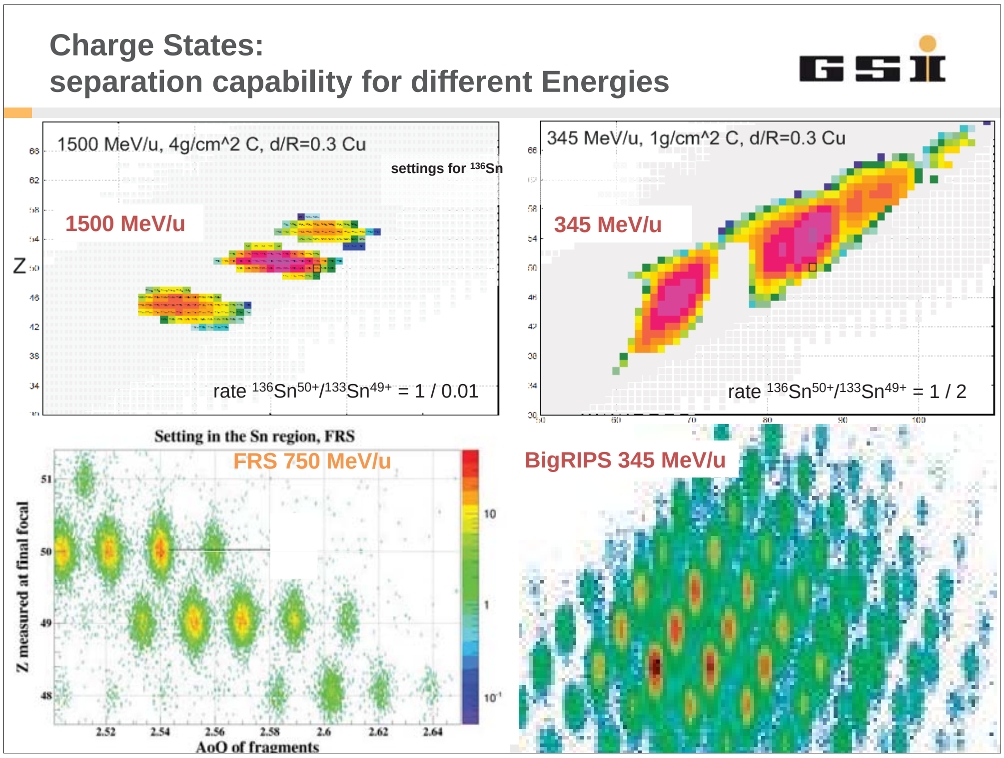
Fully stripped RIBs: prerequisite for separation

RARE-ISOTOPE BEAM FACILITIES

Threshold Λ-production

Threshold Δ-excitation, η,η‘

Coulomb exc. to E* = 13 MeV



Charge States:
separation capability for different Energies

1500 MeV/u, 4g/cm^2 C, d/R=0.3 Cu

settings for ^{136}Sn

1500 MeV/u

rate $^{136}Sn^{50+}/^{133}Sn^{49+}$ = 1 / 0.01

345 MeV/u, 1g/cm^2 C, d/R=0.3 Cu

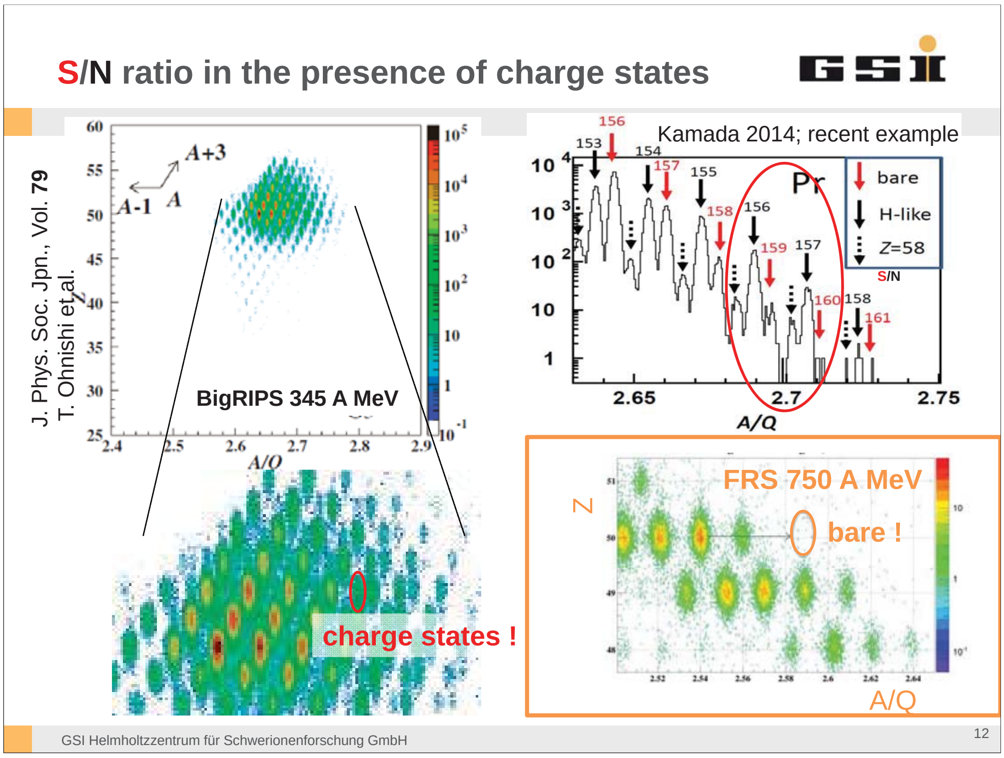
345 MeV/u

rate $^{136}Sn^{50+}/^{133}Sn^{49+}$ = 1 / 2

Setting in the Sn region, FRS

FRS 750 MeV/u

BigRIPS 345 MeV/u



S/N ratio in the presence of charge states

J. Phys. Soc. Jpn., Vol. 79
T. Ohnishi et al.

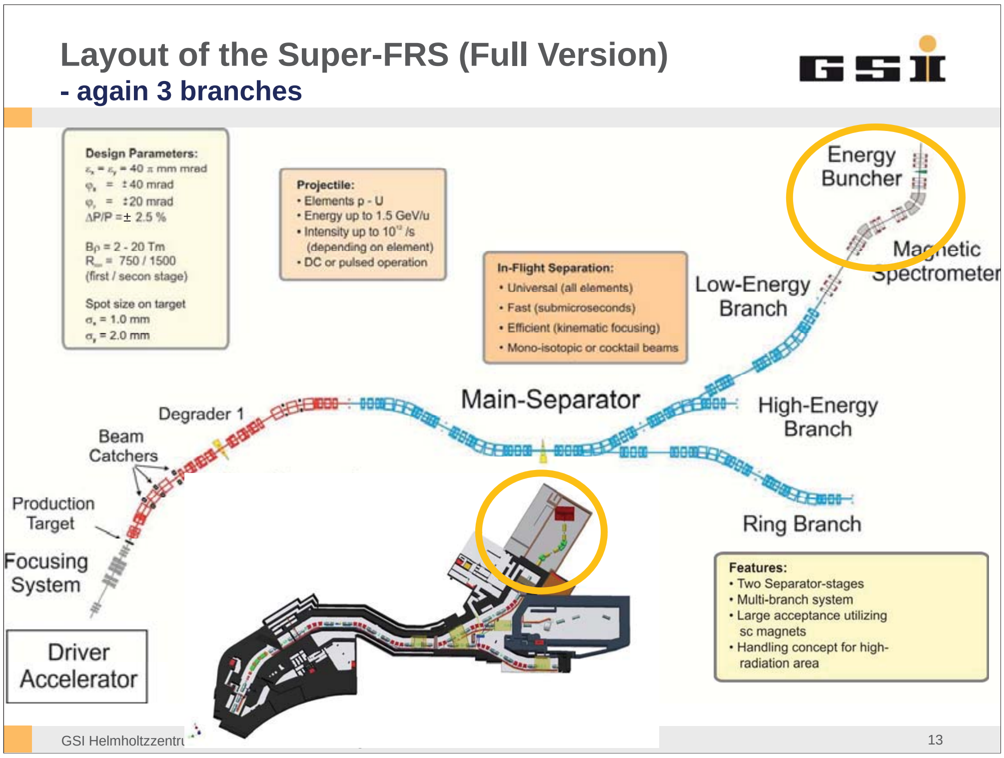
BigRIPS 345 A MeV

Kamada 2014; recent example

charge states !

FRS 750 A MeV

bare !



Layout of the Super-FRS (Full Version)

- again 3 branches

Design Parameters:
$\varepsilon_x = \varepsilon_y = 40\ \pi$ mm mrad
φ_x = ±40 mrad
φ_y = ±20 mrad
$\Delta P/P = \pm 2.5$ %

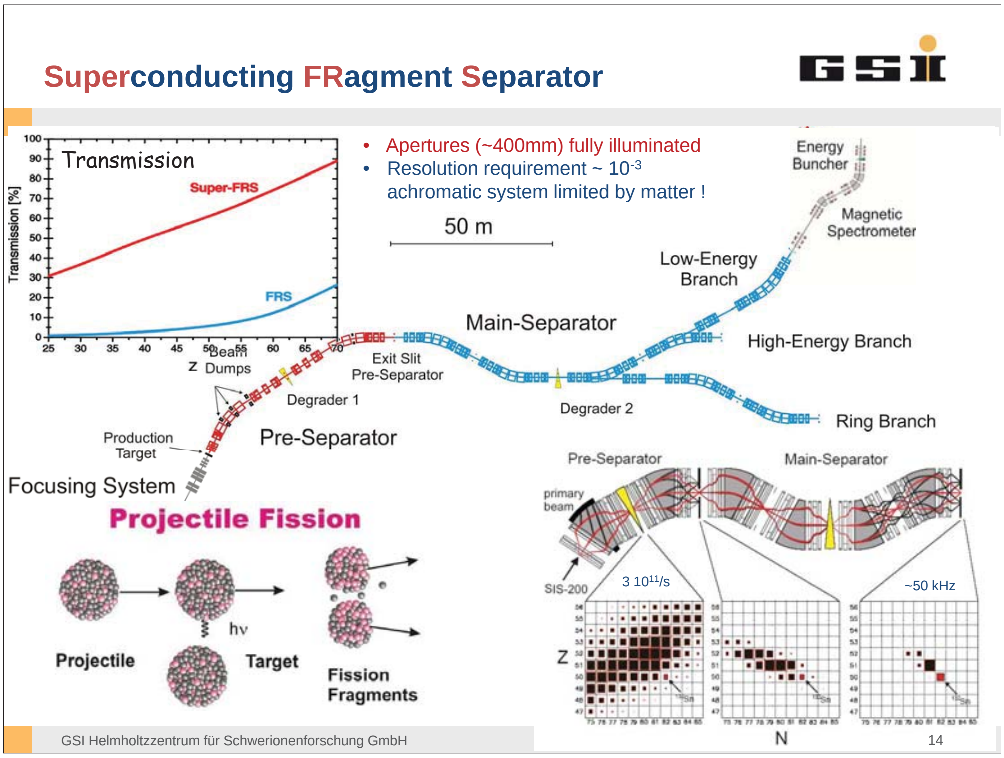
$B\rho$ = 2 - 20 Tm
$R_{...}$ = 750 / 1500
(first / secon stage)

Spot size on target
σ_x = 1.0 mm
σ_y = 2.0 mm

Projectile:
- Elements p - U
- Energy up to 1.5 GeV/u
- Intensity up to 10^{12} /s (depending on element)
- DC or pulsed operation

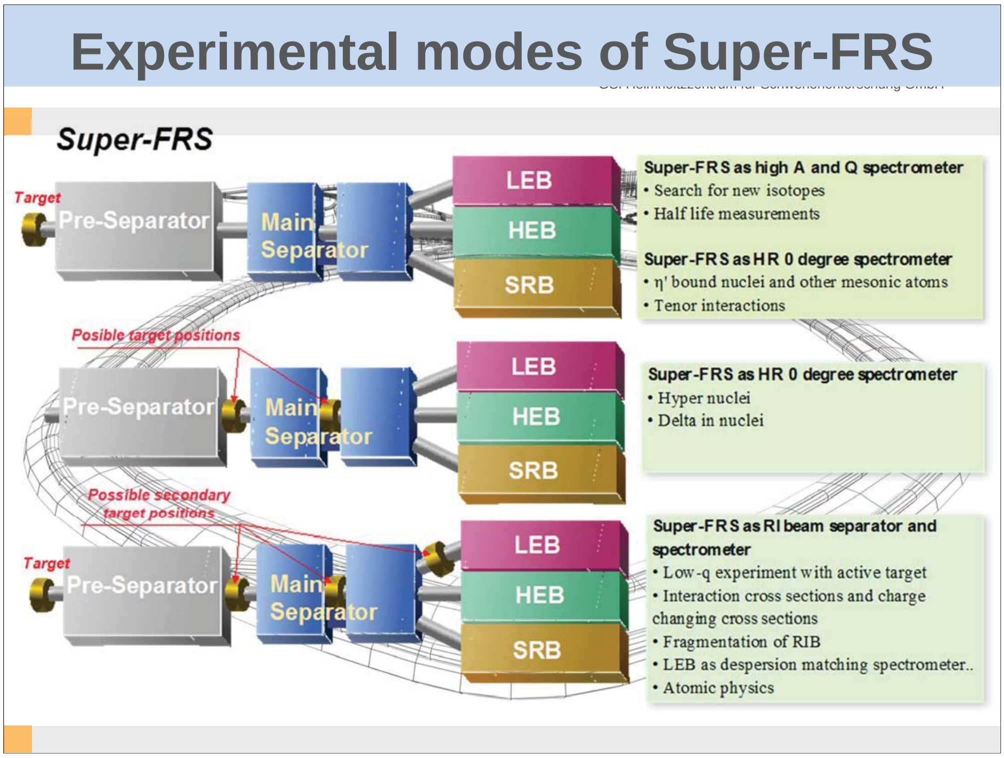
In-Flight Separation:
- Universal (all elements)
- Fast (submicroseconds)
- Efficient (kinematic focusing)
- Mono-isotopic or cocktail beams

Features:
- Two Separator-stages
- Multi-branch system
- Large acceptance utilizing sc magnets
- Handling concept for high-radiation area



Superconducting FRagment Separator

- Apertures (~400mm) fully illuminated
- Resolution requirement ~ 10^{-3}
achromatic system limited by matter !



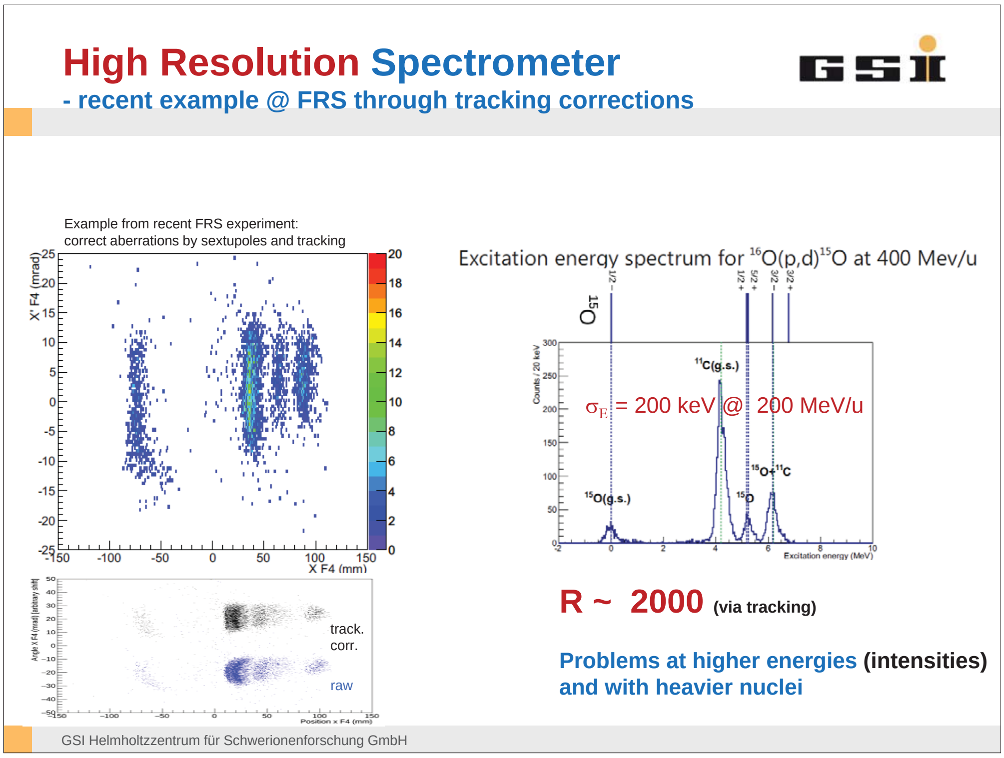
Experimental modes of Super-FRS

Super-FRS as high A and Q spectrometer
- Search for new isotopes
- Half life measurements

Super-FRS as HR 0 degree spectrometer
- η' bound nuclei and other mesonic atoms
- Tenor interactions

Super-FRS as HR 0 degree spectrometer
- Hyper nuclei
- Delta in nuclei

Super-FRS as RI beam separator and spectrometer
- Low-q experiment with active target
- Interaction cross sections and charge changing cross sections
- Fragmentation of RIB
- LEB as despersion matching spectrometer..
- Atomic physics



High Resolution Spectrometer

- recent example @ FRS through tracking corrections

Example from recent FRS experiment:
correct aberrations by sextupoles and tracking

Excitation energy spectrum for $^{16}O(p,d)^{15}O$ at 400 Mev/u

σ_E = 200 keV @ 200 MeV/u

R ~ 2000 (via tracking)

Problems at higher energies (intensities) and with heavier nuclei

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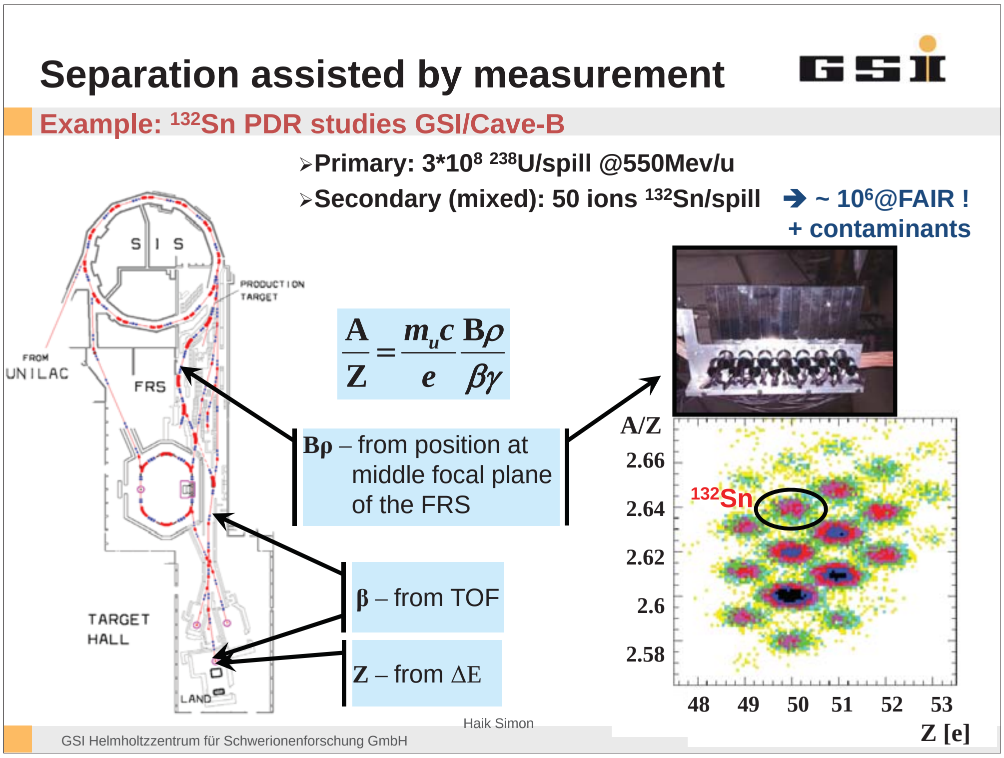

Separation assisted by measurement

Example: ^{132}Sn PDR studies GSI/Cave-B

- **Primary: 3*10^8 ^{238}U/spill @550Mev/u**
- **Secondary (mixed): 50 ions ^{132}Sn/spill** ➔ **~ 10^6@FAIR !** **+ contaminants**

$$\frac{A}{Z} = \frac{m_u c}{e}\,\frac{B\rho}{\beta\gamma}$$

Bρ – from position at middle focal plane of the FRS

β – from TOF

Z – from ΔE

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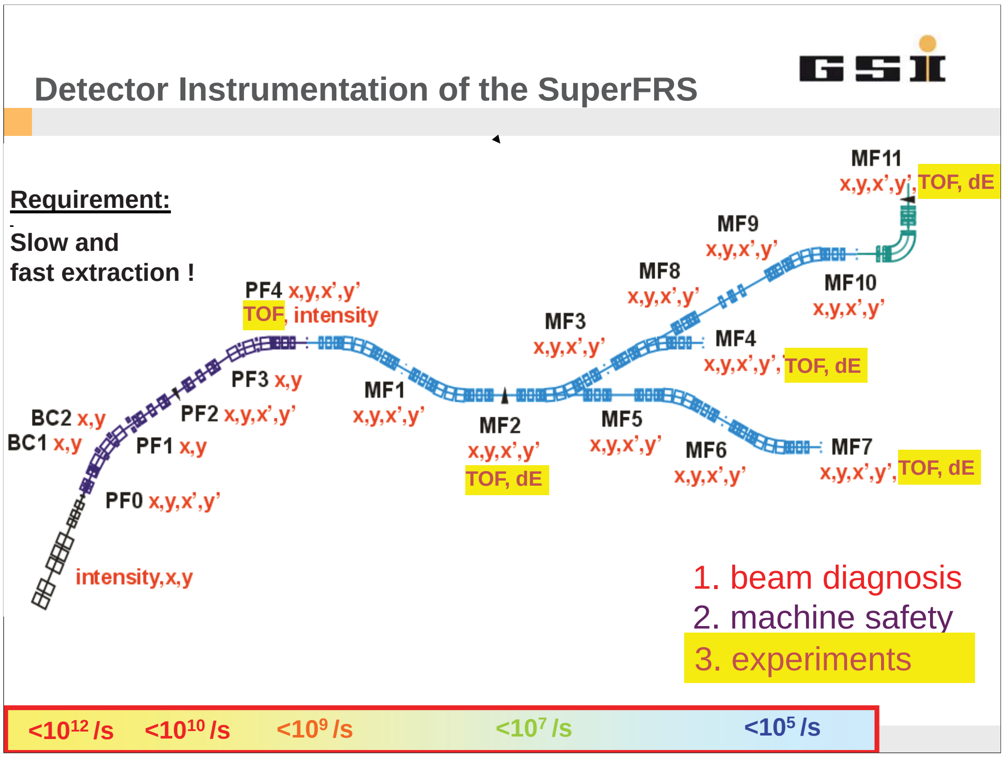
Haik Simon



Detector Instrumentation of the SuperFRS

Requirement:

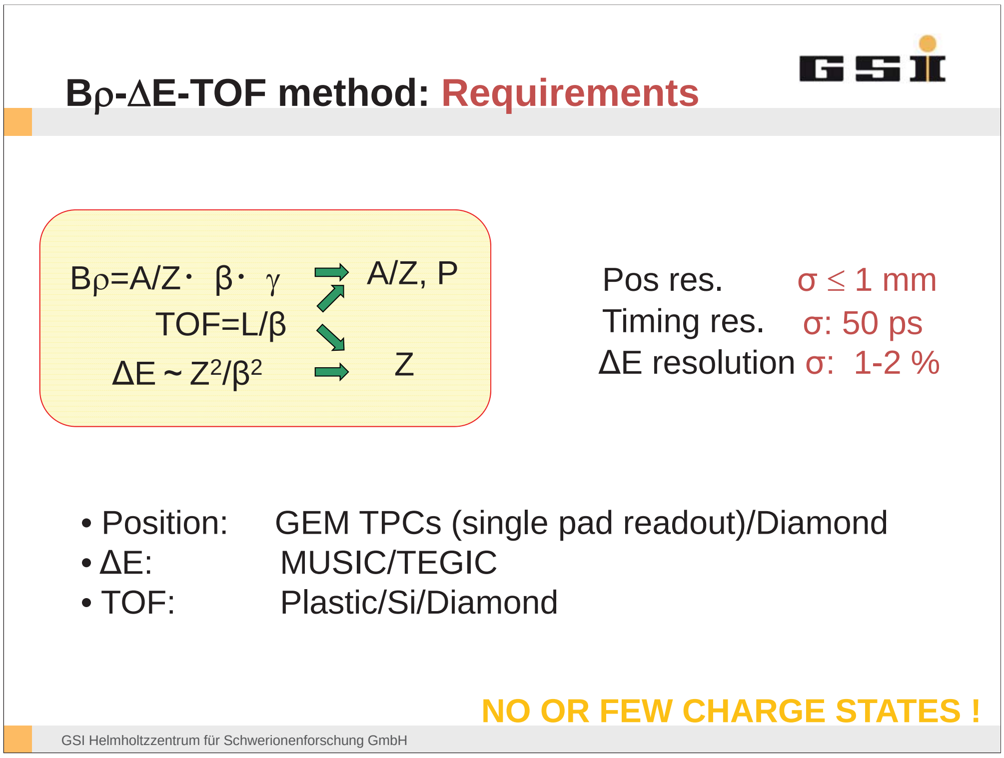
Slow and fast extraction !

1. beam diagnosis
2. machine safety
3. experiments

$<10^{12}$ /s $<10^{10}$ /s $<10^{9}$ /s $<10^{7}$ /s $<10^{5}$ /s

Specific Design !

Haik Simon



Bρ-ΔE-TOF method: Requirements

$B\rho = A/Z \cdot \beta \cdot \gamma \Rightarrow$ A/Z, P

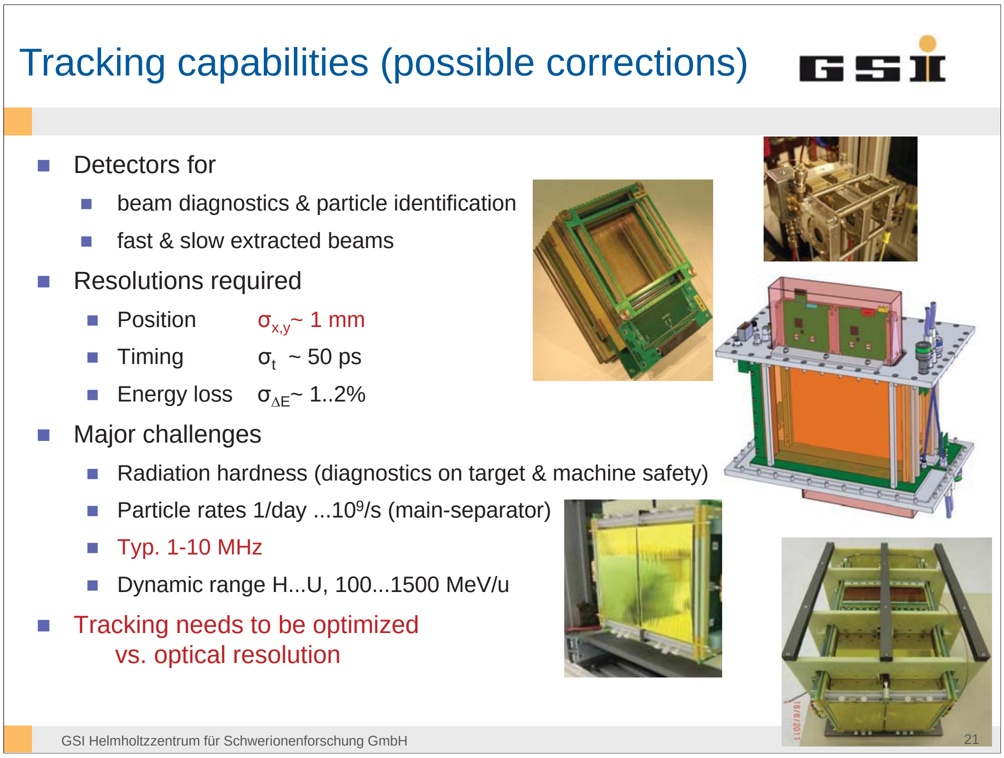
$TOF = L/\beta$

$\Delta E \sim Z^2/\beta^2 \Rightarrow$ Z

Pos res.	σ ≤ 1 mm
Timing res.	σ: 50 ps
ΔE resolution	σ: 1-2 %

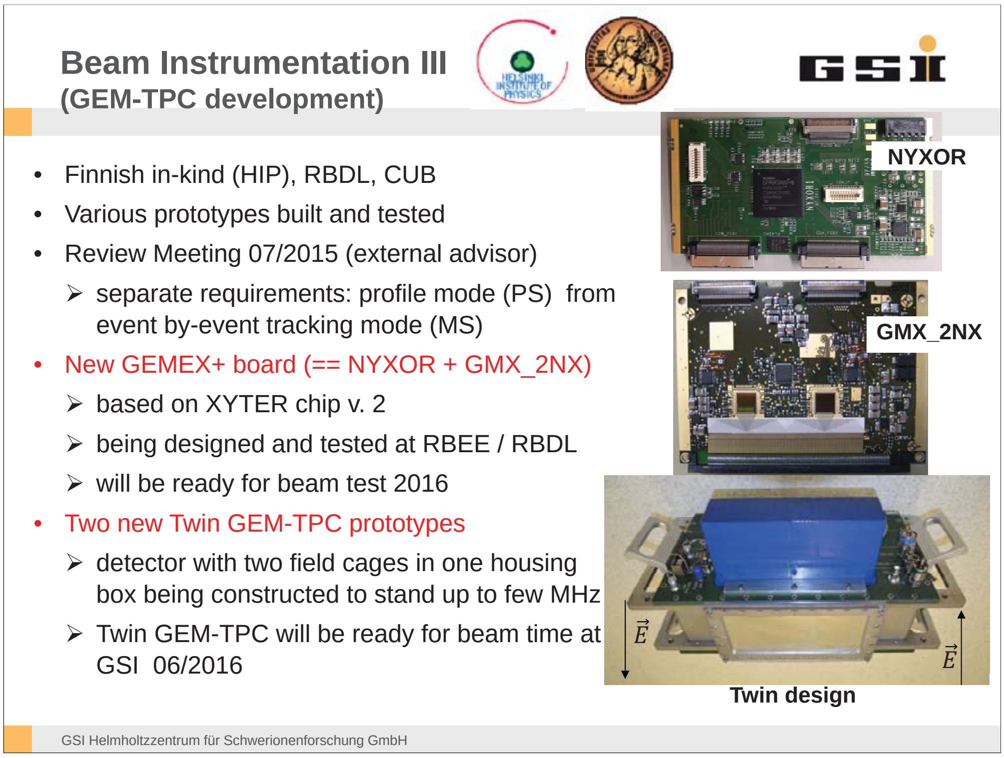
- Position: GEM TPCs (single pad readout)/Diamond
- ΔE: MUSIC/TEGIC
- TOF: Plastic/Si/Diamond

NO OR FEW CHARGE STATES !



Tracking capabilities (possible corrections)

- Detectors for
  - beam diagnostics & particle identification
  - fast & slow extracted beams
- Resolutions required
  - Position $\sigma_{x,y}$~ 1 mm
  - Timing σ_t ~ 50 ps
  - Energy loss $\sigma_{\Delta E}$~ 1..2%
- Major challenges
  - Radiation hardness (diagnostics on target & machine safety)
  - Particle rates 1/day ...10^9/s (main-separator)
  - Typ. 1-10 MHz
  - Dynamic range H...U, 100...1500 MeV/u
- Tracking needs to be optimized vs. optical resolution

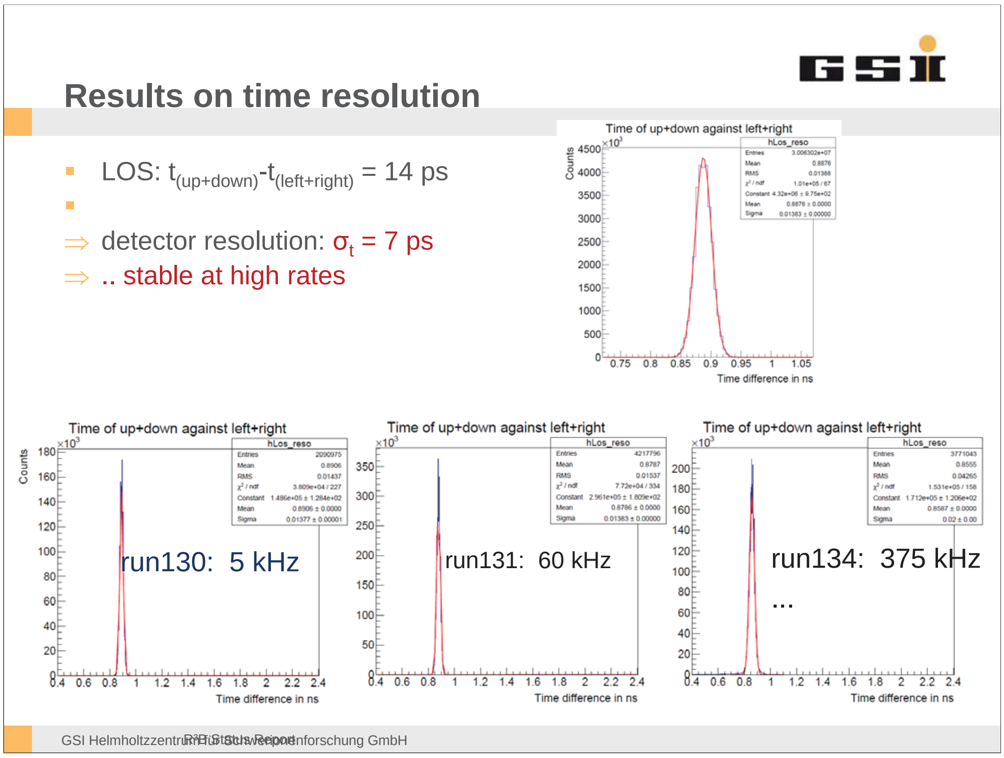


Beam Instrumentation III
(GEM-TPC development)

- Finnish in-kind (HIP), RBDL, CUB
- Various prototypes built and tested
- Review Meeting 07/2015 (external advisor)
  - ➢ separate requirements: profile mode (PS) from event by-event tracking mode (MS)
- New GEMEX+ board (== NYXOR + GMX_2NX)
  - ➢ based on XYTER chip v. 2
  - ➢ being designed and tested at RBEE / RBDL
  - ➢ will be ready for beam test 2016
- Two new Twin GEM-TPC prototypes
  - ➢ detector with two field cages in one housing box being constructed to stand up to few MHz
  - ➢ Twin GEM-TPC will be ready for beam time at GSI 06/2016

The new start detector LOS

- EJ230 scintillator with thickness of 0.5 mm
- Aluminum frame for stabilization of thin scintillator foils (e.g. 50 µm)
- active area: 5 x 5 cm^2
- 4 Hamamatsu R9779-20 PMs, TTS: 250 ps
- Mesytec MCFD16-PMT constant fraction discriminator



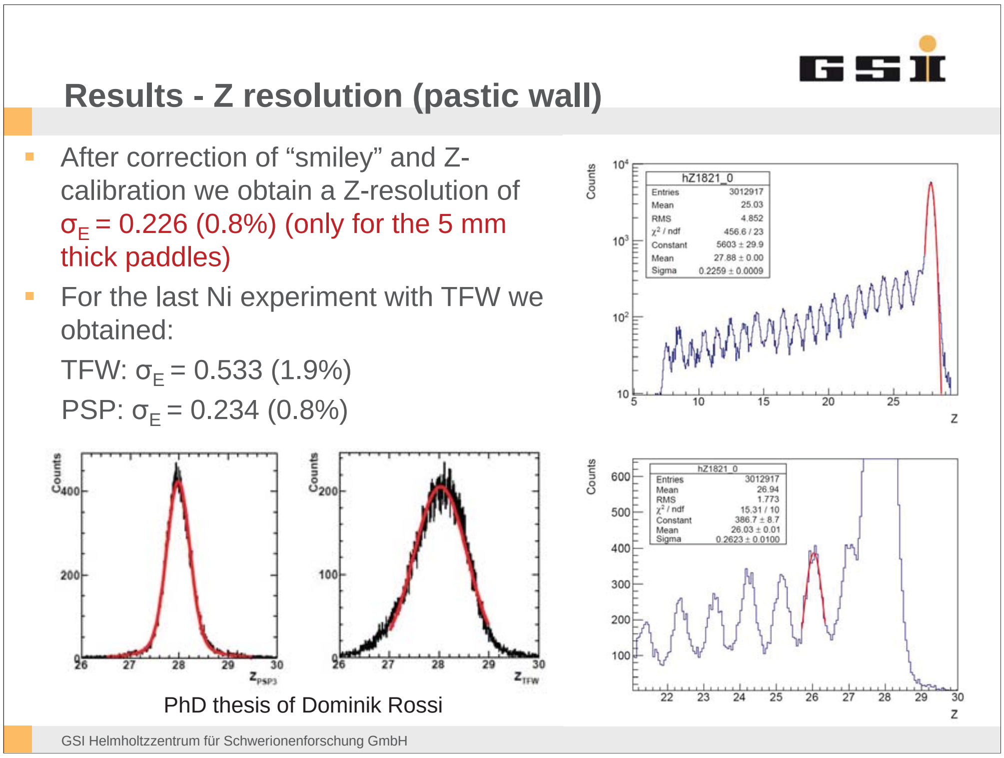
Results on time resolution

- LOS: $t_{(up+down)}-t_{(left+right)}$ = 14 ps

⇒ detector resolution: σ_t = 7 ps

⇒ .. stable at high rates

GSI Helmholtzzentrum für Schwerionenforschung GmbH R3B Status Report



Results - Z resolution (pastic wall)

- After correction of “smiley” and Z-calibration we obtain a Z-resolution of σ_E = 0.226 (0.8%) (only for the 5 mm thick paddles)
- For the last Ni experiment with TFW we obtained:

TFW: σ_E = 0.533 (1.9%)

PSP: σ_E = 0.234 (0.8%)

PhD thesis of Dominik Rossi

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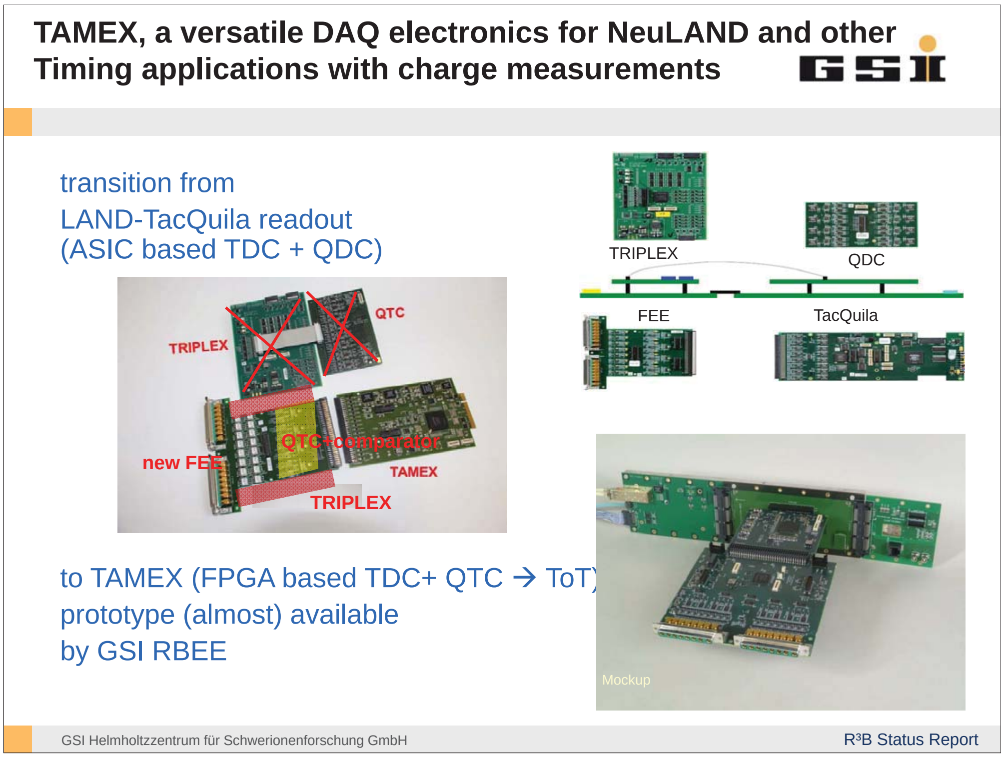

TAMEX, a versatile DAQ electronics for NeuLAND and other Timing applications with charge measurements

transition from
LAND-TacQuila readout
(ASIC based TDC + QDC)

to TAMEX (FPGA based TDC+ QTC → ToT)
prototype (almost) available
by GSI RBEE

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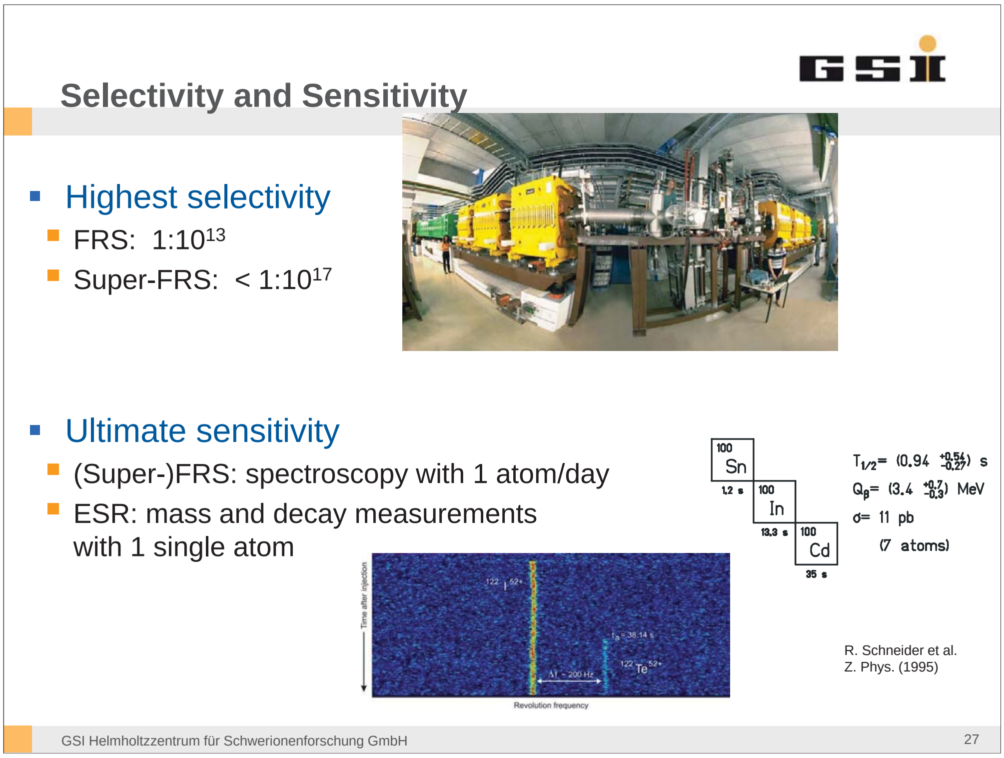
R³B Status Report

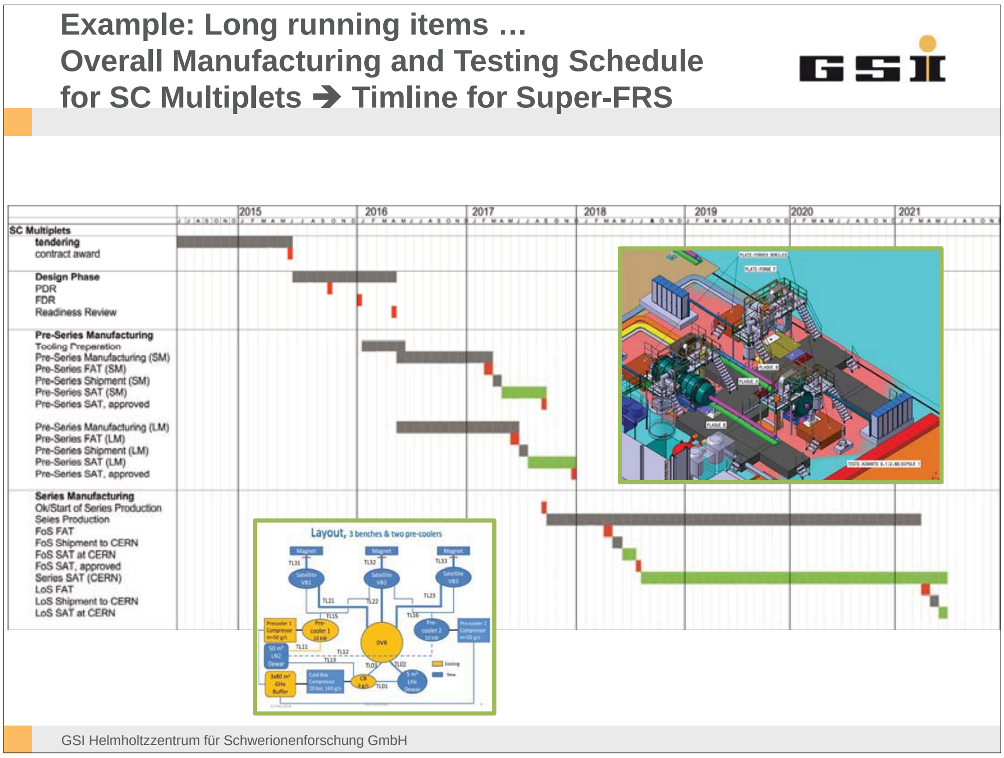


Selectivity and Sensitivity

- Highest selectivity
  - FRS: 1:10^{13}
  - Super-FRS: < 1:10^{17}
- Ultimate sensitivity
  - (Super-)FRS: spectroscopy with 1 atom/day
  - ESR: mass and decay measurements with 1 single atom

$T_{1/2} = (0.94\ ^{+0.54}_{-0.27})$ s
$Q_\beta = (3.4\ ^{+0.7}_{-0.3})$ MeV
σ = 11 pb
(7 atoms)

R. Schneider et al.
Z. Phys. (1995)



Example: Long running items …
Overall Manufacturing and Testing Schedule for SC Multiplets ➔ Timline for Super-FRS

SC Multiplets
tendering
contract award

Design Phase
PDR
FDR
Readiness Review

Pre-Series Manufacturing
Tooling Preperation
Pre-Series Manufacturing (SM)
Pre-Series FAT (SM)
Pre-Series Shipment (SM)
Pre-Series SAT (SM)
Pre-Series SAT, approved

Pre-Series Manufacturing (LM)
Pre-Series FAT (LM)
Pre-Series Shipment (LM)
Pre-Series SAT (LM)
Pre-Series SAT, approved

Series Manufacturing
Ok/Start of Series Production
Seies Production
FoS FAT
FoS Shipment to CERN
FoS SAT at CERN
FoS SAT, approved
Series SAT (CERN)
LoS FAT
LoS Shipment to CERN
LoS SAT at CERN

GLAD has arrived and is being installed in Cave-C

- Power supply there and tested
- Crypo plant installed and tested
- Magnet has arrived and passed first series of SAT tests

➔ non conformity in the exit flange mitigation in progress

- in-kind contracts with F/D in preparation

- 04/2016 installation of instrumentation and MSS/MCS by CEA
- End 2016 to get magnet into operation!

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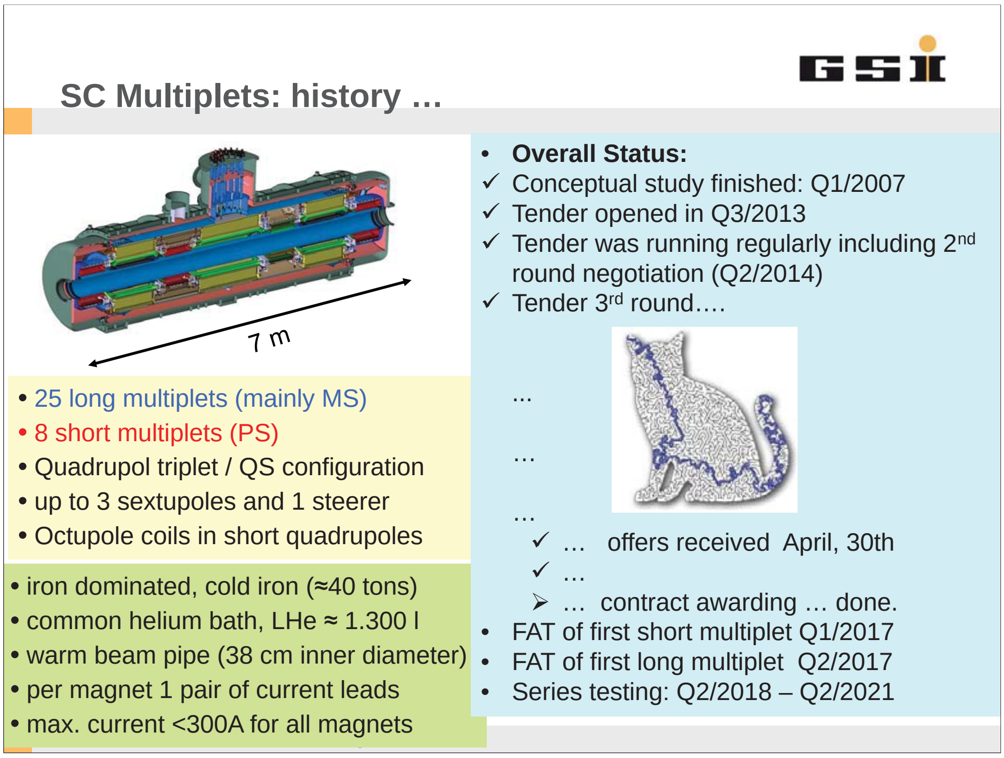
R^{3}B Status Report



SC Multiplets: history …

- 25 long multiplets (mainly MS)
- 8 short multiplets (PS)
- Quadrupol triplet / QS configuration
- up to 3 sextupoles and 1 steerer
- Octupole coils in short quadrupoles

- iron dominated, cold iron (≈40 tons)
- common helium bath, LHe ≈ 1.300 l
- warm beam pipe (38 cm inner diameter)
- per magnet 1 pair of current leads
- max. current <300A for all magnets

- **Overall Status:**

✓ Conceptual study finished: Q1/2007
✓ Tender opened in Q3/2013
✓ Tender was running regularly including 2nd round negotiation (Q2/2014)
✓ Tender 3rd round….

…

…

…

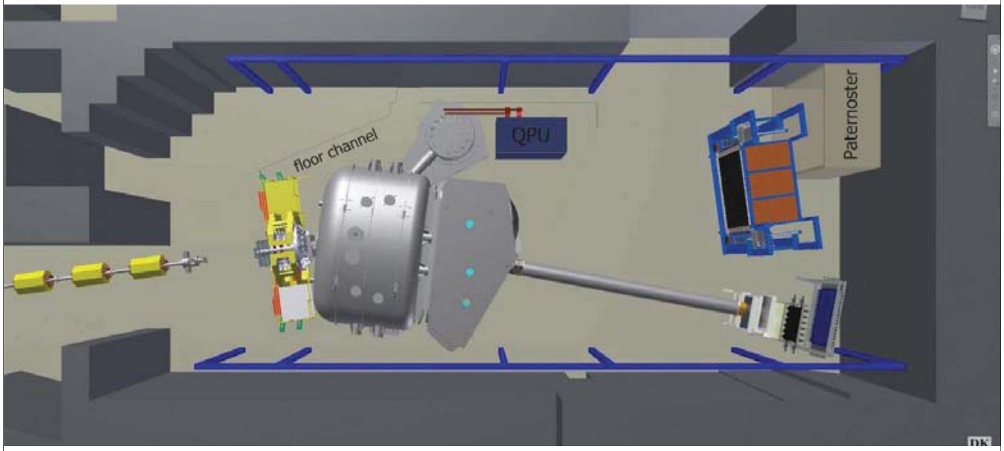
✓ … offers received April, 30th
✓ …
➢ … contract awarding … done.

- FAT of first short multiplet Q1/2017
- FAT of first long multiplet Q2/2017
- Series testing: Q2/2018 – Q2/2021

Definition of NUSTAR experiment phases

- **Phase 0 (2017-)**
  - R&D and experiments to be carried out with present facilities and FAIR/NUSTAR equipment
- **Phase 1 (2022 -)**
  - Core detectors and subsystems completed
  - First measurements with FAIR/Super-FRS beams
    - ➢ **Carry out experiments with highest visibility as part of the core program and within the FAIR MSV**
- **Phase 2**
  - FAIR evolving towards full power
  - Completion of experiments within MSV
    - ➢ **Essentially the full program of MSV can be performed**
- **Phase 3**
  - Moderate projects, which have been initiated on the way (outside MSV) can be included (e.g. experiments related to return line for rings)
- **Phase 4**
  - Major new investments and upgrades for all experiments

GLAD @ Cave-C



GLAD has arrived and is being installed in Cave-C

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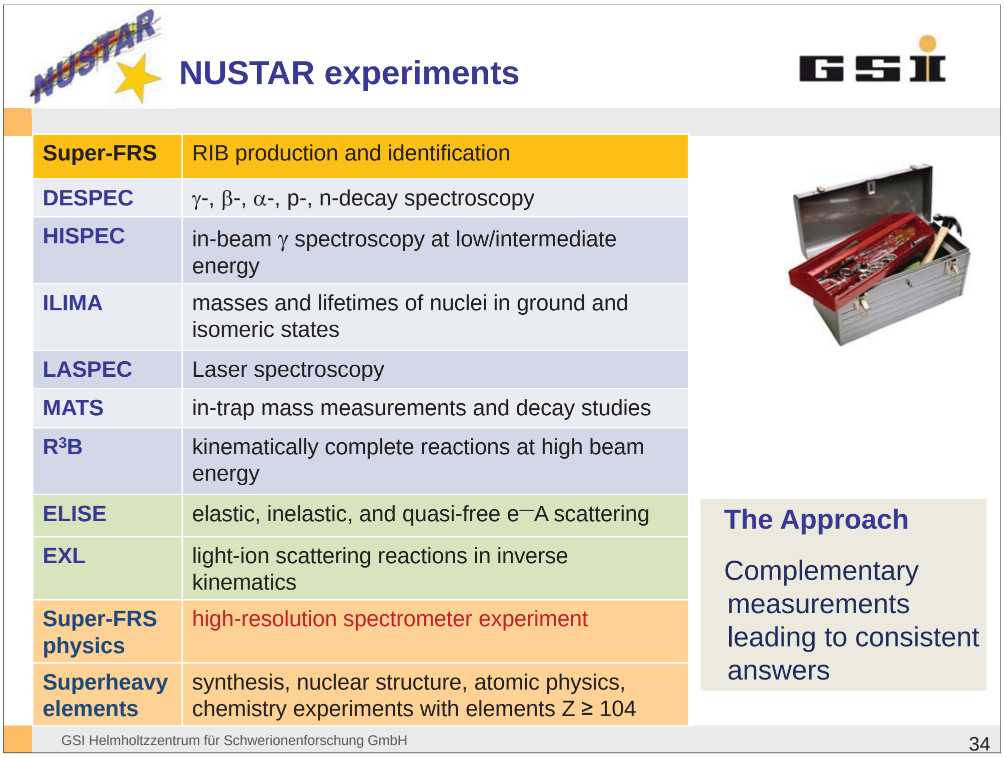

NUSTAR experiments

Super-FRS	RIB production and identification
DESPEC	γ-, β-, α-, p-, n-decay spectroscopy
HISPEC	in-beam γ spectroscopy at low/intermediate energy
ILIMA	masses and lifetimes of nuclei in ground and isomeric states
LASPEC	Laser spectroscopy
MATS	in-trap mass measurements and decay studies
R³B	kinematically complete reactions at high beam energy
ELISE	elastic, inelastic, and quasi-free e–A scattering
EXL	light-ion scattering reactions in inverse kinematics
Super-FRS physics	high-resolution spectrometer experiment
Superheavy elements	synthesis, nuclear structure, atomic physics, chemistry experiments with elements Z ≥ 104

The Approach

Complementary measurements leading to consistent answers

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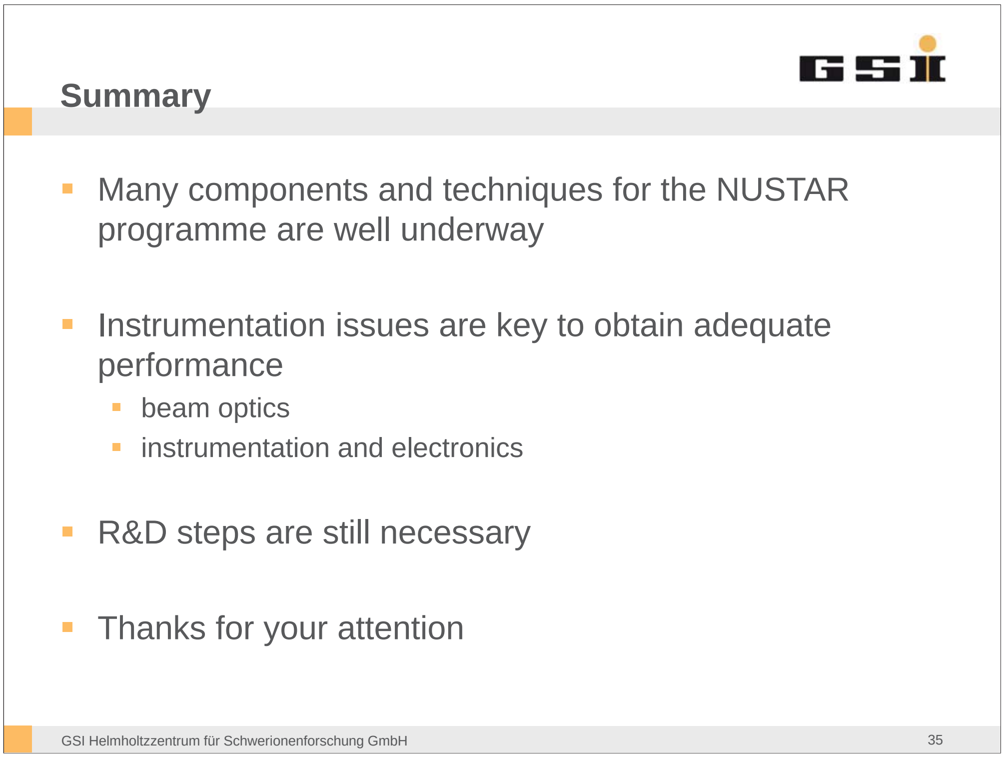
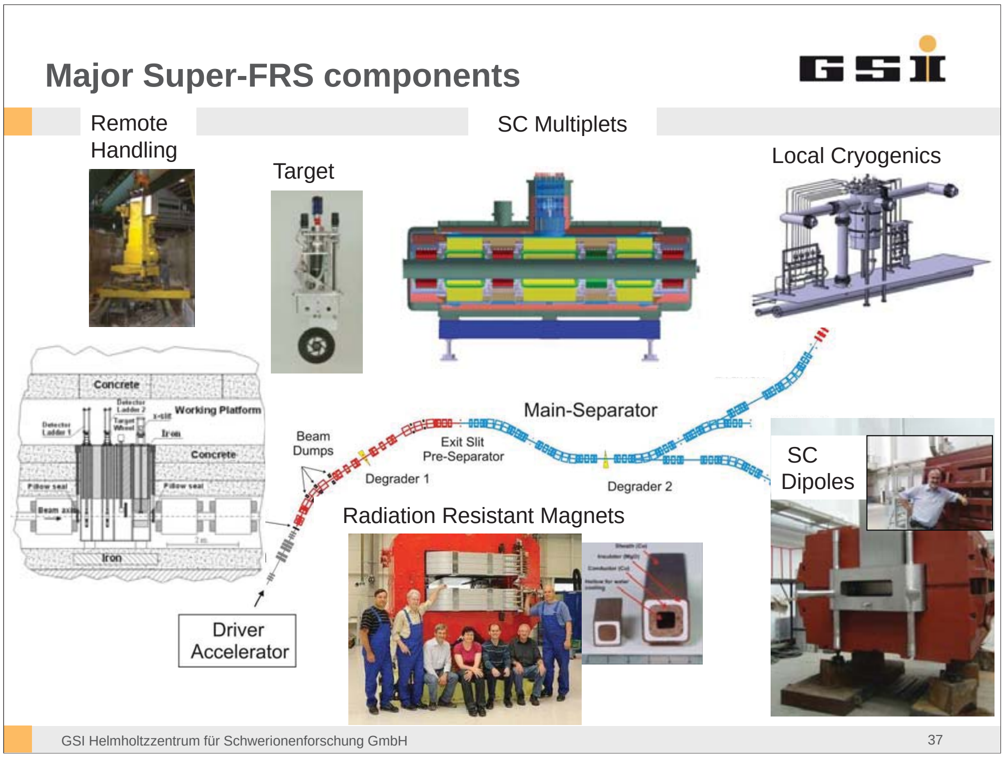


Summary

- Many components and techniques for the NUSTAR programme are well underway
- Instrumentation issues are key to obtain adequate performance
  - beam optics
  - instrumentation and electronics
- R&D steps are still necessary
- Thanks for your attention



Major Super-FRS components

Remote Handling

SC Multiplets

Target

Local Cryogenics

Main-Separator

Beam Dumps

Exit Slit

Pre-Separator

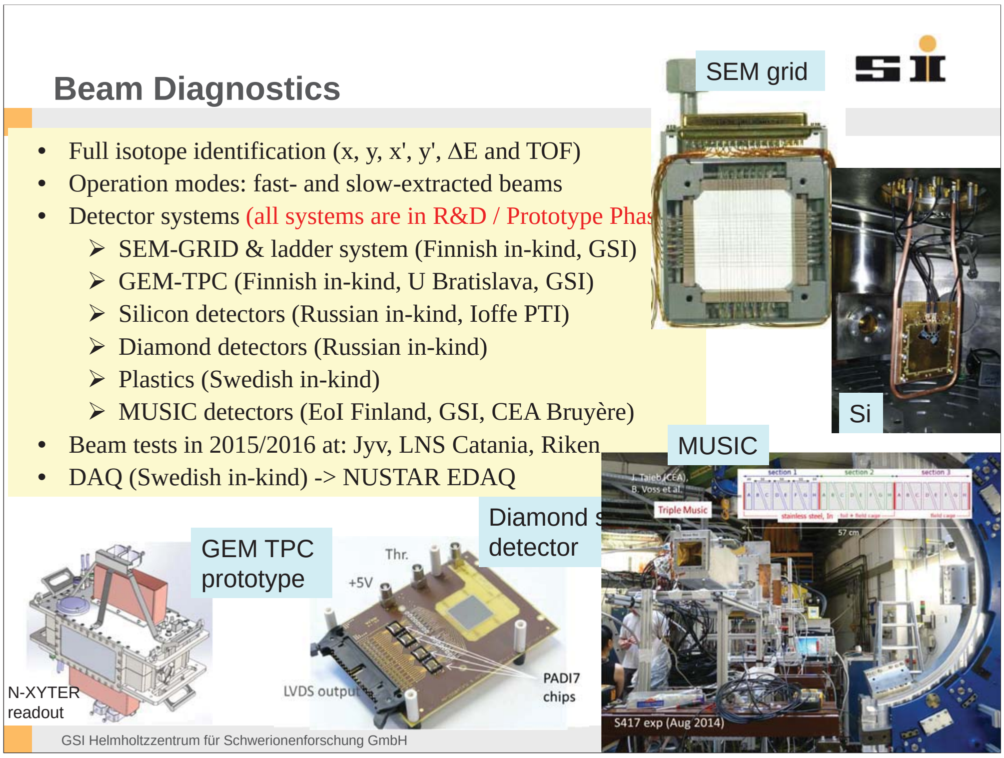
Degrader 1

Degrader 2

SC Dipoles

Radiation Resistant Magnets

Driver Accelerator



Beam Diagnostics

- Full isotope identification (x, y, x', y', ΔE and TOF)
- Operation modes: fast- and slow-extracted beams
- Detector systems (all systems are in R&D / Prototype Phas
  - ➢ SEM-GRID & ladder system (Finnish in-kind, GSI)
  - ➢ GEM-TPC (Finnish in-kind, U Bratislava, GSI)
  - ➢ Silicon detectors (Russian in-kind, Ioffe PTI)
  - ➢ Diamond detectors (Russian in-kind)
  - ➢ Plastics (Swedish in-kind)
  - ➢ MUSIC detectors (EoI Finland, GSI, CEA Bruyère)
- Beam tests in 2015/2016 at: Jyv, LNS Catania, Riken
- DAQ (Swedish in-kind) -> NUSTAR EDAQ

SEM grid

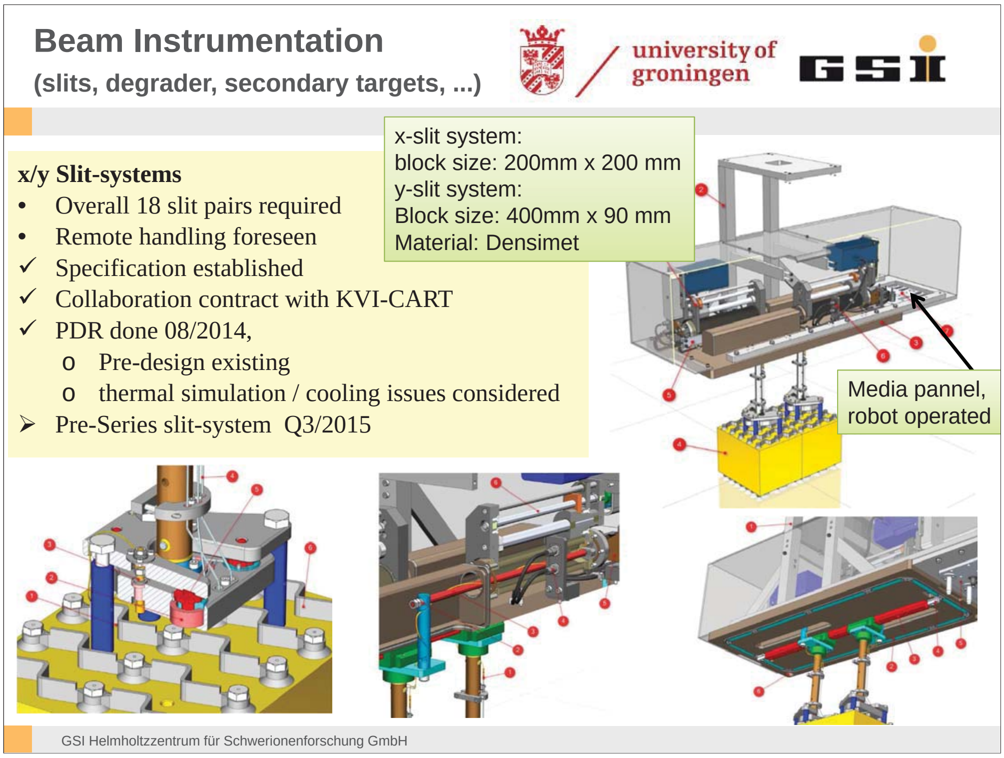
Si

MUSIC

Diamond s detector

GEM TPC prototype

N-XYTER readout



Beam Instrumentation

(slits, degrader, secondary targets, ...)

x-slit system:
block size: 200mm x 200 mm
y-slit system:
Block size: 400mm x 90 mm
Material: Densimet

x/y Slit-systems

- Overall 18 slit pairs required
- Remote handling foreseen
- ✓ Specification established
- ✓ Collaboration contract with KVI-CART
- ✓ PDR done 08/2014,
  - o Pre-design existing
  - o thermal simulation / cooling issues considered
- ➢ Pre-Series slit-system Q3/2015

Media pannel, robot operated

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Stepping stones towards the facility

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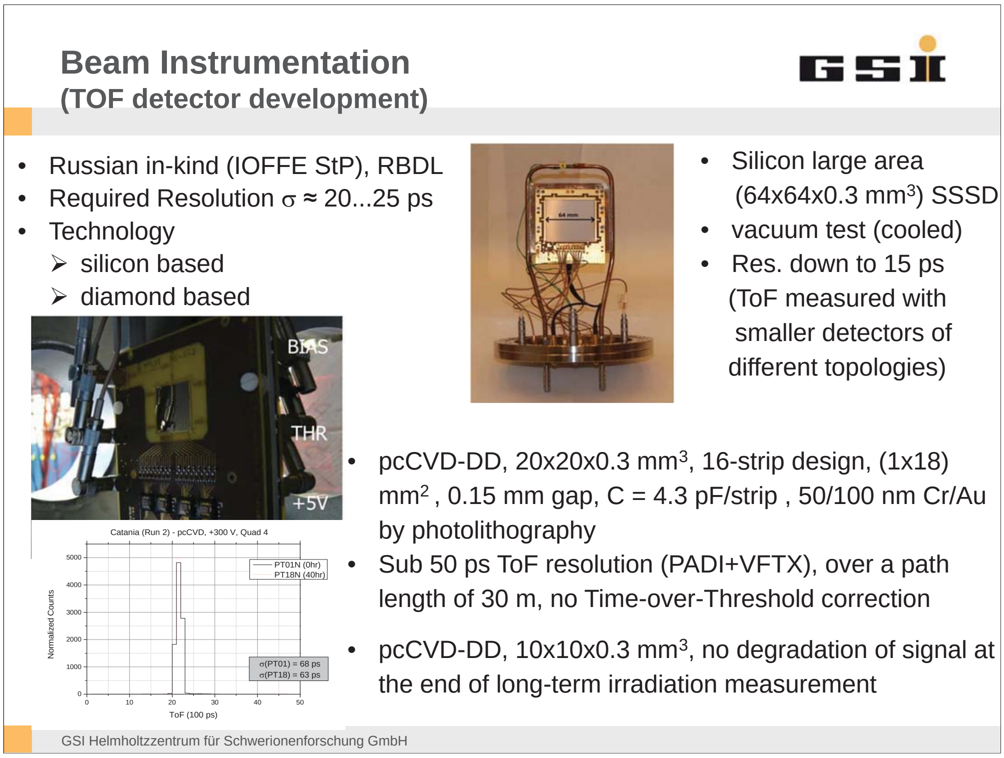

Beam Instrumentation
(TOF detector development)

- Russian in-kind (IOFFE StP), RBDL
- Required Resolution σ ≈ 20...25 ps
- Technology
  - silicon based
  - diamond based

- Silicon large area (64x64x0.3 mm^3) SSSD
- vacuum test (cooled)
- Res. down to 15 ps (ToF measured with smaller detectors of different topologies)

- pcCVD-DD, 20x20x0.3 mm^3, 16-strip design, (1x18) mm^2 , 0.15 mm gap, C = 4.3 pF/strip , 50/100 nm Cr/Au by photolithography
- Sub 50 ps ToF resolution (PADI+VFTX), over a path length of 30 m, no Time-over-Threshold correction

- pcCVD-DD, 10x10x0.3 mm^3, no degradation of signal at the end of long-term irradiation measurement

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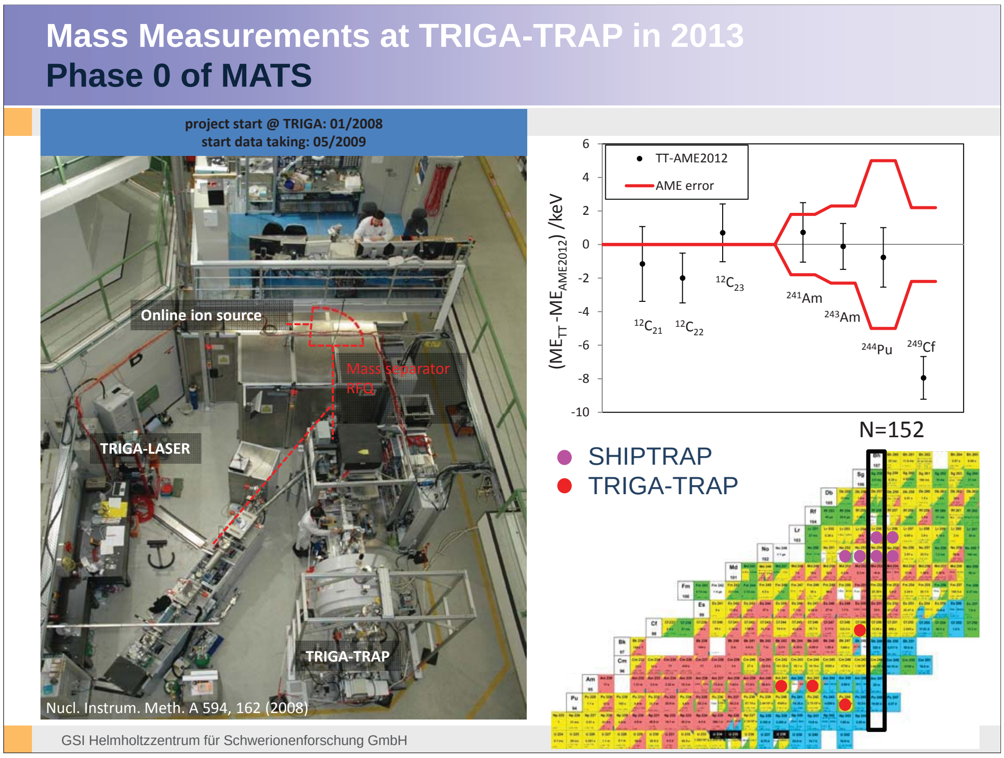

Mass Measurements at TRIGA-TRAP in 2013
Phase 0 of MATS

project start @ TRIGA: 01/2008
start data taking: 05/2009

Nucl. Instrum. Meth. A 594, 162 (2008)

- ● SHIPTRAP
- ● TRIGA-TRAP

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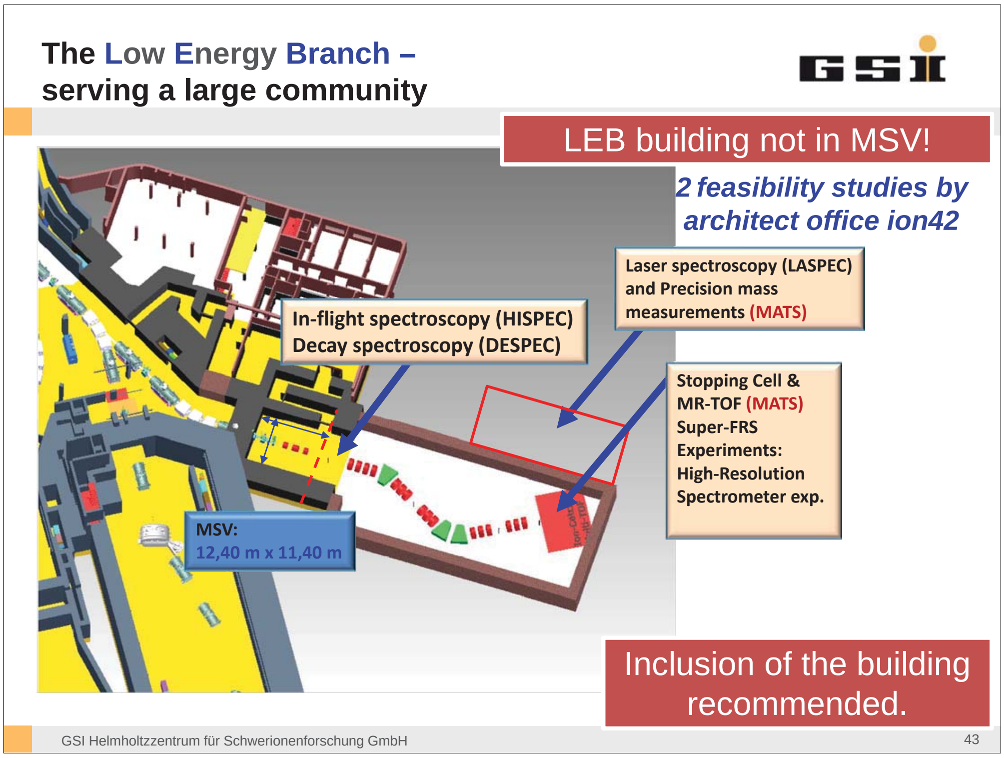

The Low Energy Branch – serving a large community

LEB building not in MSV!

2 feasibility studies by architect office ion42

Laser spectroscopy (LASPEC) and Precision mass measurements (MATS)

In-flight spectroscopy (HISPEC)
Decay spectroscopy (DESPEC)

Stopping Cell & MR-TOF (MATS)
Super-FRS Experiments:
High-Resolution Spectrometer exp.

MSV:
12,40 m x 11,40 m

Inclusion of the building recommended.

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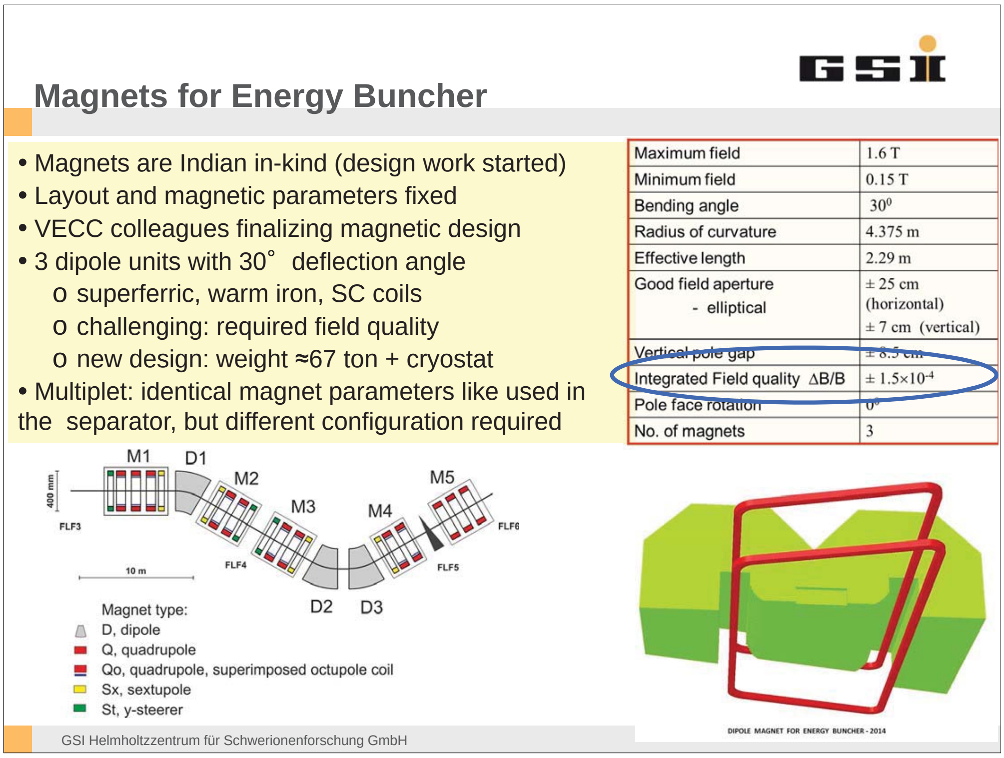

Magnets for Energy Buncher

- Magnets are Indian in-kind (design work started)
- Layout and magnetic parameters fixed
- VECC colleagues finalizing magnetic design
- 3 dipole units with 30° deflection angle
  - o superferric, warm iron, SC coils
  - o challenging: required field quality
  - o new design: weight ≈67 ton + cryostat
- Multiplet: identical magnet parameters like used in the separator, but different configuration required

Maximum field	1.6 T
Minimum field	0.15 T
Bending angle	30^0
Radius of curvature	4.375 m
Effective length	2.29 m
Good field aperture - elliptical	± 25 cm (horizontal) ± 7 cm (vertical)
Vertical pole gap	± 8.5 cm
Integrated Field quality ΔB/B	$\pm 1.5\times10^{-4}$
Pole face rotation	0°
No. of magnets	3

Magnet type:
- D, dipole
- 🟥 Q, quadrupole
- Qo, quadrupole, superimposed octupole coil
- 🟨 Sx, sextupole
- 🟩 St, y-steerer

DIPOLE MAGNET FOR ENERGY BUNCHER - 2014

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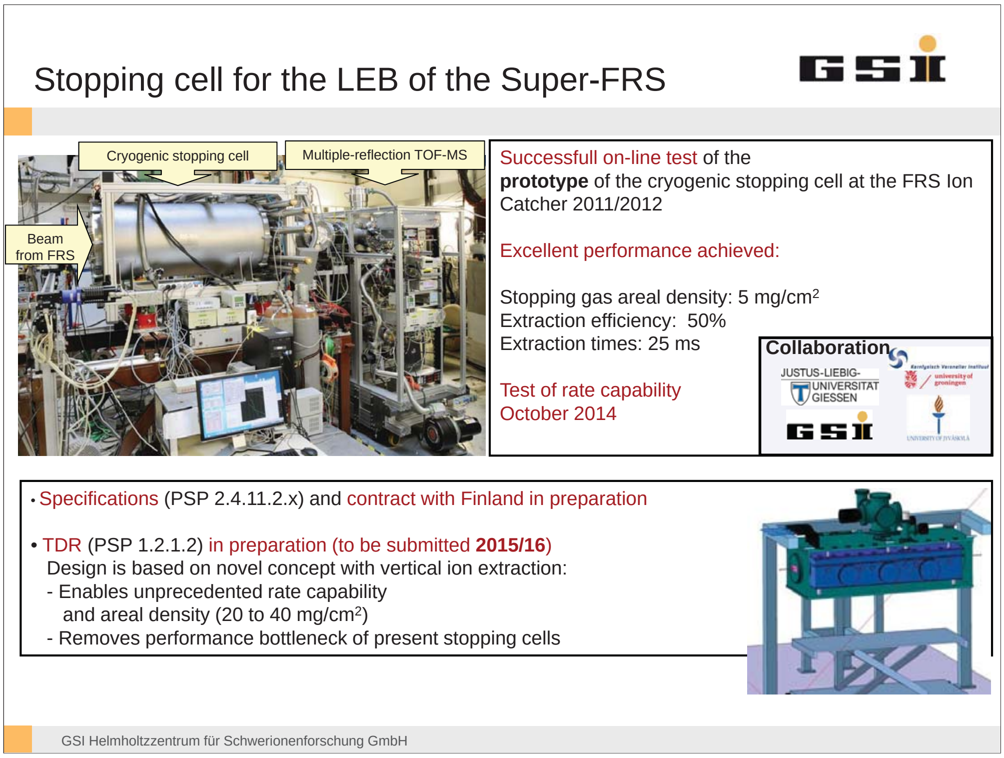


Stopping cell for the LEB of the Super-FRS

Successfull on-line test of the **prototype** of the cryogenic stopping cell at the FRS Ion Catcher 2011/2012

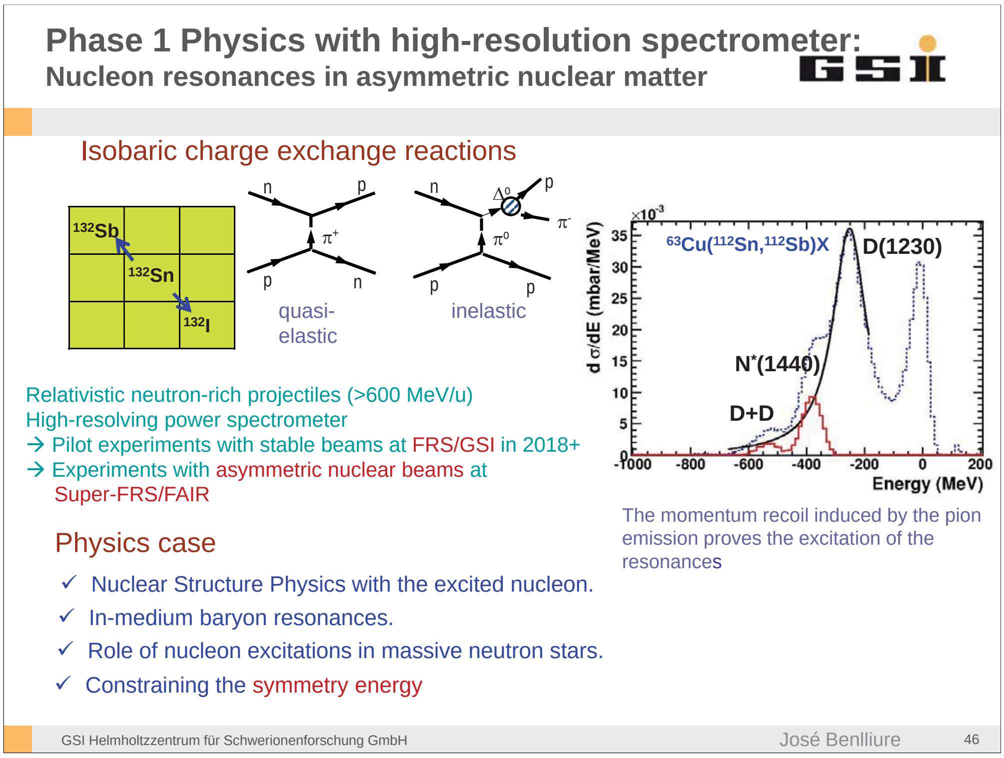
Excellent performance achieved:

Stopping gas areal density: 5 mg/cm^2
Extraction efficiency: 50%
Extraction times: 25 ms

Test of rate capability
October 2014

Collaboration

- Specifications (PSP 2.4.11.2.x) and contract with Finland in preparation
- TDR (PSP 1.2.1.2) in preparation (to be submitted **2015/16**)
  Design is based on novel concept with vertical ion extraction:
  - Enables unprecedented rate capability
    and areal density (20 to 40 mg/cm^2)
  - Removes performance bottleneck of present stopping cells



Phase 1 Physics with high-resolution spectrometer:

Nucleon resonances in asymmetric nuclear matter

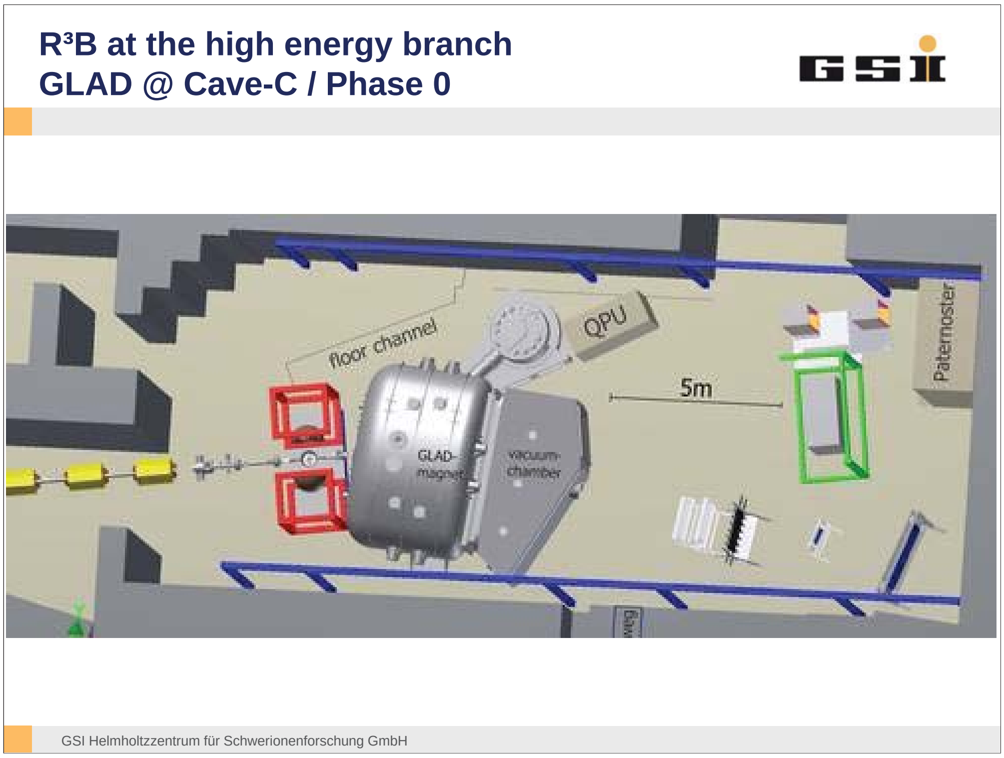
Isobaric charge exchange reactions

Relativistic neutron-rich projectiles (>600 MeV/u)
High-resolving power spectrometer
→ Pilot experiments with stable beams at FRS/GSI in 2018+
→ Experiments with asymmetric nuclear beams at Super-FRS/FAIR

The momentum recoil induced by the pion emission proves the excitation of the resonances

Physics case

- ✓ Nuclear Structure Physics with the excited nucleon.
- ✓ In-medium baryon resonances.
- ✓ Role of nucleon excitations in massive neutron stars.
- ✓ Constraining the symmetry energy



R^3B at the high energy branch
GLAD @ Cave-C / Phase 0

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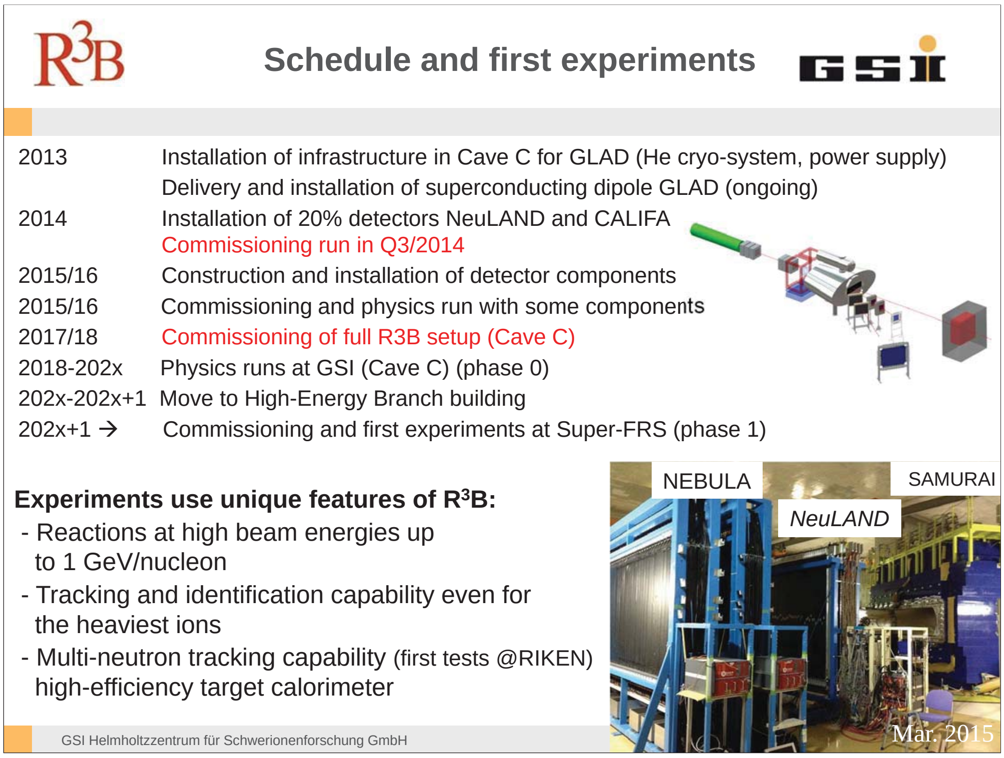

Schedule and first experiments

2013	Installation of infrastructure in Cave C for GLAD (He cryo-system, power supply) Delivery and installation of superconducting dipole GLAD (ongoing)
2014	Installation of 20% detectors NeuLAND and CALIFA Commissioning run in Q3/2014
2015/16	Construction and installation of detector components
2015/16	Commissioning and physics run with some components
2017/18	Commissioning of full R3B setup (Cave C)
2018-202x	Physics runs at GSI (Cave C) (phase 0)
202x-202x+1	Move to High-Energy Branch building
202x+1 →	Commissioning and first experiments at Super-FRS (phase 1)

Experiments use unique features of R^3B:

- Reactions at high beam energies up to 1 GeV/nucleon
- Tracking and identification capability even for the heaviest ions
- Multi-neutron tracking capability (first tests @RIKEN) high-efficiency target calorimeter

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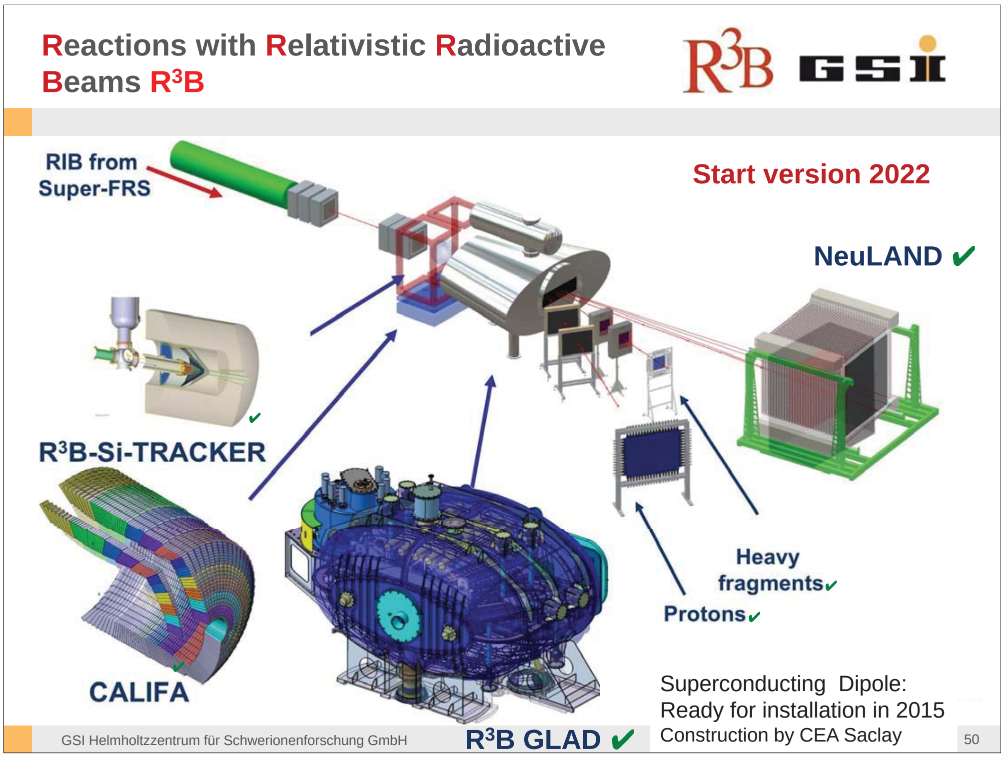
2013/14

… GLAD Infrastructure @ GSI



Reactions with Relativistic Radioactive Beams R³B

Start version 2022

Superconducting Dipole:
Ready for installation in 2015
Construction by CEA Saclay

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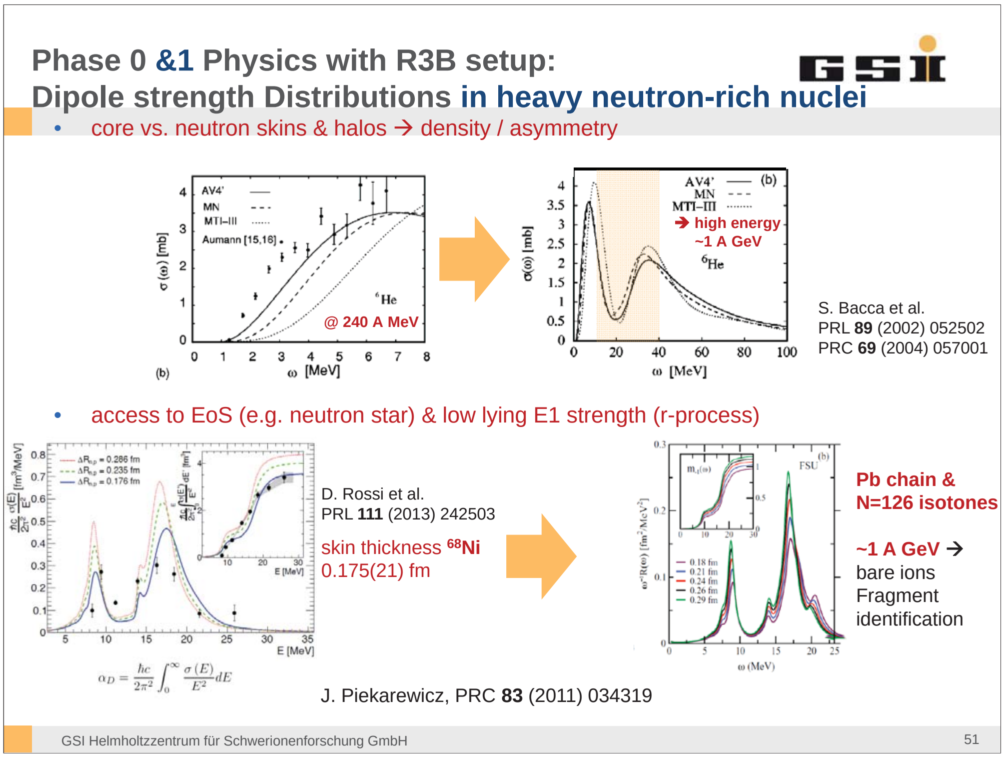

Phase 0 &1 Physics with R3B setup: Dipole strength Distributions in heavy neutron-rich nuclei

- core vs. neutron skins & halos → density / asymmetry

S. Bacca et al.
PRL **89** (2002) 052502
PRC **69** (2004) 057001

- access to EoS (e.g. neutron star) & low lying E1 strength (r-process)

$$\alpha_D = \frac{\hbar c}{2\pi^2}\int_0^\infty \frac{\sigma(E)}{E^2}dE$$

D. Rossi et al.
PRL **111** (2013) 242503

skin thickness ^{68}**Ni**
0.175(21) fm

Pb chain &
N=126 isotones

~1 A GeV →
bare ions
Fragment
identification

J. Piekarewicz, PRC **83** (2011) 034319

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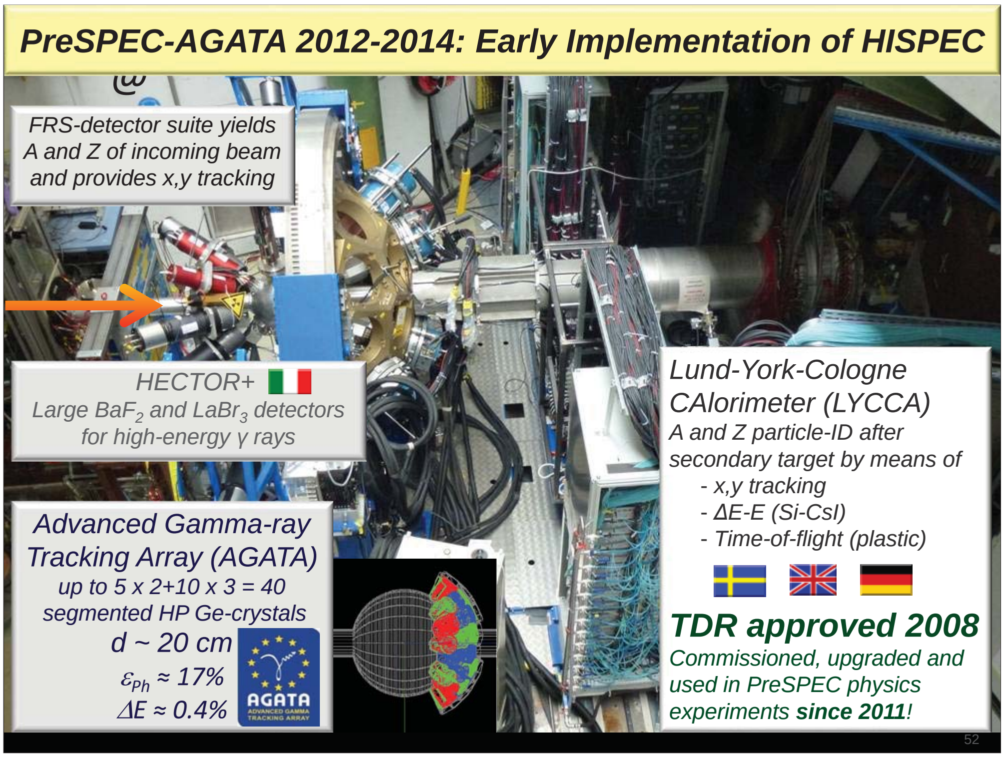

PreSPEC-AGATA 2012-2014: Early Implementation of HISPEC

FRS-detector suite yields A and Z of incoming beam and provides x,y tracking

HECTOR+
Large BaF$_2$ and LaBr$_3$ detectors for high-energy γ rays

Advanced Gamma-ray Tracking Array (AGATA)
up to 5 x 2+10 x 3 = 40 segmented HP Ge-crystals
d ~ 20 cm
ε_{Ph} ≈ 17%
ΔE ≈ 0.4%

Lund-York-Cologne CAlorimeter (LYCCA)
A and Z particle-ID after secondary target by means of
- *x,y tracking*
- *ΔE-E (Si-CsI)*
- *Time-of-flight (plastic)*

TDR approved 2008
*Commissioned, upgraded and used in PreSPEC physics experiments **since 2011**!*

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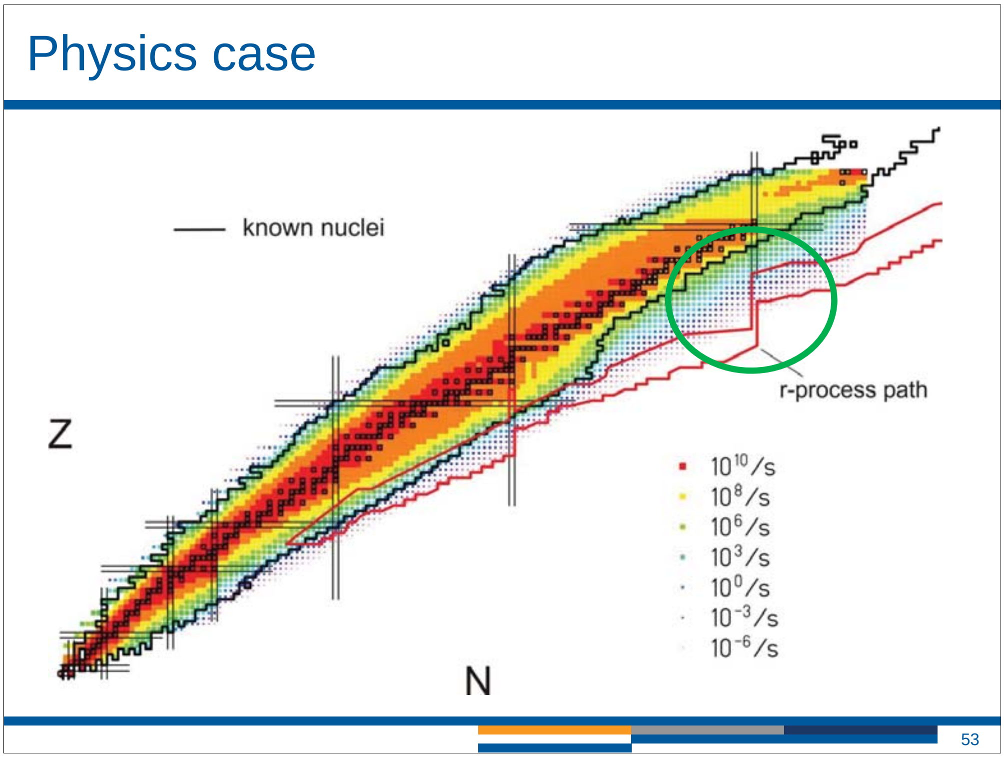
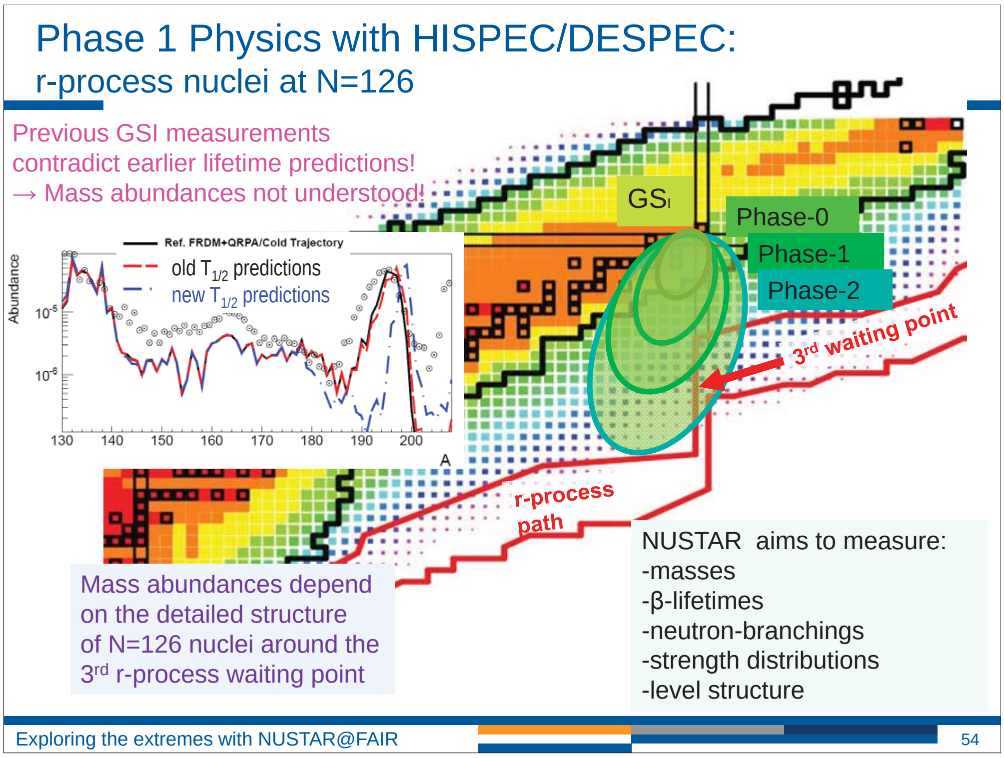


Physics case

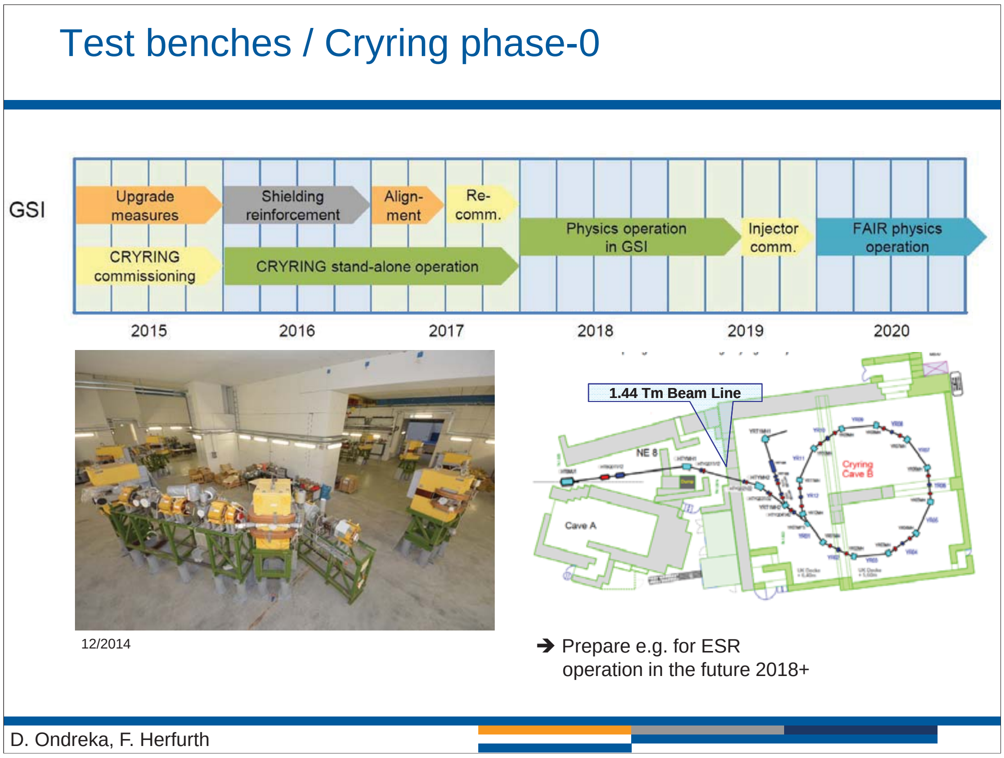


Phase 1 Physics with HISPEC/DESPEC:
r-process nuclei at N=126

Previous GSI measurements contradict earlier lifetime predictions!
→ Mass abundances not understood!

Mass abundances depend on the detailed structure of N=126 nuclei around the 3^{rd} r-process waiting point

NUSTAR aims to measure:
-masses
-β-lifetimes
-neutron-branchings
-strength distributions
-level structure

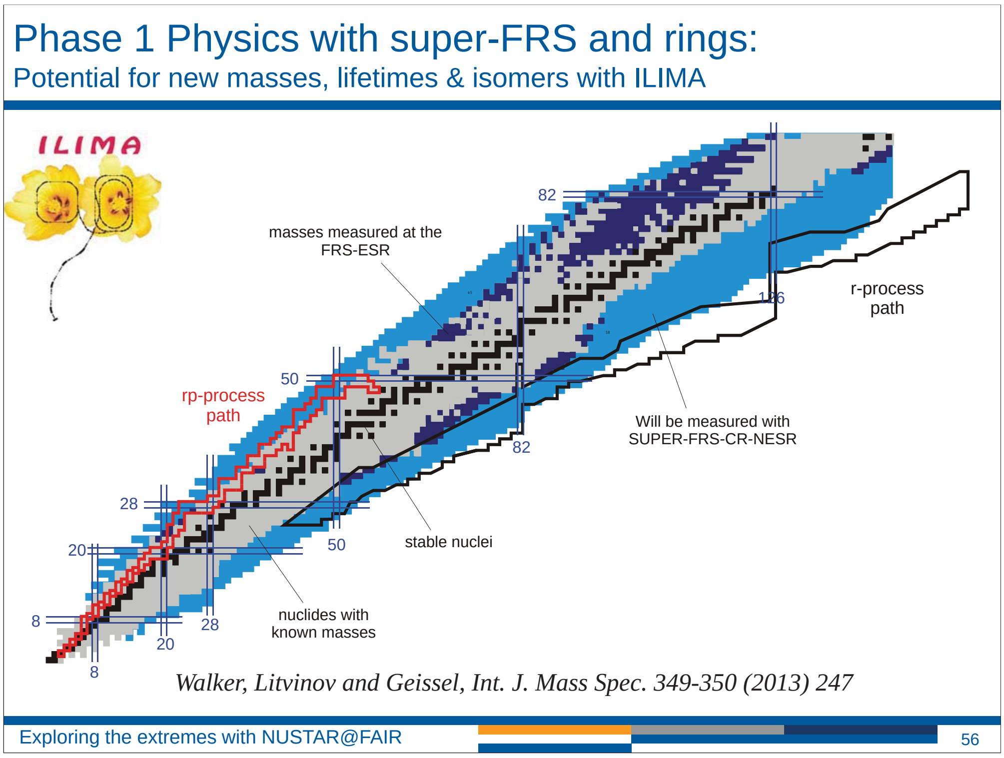


Test benches / Cryring phase-0

12/2014

➔ Prepare e.g. for ESR operation in the future 2018+

D. Ondreka, F. Herfurth

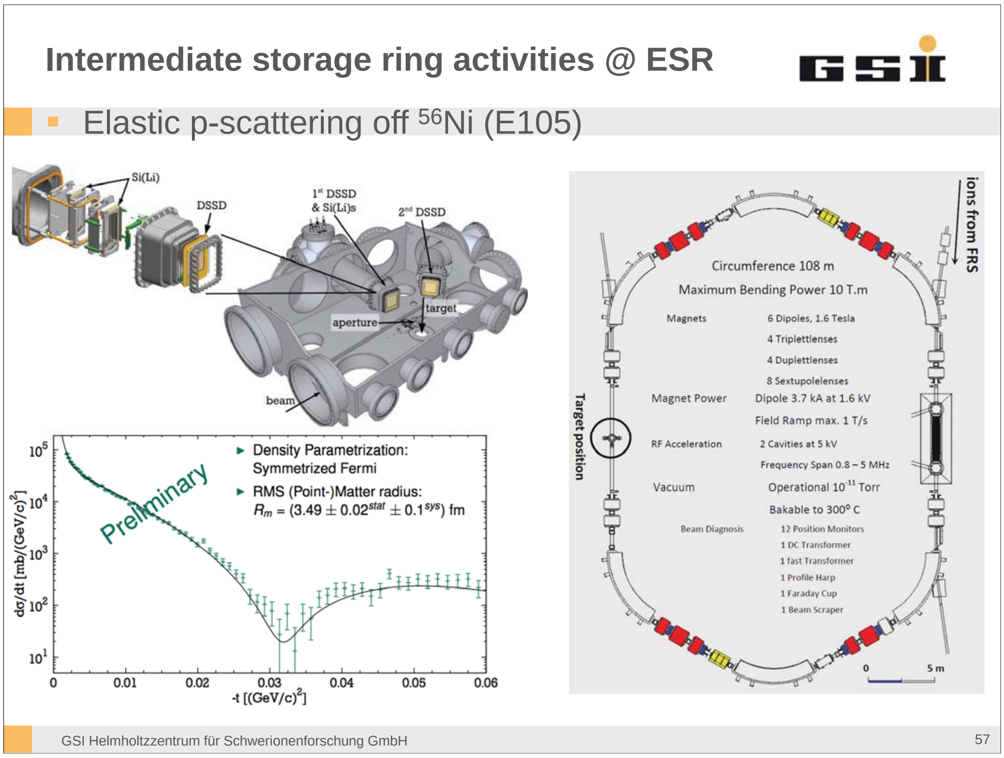


Phase 1 Physics with super-FRS and rings:
Potential for new masses, lifetimes & isomers with ILIMA

Walker, Litvinov and Geissel, Int. J. Mass Spec. 349-350 (2013) 247

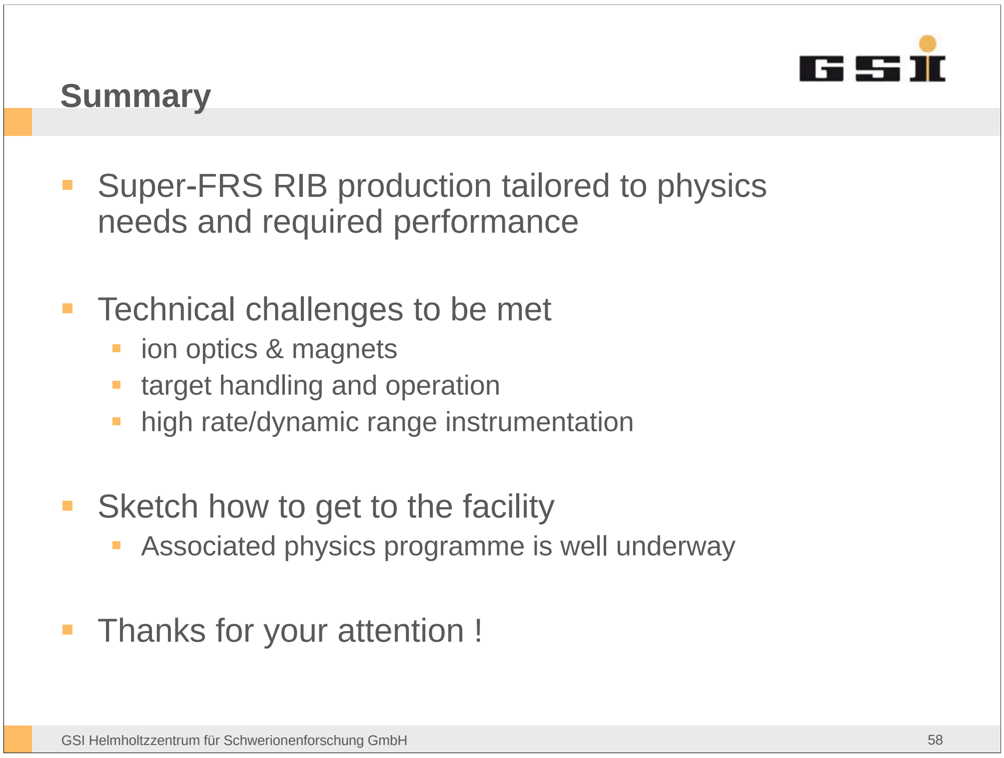
Exploring the extremes with NUSTAR@FAIR

56



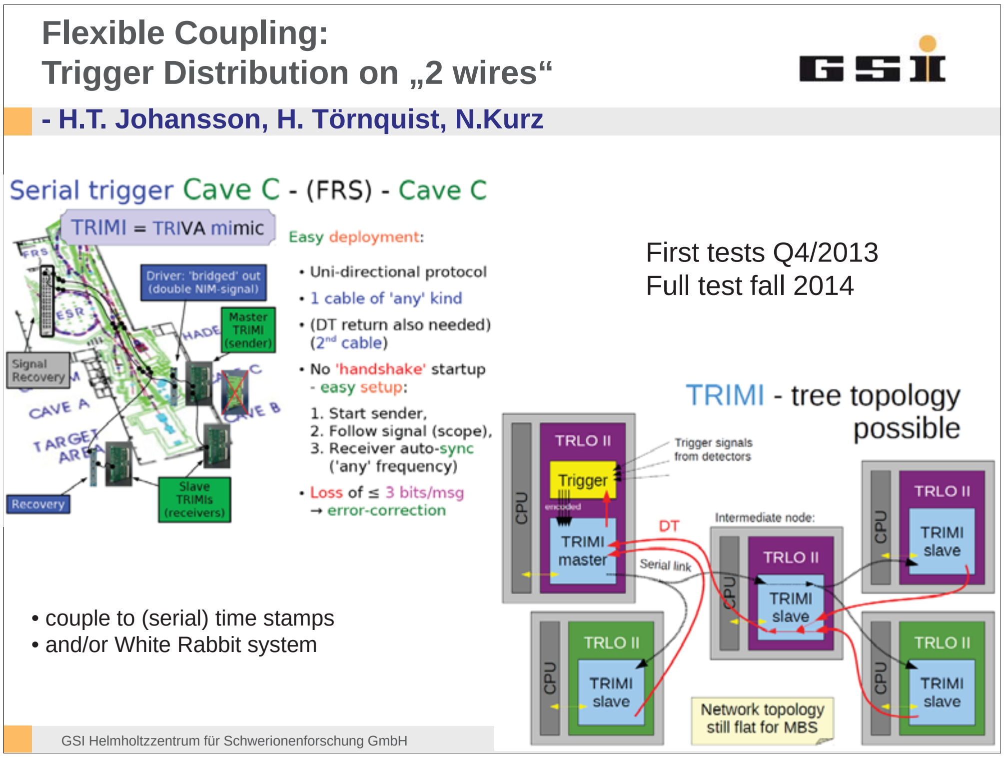
Intermediate storage ring activities @ ESR

- Elastic p-scattering off ^{56}Ni (E105)



Summary

- Super-FRS RIB production tailored to physics needs and required performance
- Technical challenges to be met
  - ion optics & magnets
  - target handling and operation
  - high rate/dynamic range instrumentation
- Sketch how to get to the facility
  - Associated physics programme is well underway
- Thanks for your attention !



Flexible Coupling: Trigger Distribution on „2 wires“

- H.T. Johansson, H. Törnquist, N.Kurz

Serial trigger Cave C - (FRS) - Cave C

TRIMI = TRIVA mimic

Easy deployment:

- Uni-directional protocol
- 1 cable of 'any' kind
- (DT return also needed) (2nd cable)
- No 'handshake' startup - easy setup:
  1. Start sender,
  2. Follow signal (scope),
  3. Receiver auto-sync ('any' frequency)
- Loss of ≤ 3 bits/msg → error-correction

First tests Q4/2013
Full test fall 2014

TRIMI - tree topology possible

- couple to (serial) time stamps
- and/or White Rabbit system

Network topology still flat for MBS

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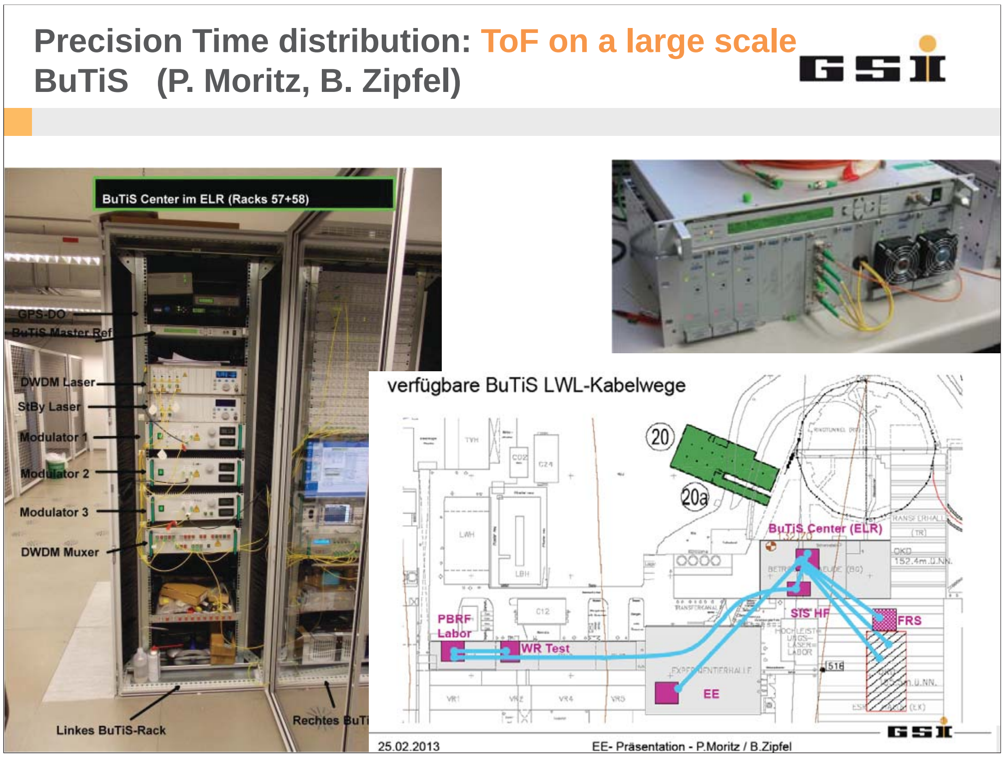


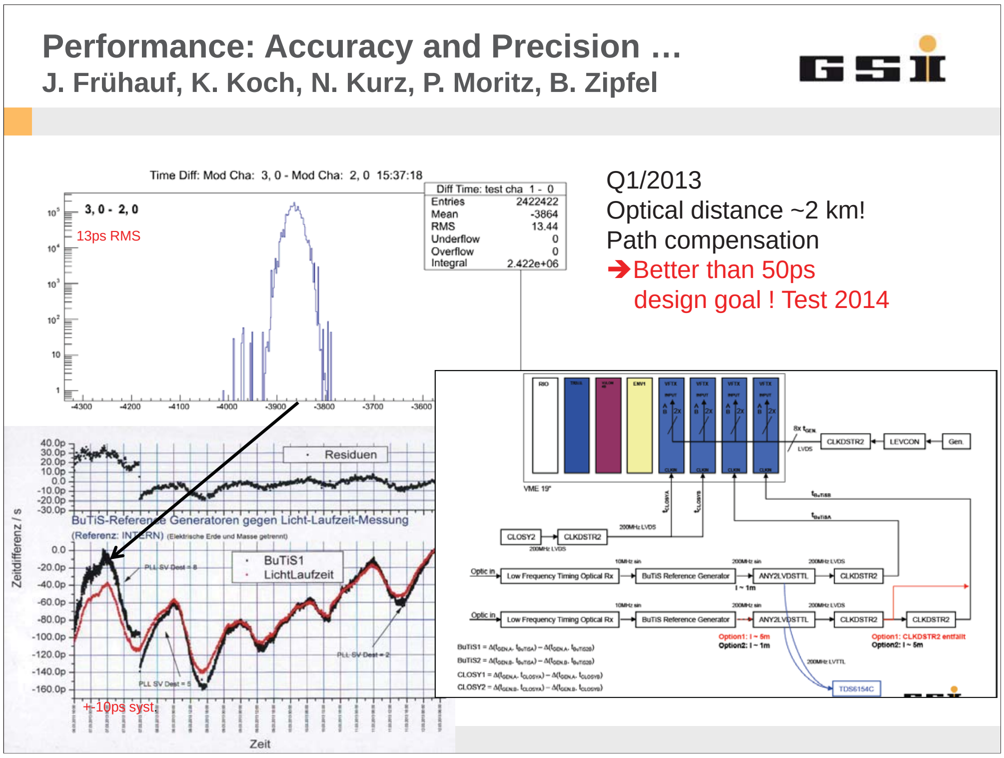
Precision Time distribution: ToF on a large scale

BuTiS (P. Moritz, B. Zipfel)

BuTiS Center im ELR (Racks 57+58)

verfügbare BuTiS LWL-Kabelwege

25.02.2013 EE- Präsentation - P.Moritz / B.Zipfel



Performance: Accuracy and Precision …

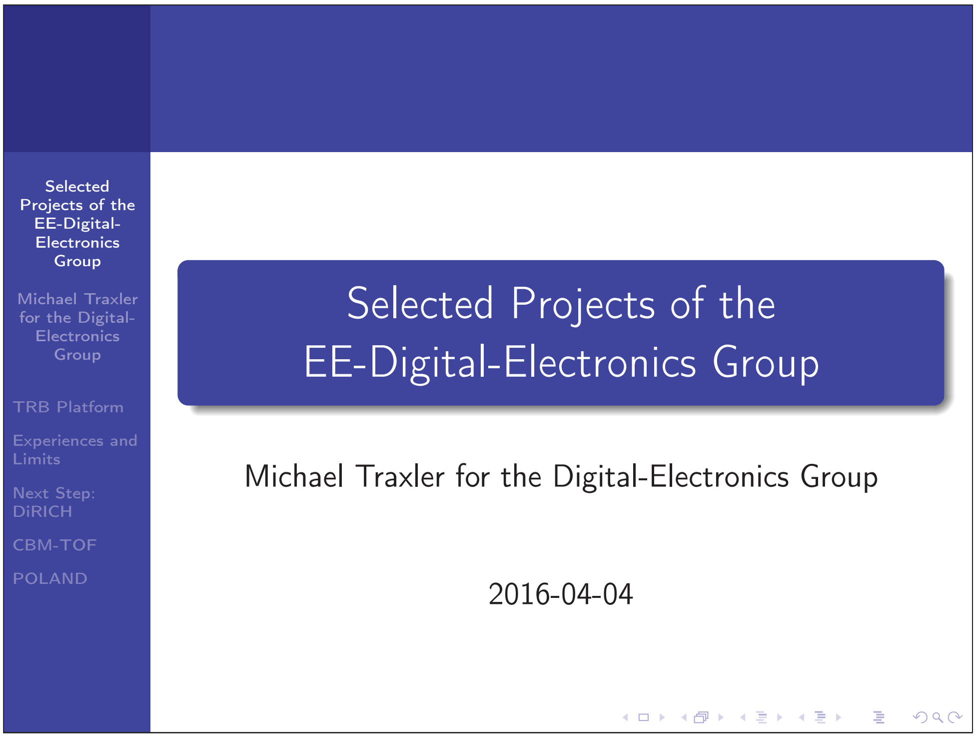
J. Frühauf, K. Koch, N. Kurz, P. Moritz, B. Zipfel

Q1/2013

Optical distance ~2 km!

Path compensation

➔Better than 50ps design goal ! Test 2014



Selected Projects of the EE-Digital-Electronics Group

Michael Traxler for the Digital-Electronics Group

TRB Platform

Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND

Selected Projects of the EE-Digital-Electronics Group

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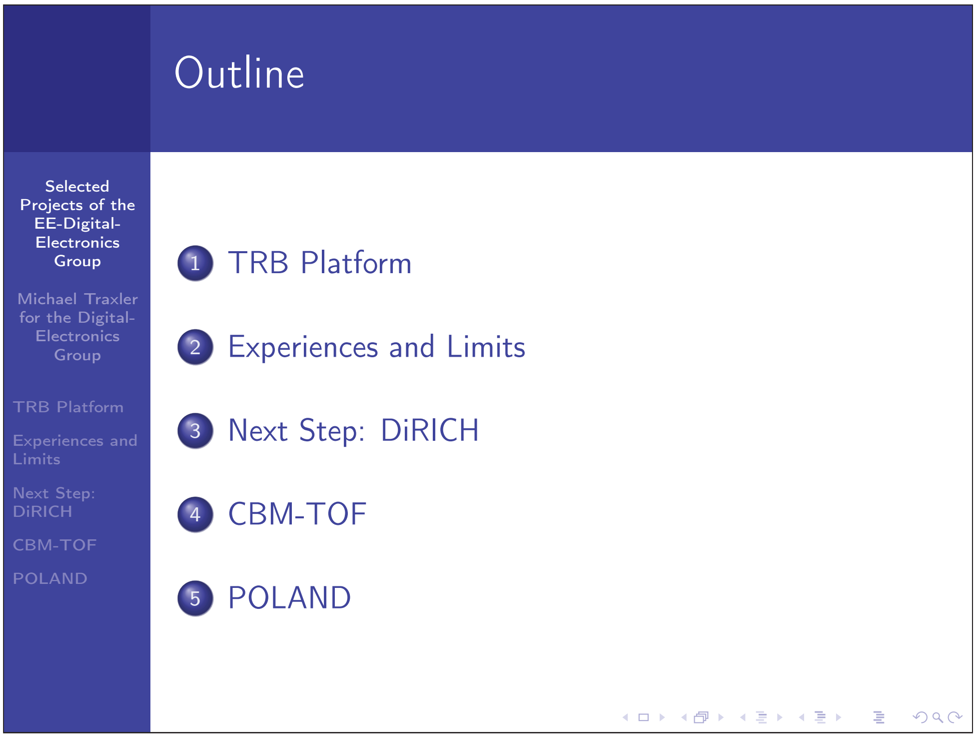
2016-04-04



Outline

Selected Projects of the EE-Digital-Electronics Group

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TRB Platform

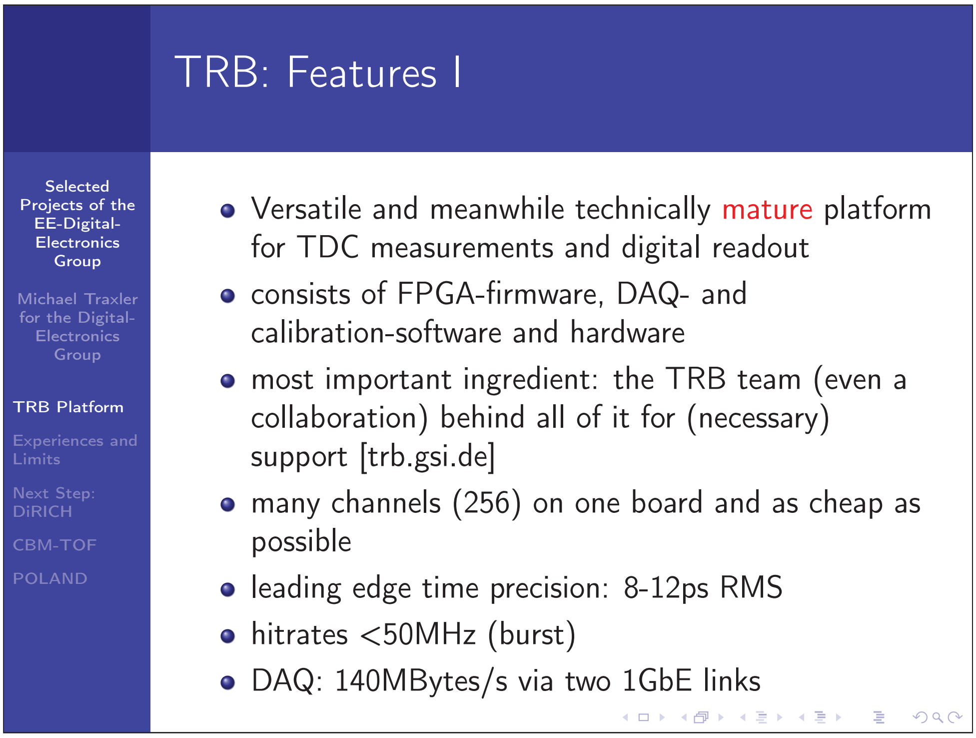
Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND

1. TRB Platform
2. Experiences and Limits
3. Next Step: DiRICH
4. CBM-TOF
5. POLAND



TRB: Features I

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TRB Platform

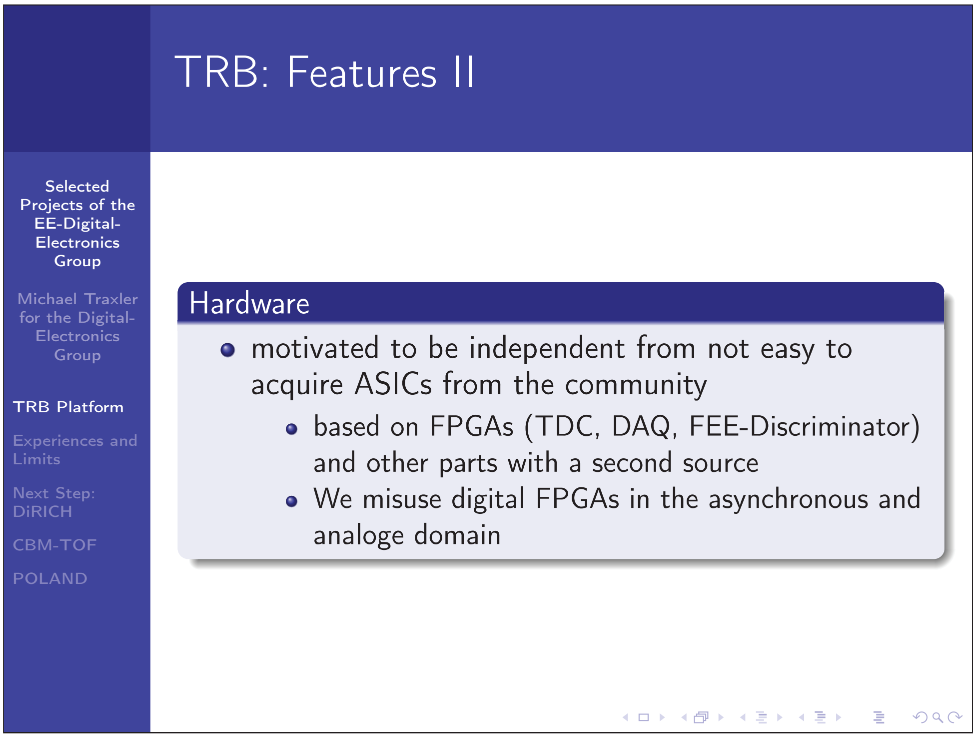
Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND

- Versatile and meanwhile technically mature platform for TDC measurements and digital readout
- consists of FPGA-firmware, DAQ- and calibration-software and hardware
- most important ingredient: the TRB team (even a collaboration) behind all of it for (necessary) support [trb.gsi.de]
- many channels (256) on one board and as cheap as possible
- leading edge time precision: 8-12ps RMS
- hitrates <50MHz (burst)
- DAQ: 140MBytes/s via two 1GbE links



TRB: Features II

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TRB Platform

Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND

Hardware

- motivated to be independent from not easy to acquire ASICs from the community
  - based on FPGAs (TDC, DAQ, FEE-Discriminator) and other parts with a second source
  - We misuse digital FPGAs in the asynchronous and analoge domain

TRB Platform: TRB3 module

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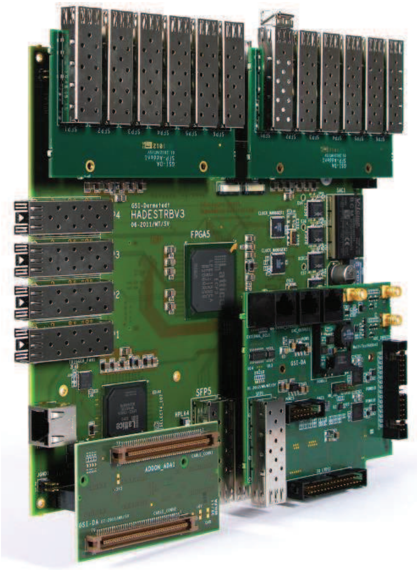
TRB Platform
Experiences and Limits
Next Step: DiRICH
CBM-TOF
POLAND



- 4 times high speed 208-pin connector for various AddONs
- Addons available:
  - 6 port Hubs
  - NIM/ECL-Input
  - ADC
  - standard 100mil pins
  - Padiwa-Adapter
  - etc.

TRB Platform: Some Hardware II

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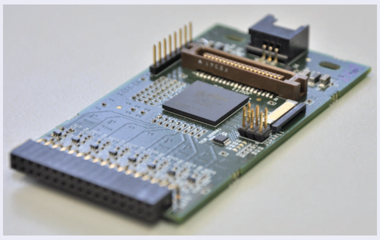
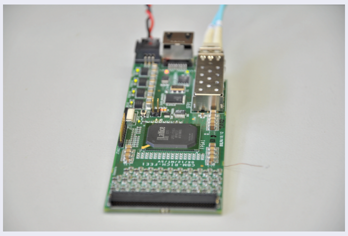
TRB Platform
Experiences and Limits
Next Step: DiRICH
CBM-TOF
POLAND

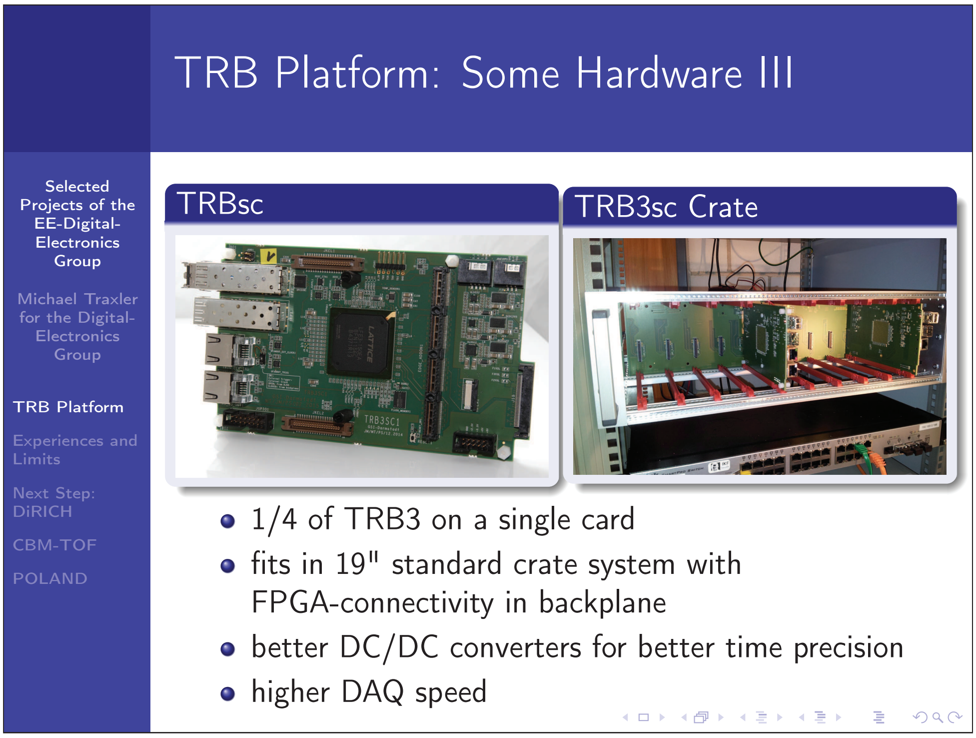
Padiwa



CBM-TOF-FEE



- Padiwa used for CBM-RICH-beamtests
- Padiwa used for Panda-Barrel-DIRC-beamtests Summer 2015 at CERN
- CBM-TOF-FEE used for CBM-TOF beamtime November 2015 at CERN



TRB Platform: Some Hardware III

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TRB Platform

Experiences and Limits

Next Step: DiRICH

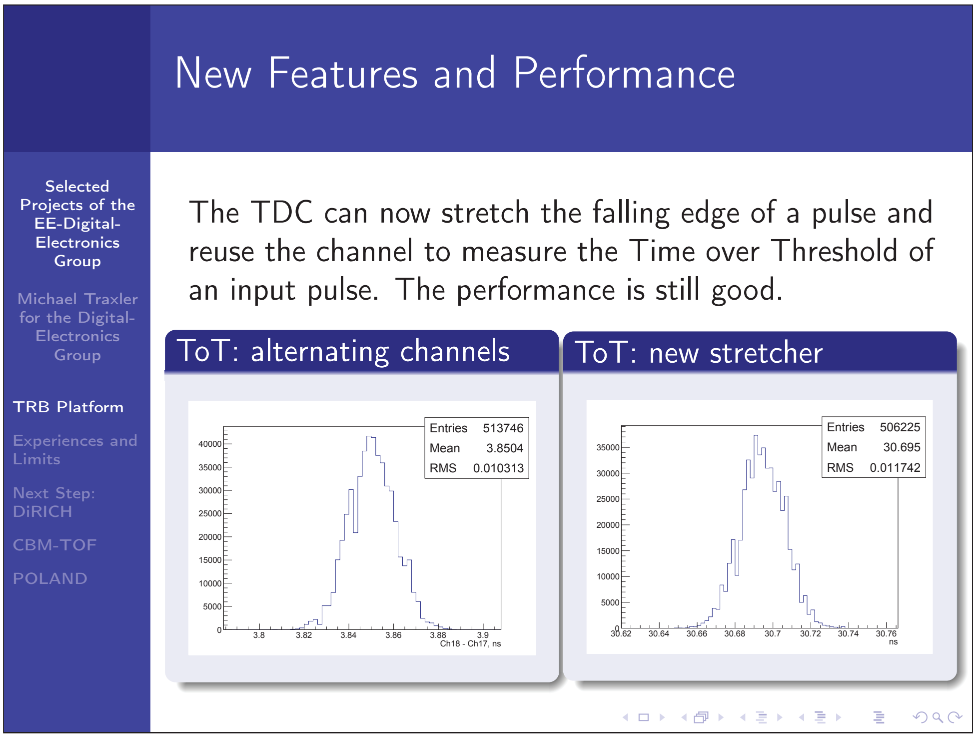
CBM-TOF

POLAND

TRBsc

TRB3sc Crate

- 1/4 of TRB3 on a single card
- fits in 19" standard crate system with FPGA-connectivity in backplane
- better DC/DC converters for better time precision
- higher DAQ speed



New Features and Performance

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TRB Platform

Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND

The TDC can now stretch the falling edge of a pulse and reuse the channel to measure the Time over Threshold of an input pulse. The performance is still good.

ToT: alternating channels

ToT: new stretcher

Feature and Problem at the same Time

Selected Projects of the EE-Digital-Electronics Group

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TRB Platform

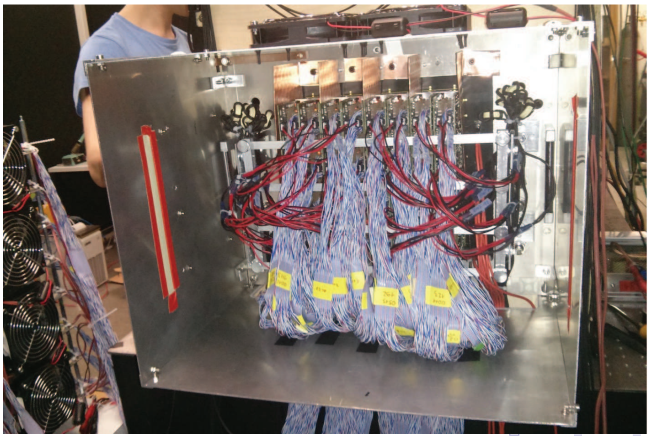
Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND

- The TRB platform is a stable and flexible
- Flexibility has a (high) price
  - Cables everywhere!



Effects of Cables

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TRB Platform

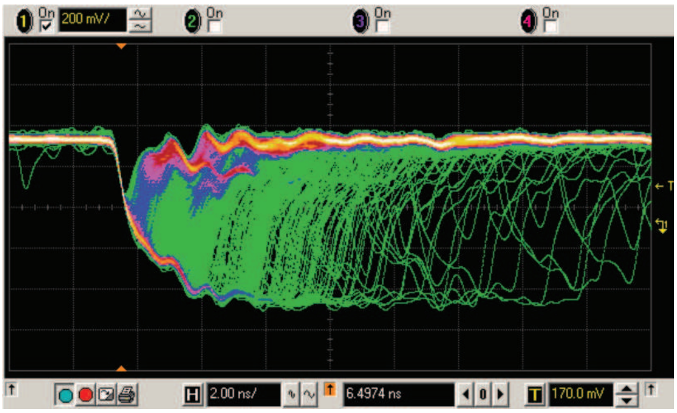
Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND

- Mechanically this becomes a problem (densities)
  - Barrel-DIRC-beam-time clearly showed that this is more than a inconvenience
- Long cables damp the signal away

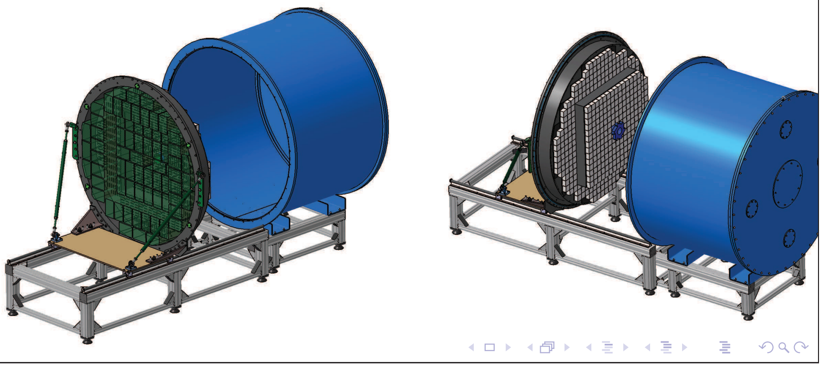


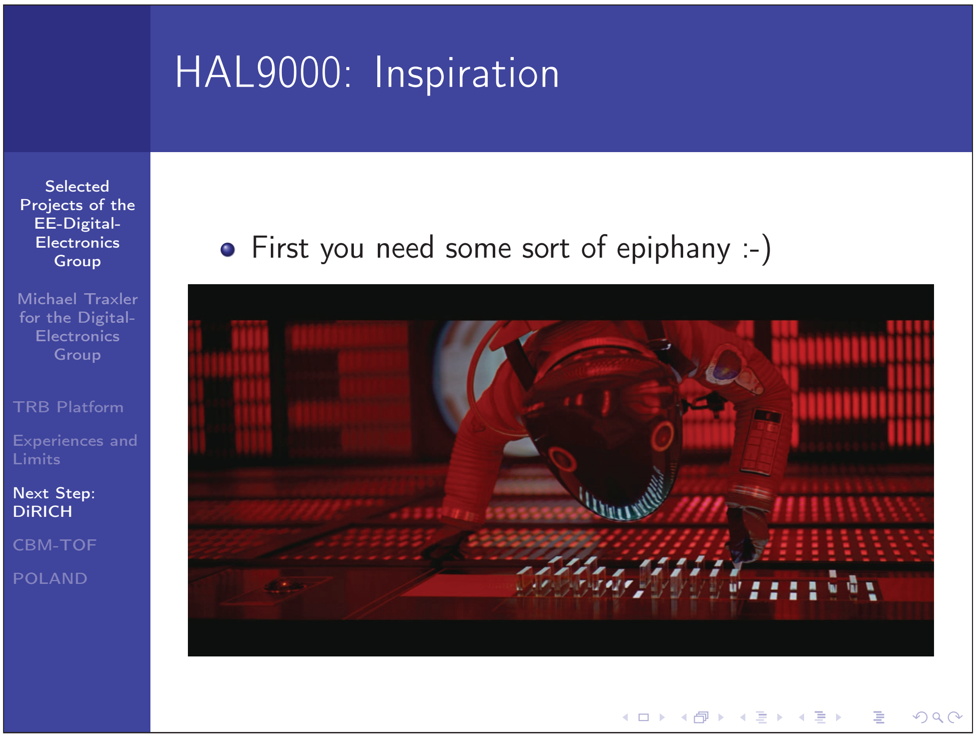
Solution

- Rethink mechanics/cables/connectors
- Improve on noise to the input of the FEE
- Improve on noise immunity of FEE
- Work together in a larger team!
- Some pressure!

RICH700 Project in HADES: to be finished in 2016

- Exchange of the HADES RICH CsI photocathode with 420 MA-PMTs
- New FEE + Readout has to be developed
- Cooperation of CBM + HADES experiments





HAL9000: Inspiration

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TRB Platform

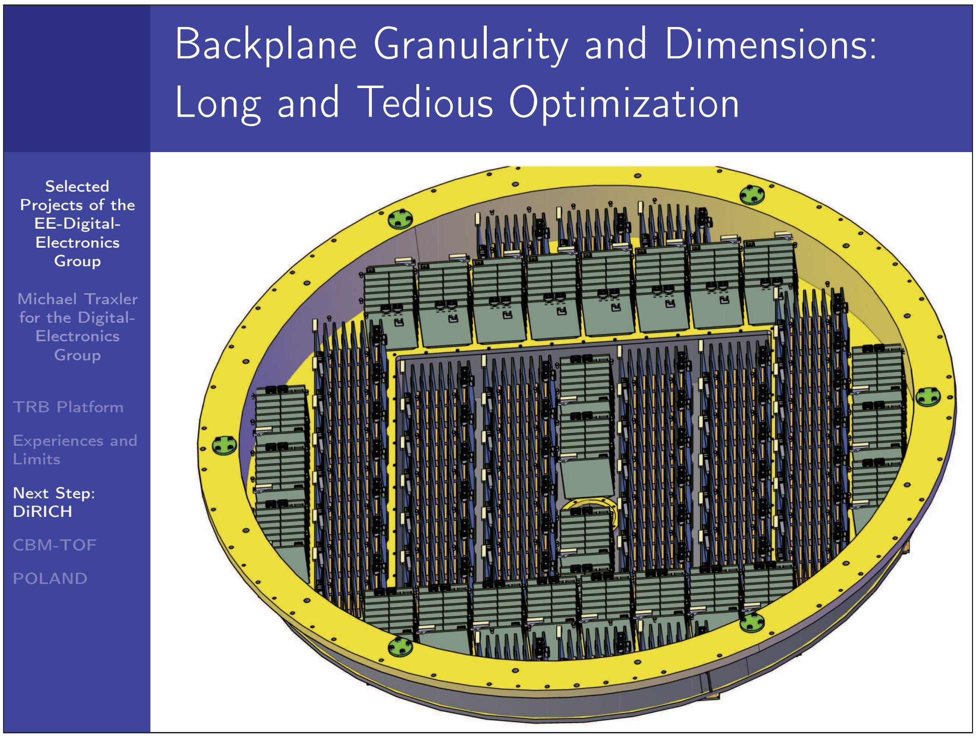
Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND

- First you need some sort of epiphany :-)



Backplane Granularity and Dimensions: Long and Tedious Optimization

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TRB Platform

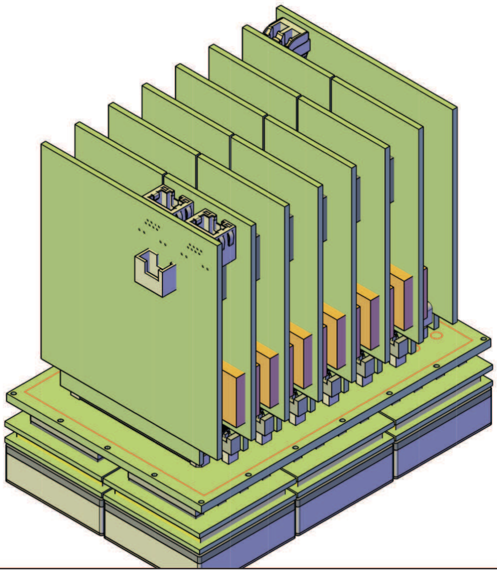
Experiences and Limits

Next Step: DiRICH

CBM-TOF

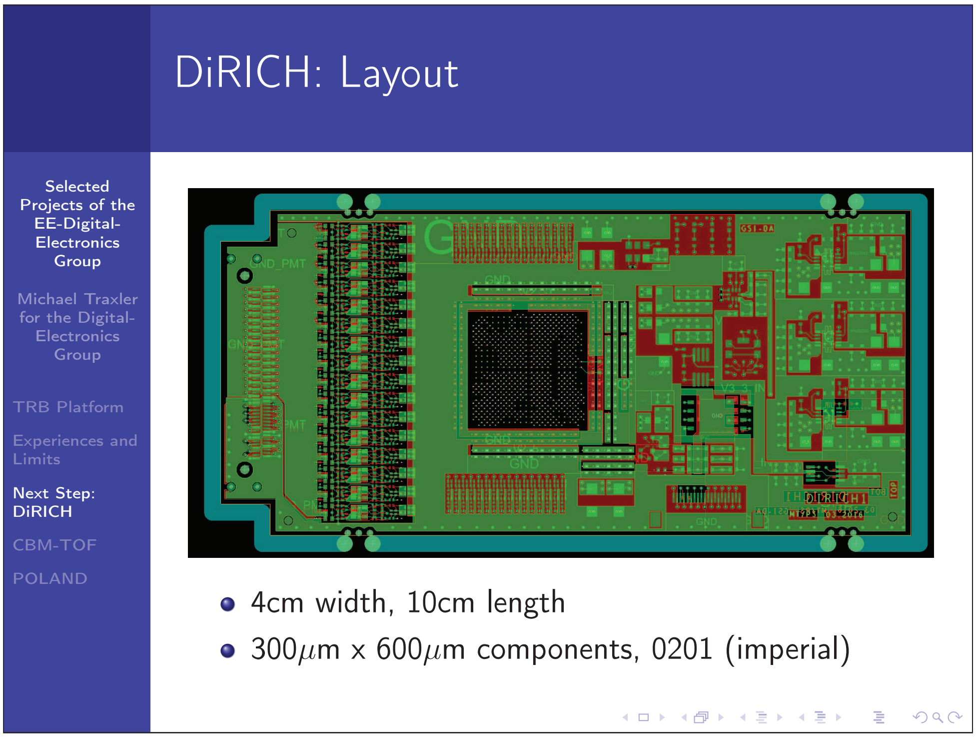
POLAND

DiRCH concept



DiRICH Requirements and Design Consequences

- FEE module for 32 channels
- Amplification, Discrimination, TDC + DAQ
- no cables
- analog input signals and digital output signals (serial transmission) over the same connector
- low power consumption
- only possible with newest FPGAs (price/performance) and most dense connectors
- galvanically isolate PMT from FEE with transformers
  - reduces issues with HV-Power-Supply GND connection



DiRICH: Layout

Selected Projects of the EE-Digital-Electronics Group

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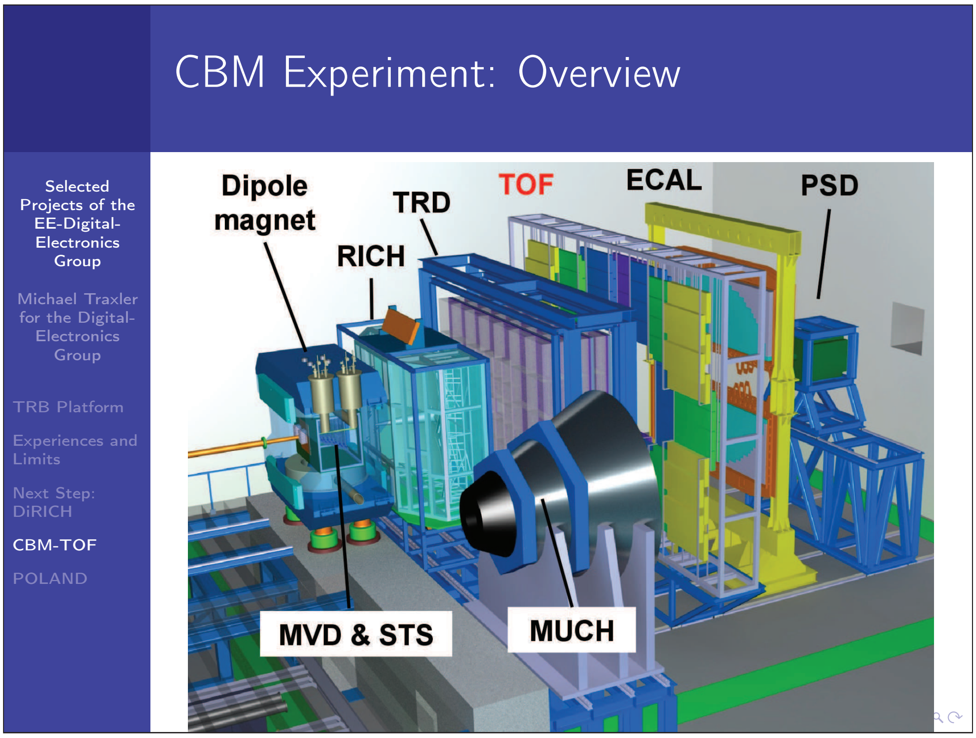
- TRB Platform
- Experiences and Limits
- Next Step: DiRICH
- CBM-TOF
- POLAND

- 4cm width, 10cm length
- 300μm x 600μm components, 0201 (imperial)



CBM Experiment: Overview

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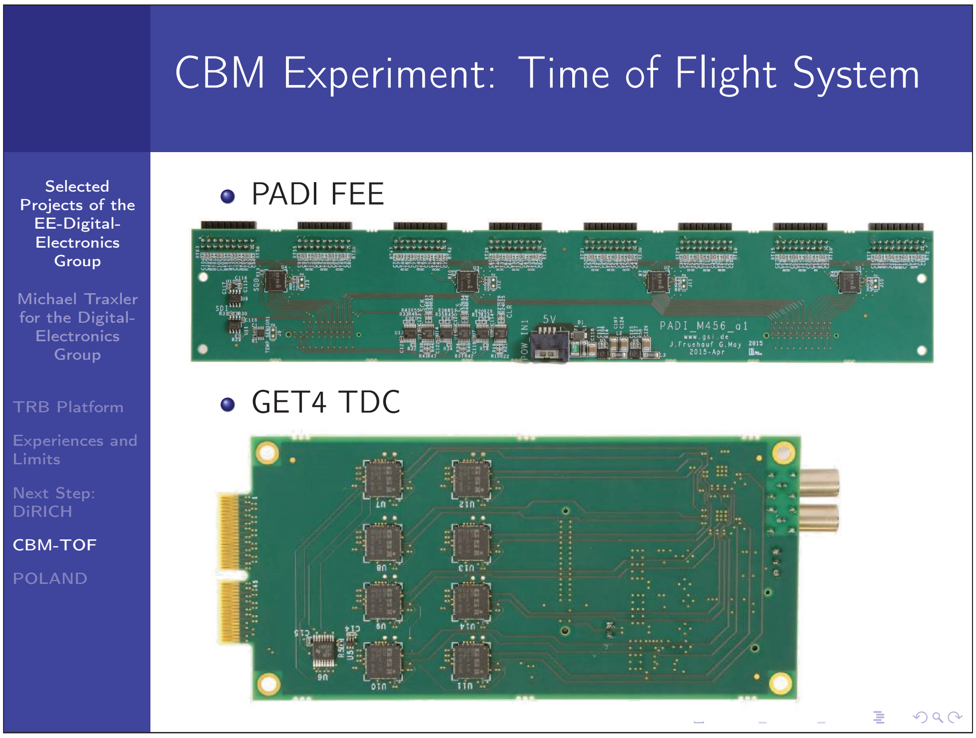
- TRB Platform
- Experiences and Limits
- Next Step: DiRICH
- CBM-TOF
- POLAND



CBM Experiment: Time of Flight System

- PADI FEE
- GET4 TDC

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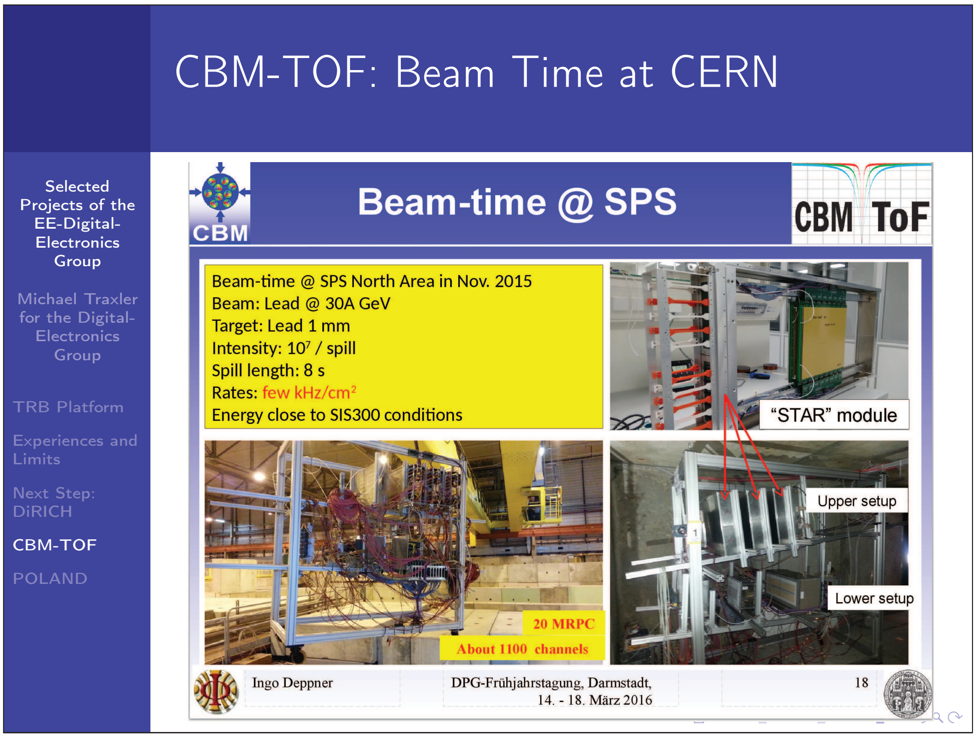
TRB Platform

Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND



CBM-TOF: Beam Time at CERN

Beam-time @ SPS

CBM ToF

Beam-time @ SPS North Area in Nov. 2015
Beam: Lead @ 30A GeV
Target: Lead 1 mm
Intensity: 10^7 / spill
Spill length: 8 s
Rates: few kHz/cm^2
Energy close to SIS300 conditions

Ingo Deppner DPG-Frühjahrstagung, Darmstadt, 14. - 18. März 2016 18

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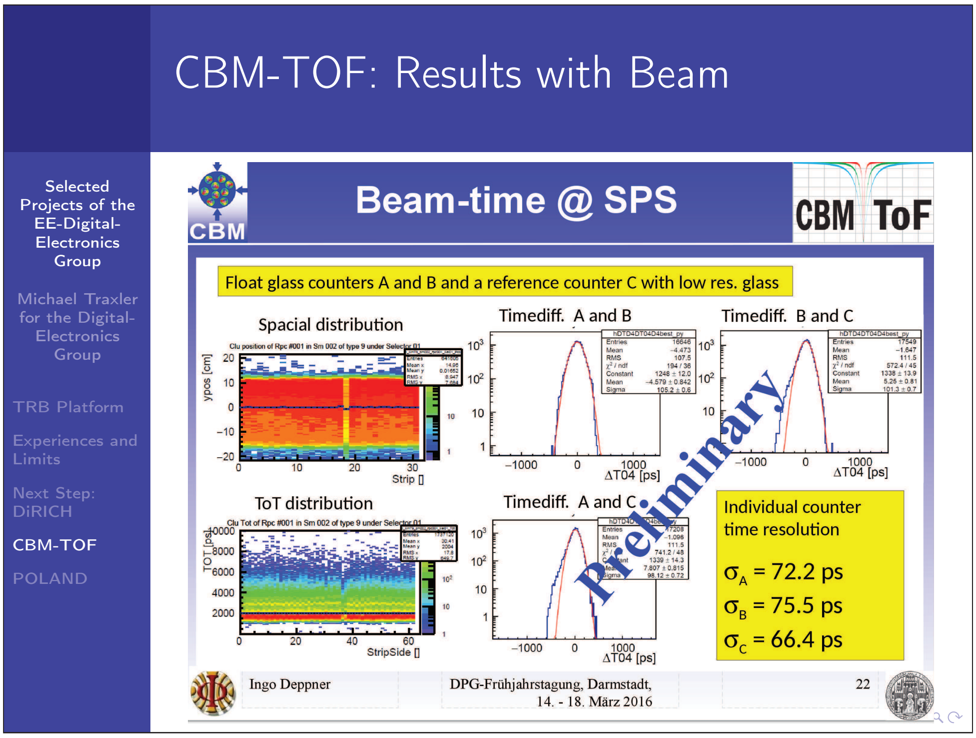
TRB Platform

Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND



CBM-TOF: Results with Beam

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TRB Platform

Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND

Beam-time @ SPS

Float glass counters A and B and a reference counter C with low res. glass

Individual counter time resolution

σ_A = 72.2 ps

σ_B = 75.5 ps

σ_C = 66.4 ps

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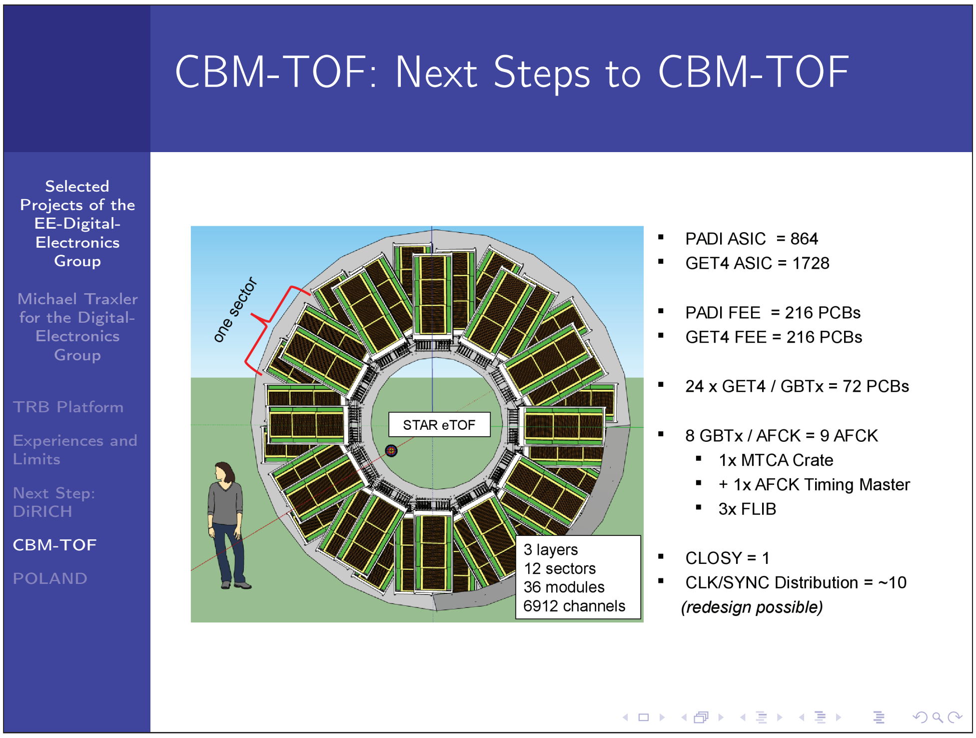

CBM-TOF: Next Steps to CBM-TOF

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TRB Platform

Experiences and Limits

Next Step: DiRICH

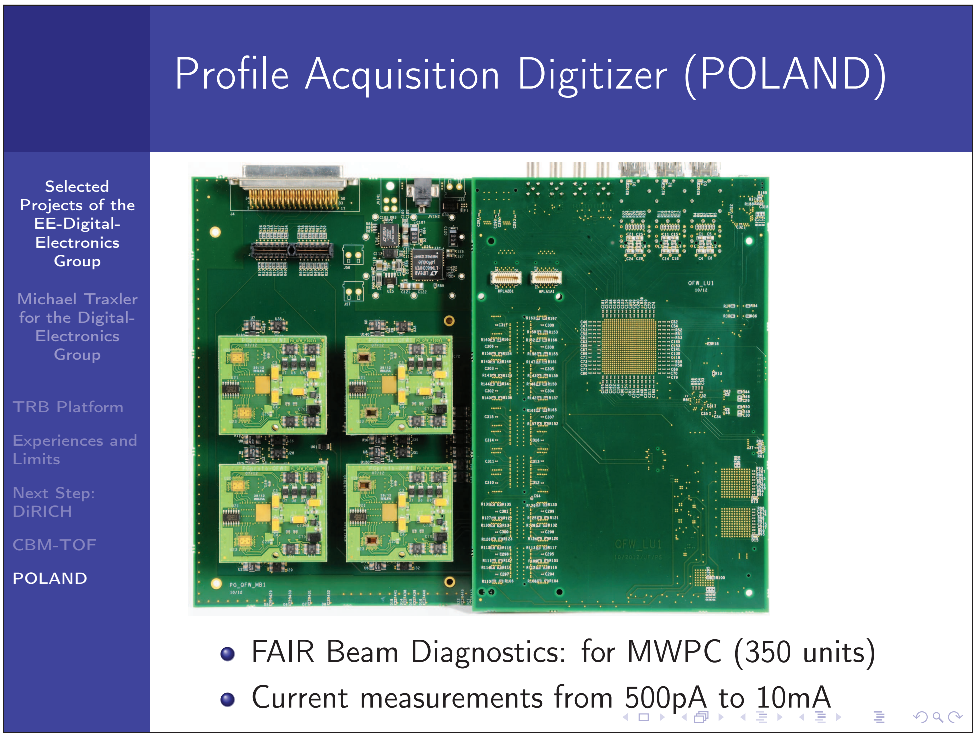
CBM-TOF

POLAND

3 layers
12 sectors
36 modules
6912 channels

- PADI ASIC = 864
- GET4 ASIC = 1728
- PADI FEE = 216 PCBs
- GET4 FEE = 216 PCBs
- 24 x GET4 / GBTx = 72 PCBs
- 8 GBTx / AFCK = 9 AFCK
  - 1x MTCA Crate
  - + 1x AFCK Timing Master
  - 3x FLIB
- CLOSY = 1
- CLK/SYNC Distribution = ~10

(redesign possible)



Profile Acquisition Digitizer (POLAND)

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TRB Platform

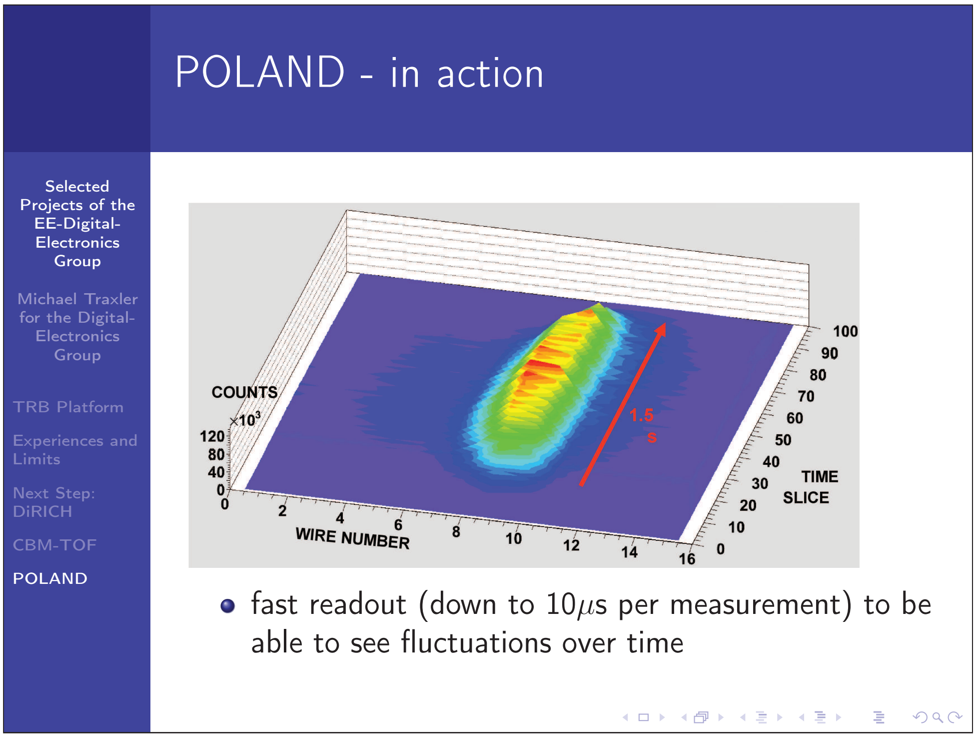
Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND

- FAIR Beam Diagnostics: for MWPC (350 units)
- Current measurements from 500pA to 10mA



POLAND - in action

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TRB Platform

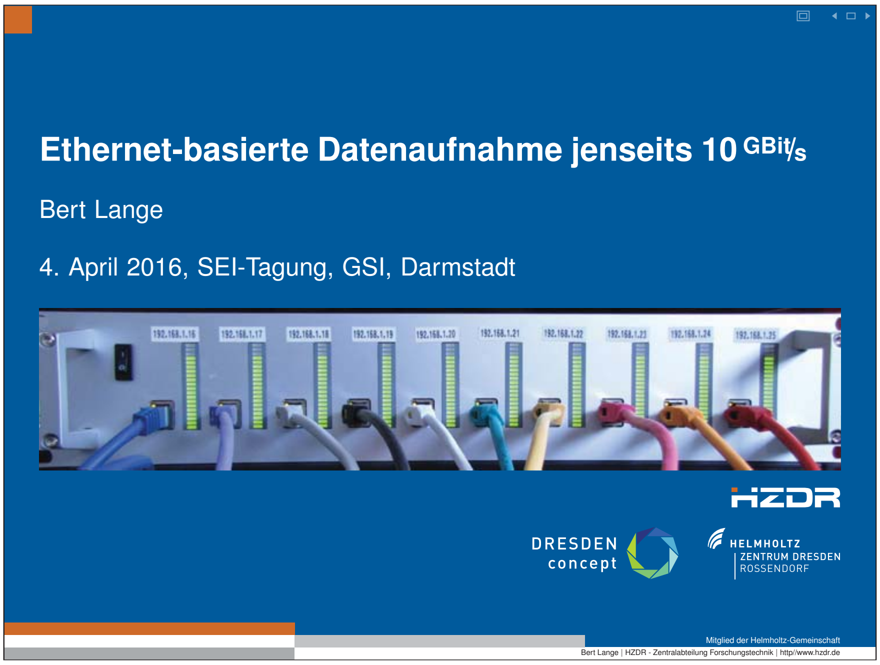
Experiences and Limits

Next Step: DiRICH

CBM-TOF

POLAND

- fast readout (down to 10μs per measurement) to be able to see fluctuations over time



Ethernet-basierte Datenaufnahme jenseits 10 GBit/s

Bert Lange

4. April 2016, SEI-Tagung, GSI, Darmstadt

Mitglied der Helmholtz-Gemeinschaft

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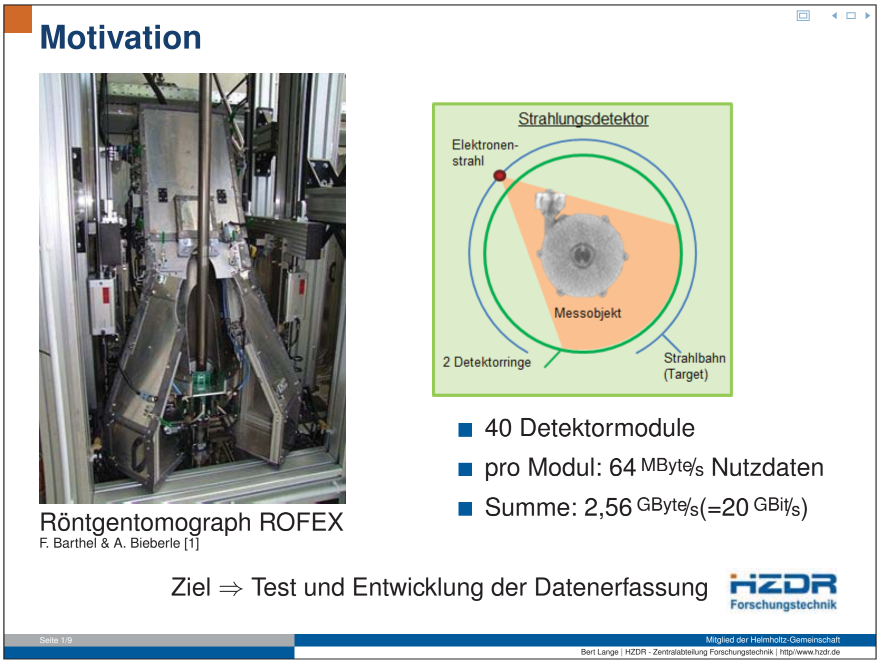

Motivation

- 40 Detektormodule
- pro Modul: 64 MByte/s Nutzdaten
- Summe: 2,56 GByte/s(=20 GBit/s)

Röntgentomograph ROFEX
F. Barthel & A. Bieberle [1]

Ziel ⇒ Test und Entwicklung der Datenerfassung

Seite 1/9

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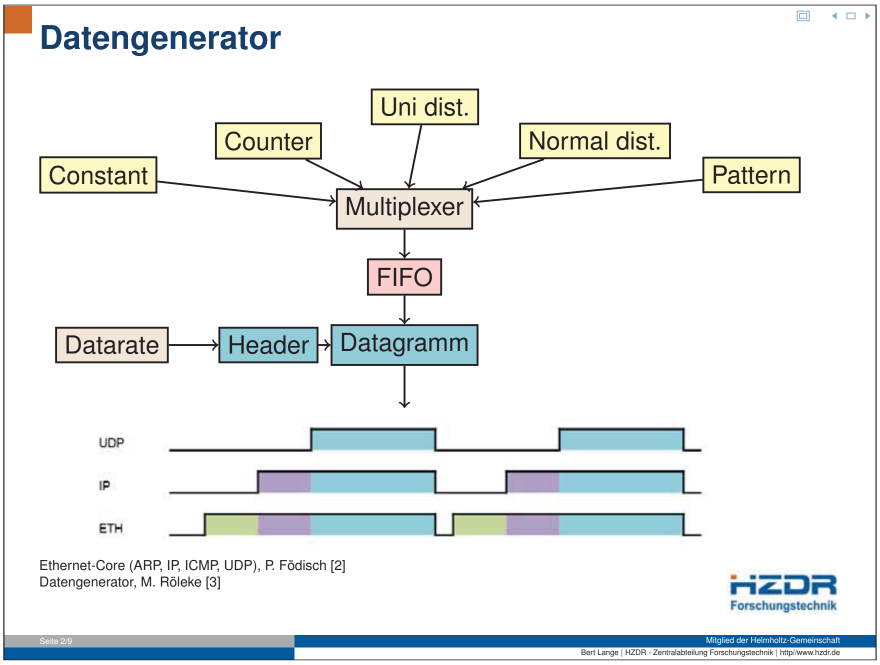
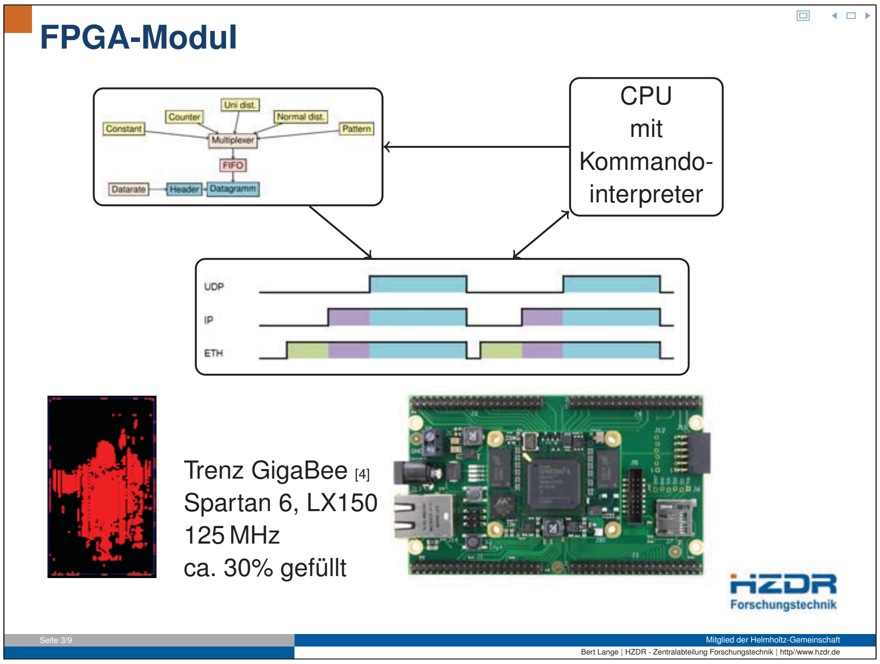


Datengenerator

Uni dist.
Counter
Normal dist.
Constant
Pattern
Multiplexer
FIFO
Datarate
Header
Datagramm

UDP
IP
ETH

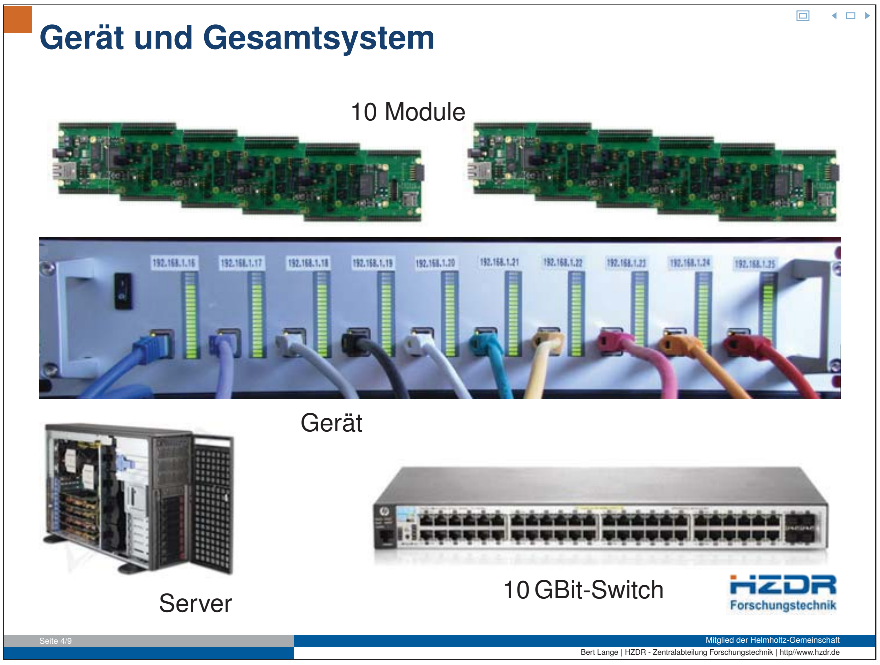
Ethernet-Core (ARP, IP, ICMP, UDP), P. Födisch [2]
Datengenerator, M. Röleke [3]



FPGA-Modul

CPU
mit
Kommando-
interpreter

Trenz GigaBee [4]
Spartan 6, LX150
125 MHz
ca. 30% gefüllt



Gerät und Gesamtsystem

10 Module

Gerät

Server

10 GBit-Switch

Seite 4/9

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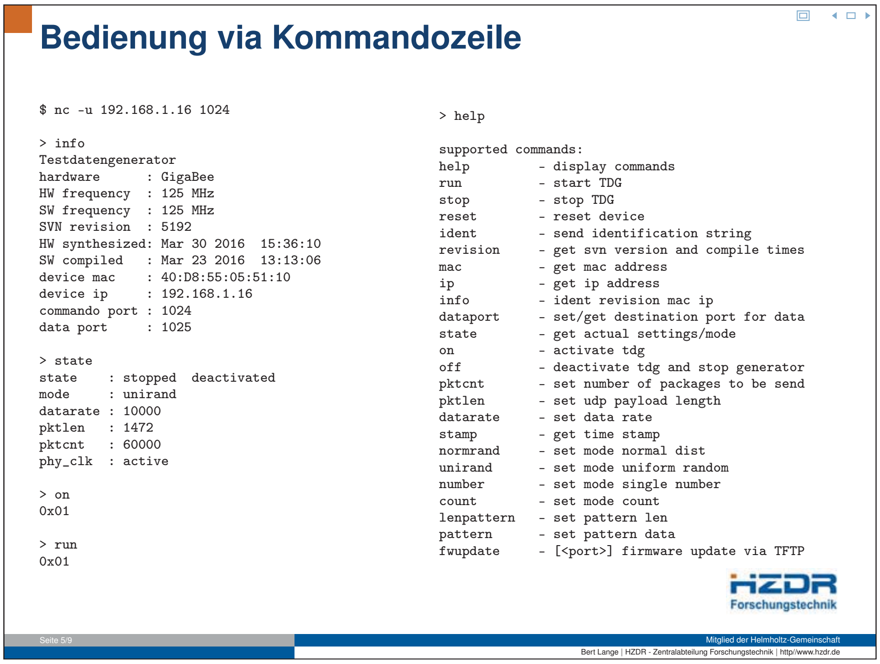

Bedienung via Kommandozeile

```
$ nc -u 192.168.1.16 1024

> info
Testdatengenerator
hardware       : GigaBee
HW frequency   : 125 MHz
SW frequency   : 125 MHz
SVN revision   : 5192
HW synthesized: Mar 30 2016  15:36:10
SW compiled    : Mar 23 2016  13:13:06
device mac     : 40:D8:55:05:51:10
device ip      : 192.168.1.16
commando port : 1024
data port      : 1025

> state
state     : stopped  deactivated
mode      : unirand
datarate : 10000
pktlen    : 1472
pktcnt    : 60000
phy_clk  : active

> on
0x01

> run
0x01
```

```
> help

supported commands:
help         - display commands
run          - start TDG
stop         - stop TDG
reset        - reset device
ident        - send identification string
revision     - get svn version and compile times
mac          - get mac address
ip           - get ip address
info         - ident revision mac ip
dataport     - set/get destination port for data
state        - get actual settings/mode
on           - activate tdg
off          - deactivate tdg and stop generator
pktcnt       - set number of packages to be send
pktlen       - set udp payload length
datarate     - set data rate
stamp        - get time stamp
normrand     - set mode normal dist
unirand      - set mode uniform random
number       - set mode single number
count        - set mode count
lenpattern   - set pattern len
pattern      - set pattern data
fwupdate     - [<port>] firmware update via TFTP
```

Seite 5/9

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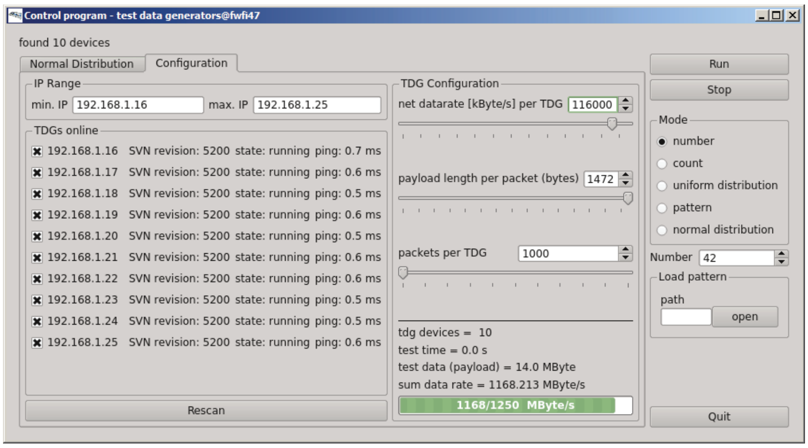
Bedienung via GUI



found 10 devices

IP Range
min. IP 192.168.1.16 max. IP 192.168.1.25

TDGs online
☒ 192.168.1.16 SVN revision: 5200 state: running ping: 0.7 ms
☒ 192.168.1.17 SVN revision: 5200 state: running ping: 0.6 ms
☒ 192.168.1.18 SVN revision: 5200 state: running ping: 0.5 ms
☒ 192.168.1.19 SVN revision: 5200 state: running ping: 0.6 ms
☒ 192.168.1.20 SVN revision: 5200 state: running ping: 0.5 ms
☒ 192.168.1.21 SVN revision: 5200 state: running ping: 0.6 ms
☒ 192.168.1.22 SVN revision: 5200 state: running ping: 0.6 ms
☒ 192.168.1.23 SVN revision: 5200 state: running ping: 0.5 ms
☒ 192.168.1.24 SVN revision: 5200 state: running ping: 0.5 ms
☒ 192.168.1.25 SVN revision: 5200 state: running ping: 0.6 ms

TDG Configuration
net datarate [kByte/s] per TDG 116000
payload length per packet (bytes) 1472
packets per TDG 1000

tdg devices = 10
test time = 0.0 s
test data (payload) = 14.0 MByte
sum data rate = 1168.213 MByte/s
1168/1250 MByte/s

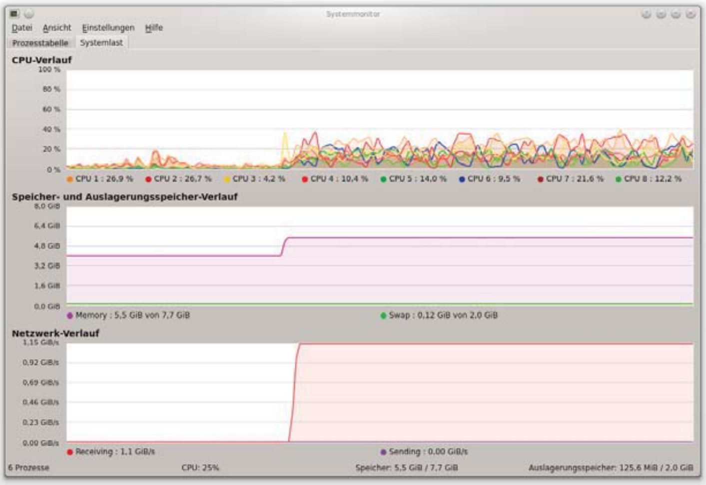
Mode
● number
○ count
○ uniform distribution
○ pattern
○ normal distribution

Number 42

Load pattern
path

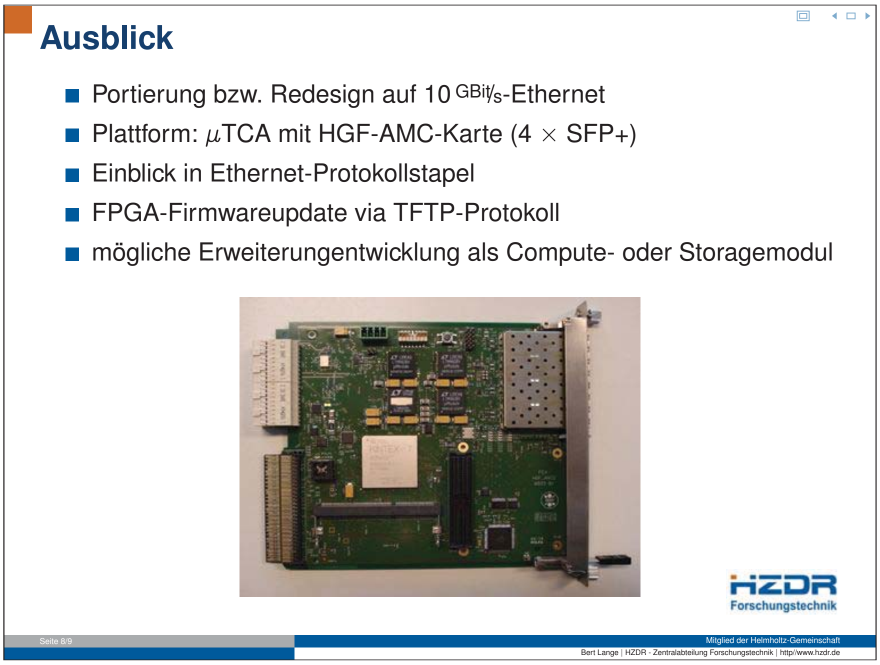
Realisierung mit Python und PyQt

Ergebnisse



Datenrate: 1,11 GByte/s
(ohne Paketverlust)

CPU: Core i7-3770 mit 3,4 GHz



Ausblick

- Portierung bzw. Redesign auf 10 $^{\text{GBit}}/_{\text{s}}$-Ethernet
- Plattform: μTCA mit HGF-AMC-Karte (4 × SFP+)
- Einblick in Ethernet-Protokollstapel
- FPGA-Firmwareupdate via TFTP-Protokoll
- mögliche Erweiterungentwicklung als Compute- oder Storagemodul

HZDR
Forschungstechnik

Seite 8/9

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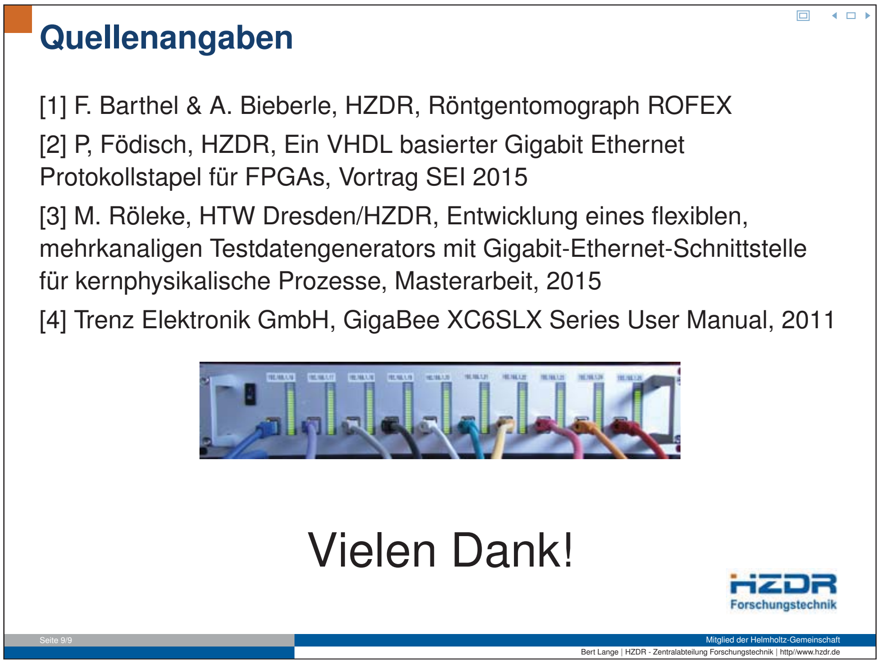
Bert Lange | HZDR - Zentralabteilung Forschungstechnik | http//www.hzdr.de



Quellenangaben

[1] F. Barthel & A. Bieberle, HZDR, Röntgentomograph ROFEX

[2] P, Födisch, HZDR, Ein VHDL basierter Gigabit Ethernet Protokollstapel für FPGAs, Vortrag SEI 2015

[3] M. Röleke, HTW Dresden/HZDR, Entwicklung eines flexiblen, mehrkanaligen Testdatengenerators mit Gigabit-Ethernet-Schnittstelle für kernphysikalische Prozesse, Masterarbeit, 2015

[4] Trenz Elektronik GmbH, GigaBee XC6SLX Series User Manual, 2011

Vielen Dank!

HZDR
Forschungstechnik

Seite 9/9

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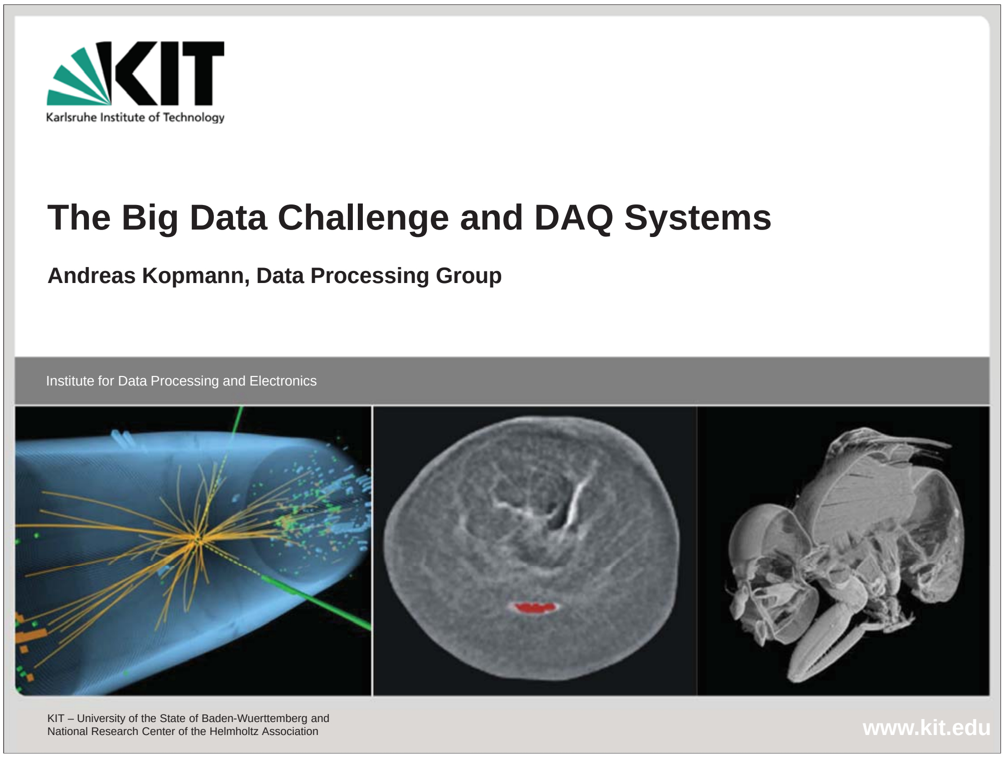


Karlsruhe Institute of Technology

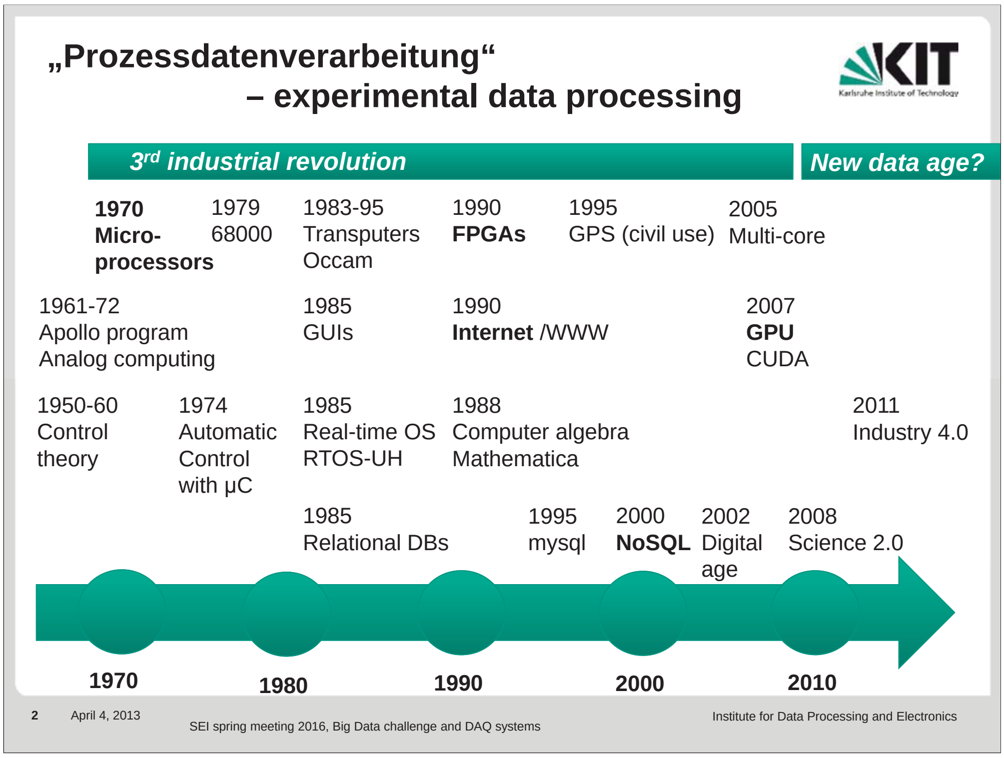
The Big Data Challenge and DAQ Systems

Andreas Kopmann, Data Processing Group

Institute for Data Processing and Electronics

KIT – University of the State of Baden-Wuerttemberg and
National Research Center of the Helmholtz Association

www.kit.edu



„Prozessdatenverarbeitung“ – experimental data processing

Karlsruhe Institute of Technology

3rd industrial revolution

New data age?

1970 Micro-processors

1979 68000

1983-95 Transputers Occam

1990 **FPGAs**

1995 GPS (civil use)

2005 Multi-core

1961-72 Apollo program Analog computing

1985 GUIs

1990 **Internet** /WWW

2007 **GPU** CUDA

1950-60 Control theory

1974 Automatic Control with µC

1985 Real-time OS RTOS-UH

1988 Computer algebra Mathematica

2011 Industry 4.0

1985 Relational DBs

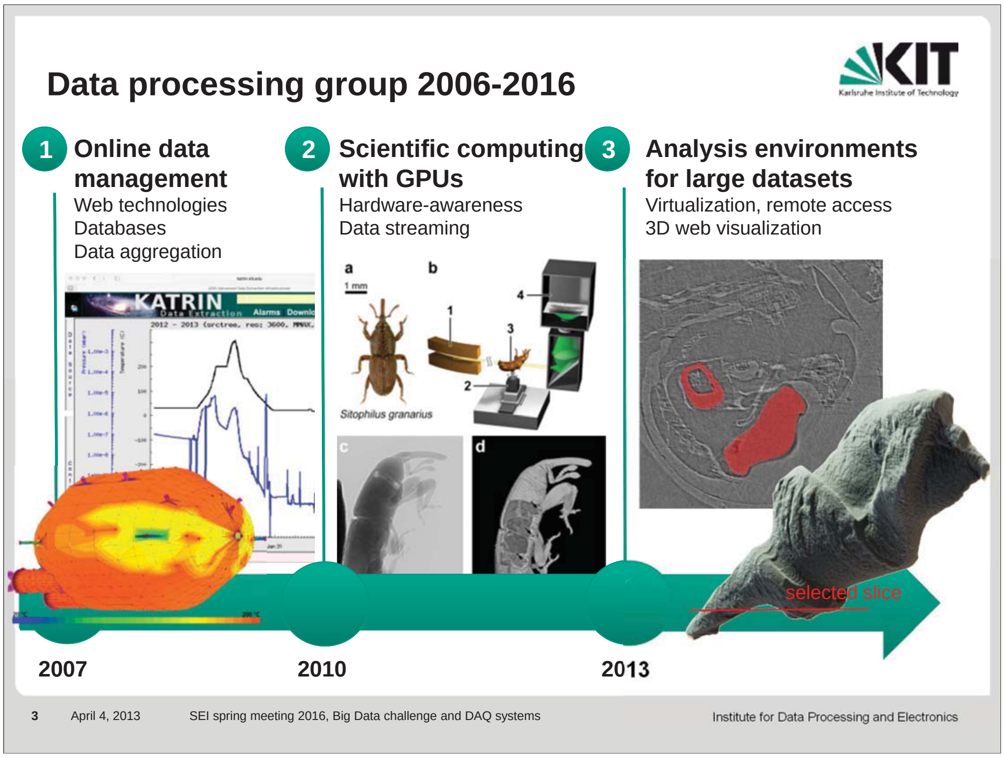
1995 mysql

2000 **NoSQL**

2002 Digital age

2008 Science 2.0

2 April 4, 2013 SEI spring meeting 2016, Big Data challenge and DAQ systems Institute for Data Processing and Electronics



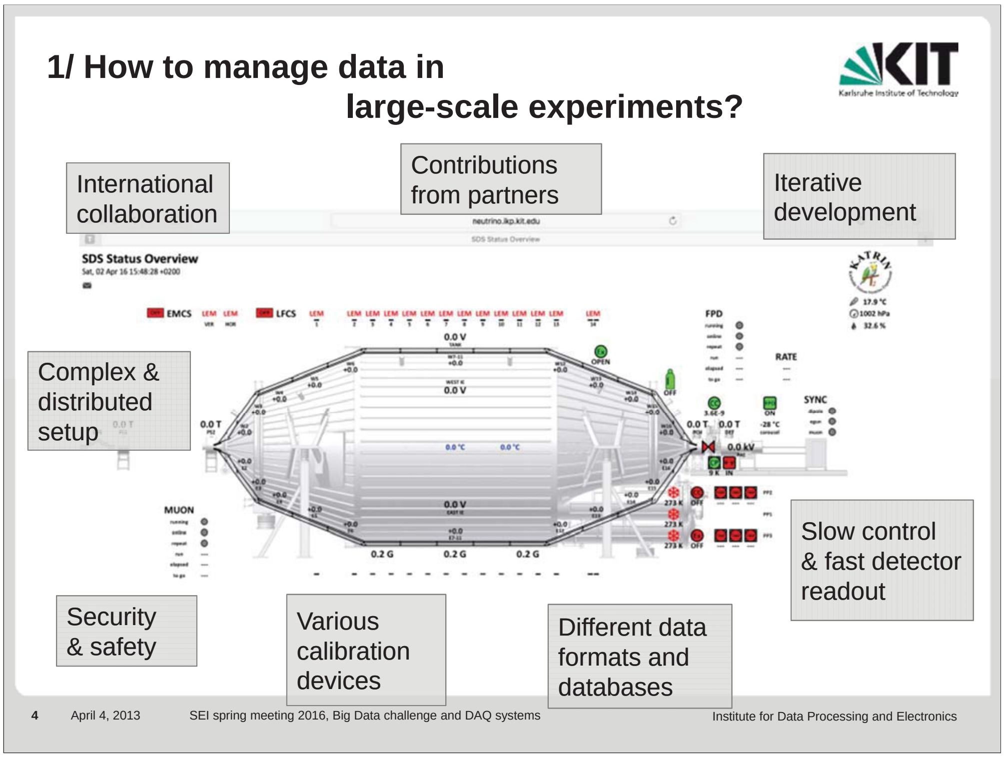
Data processing group 2006-2016

1 **Online data management**
Web technologies
Databases
Data aggregation

2 **Scientific computing with GPUs**
Hardware-awareness
Data streaming

3 **Analysis environments for large datasets**
Virtualization, remote access
3D web visualization

2007
2010
2013



1/ How to manage data in large-scale experiments?

International collaboration

Contributions from partners

Iterative development

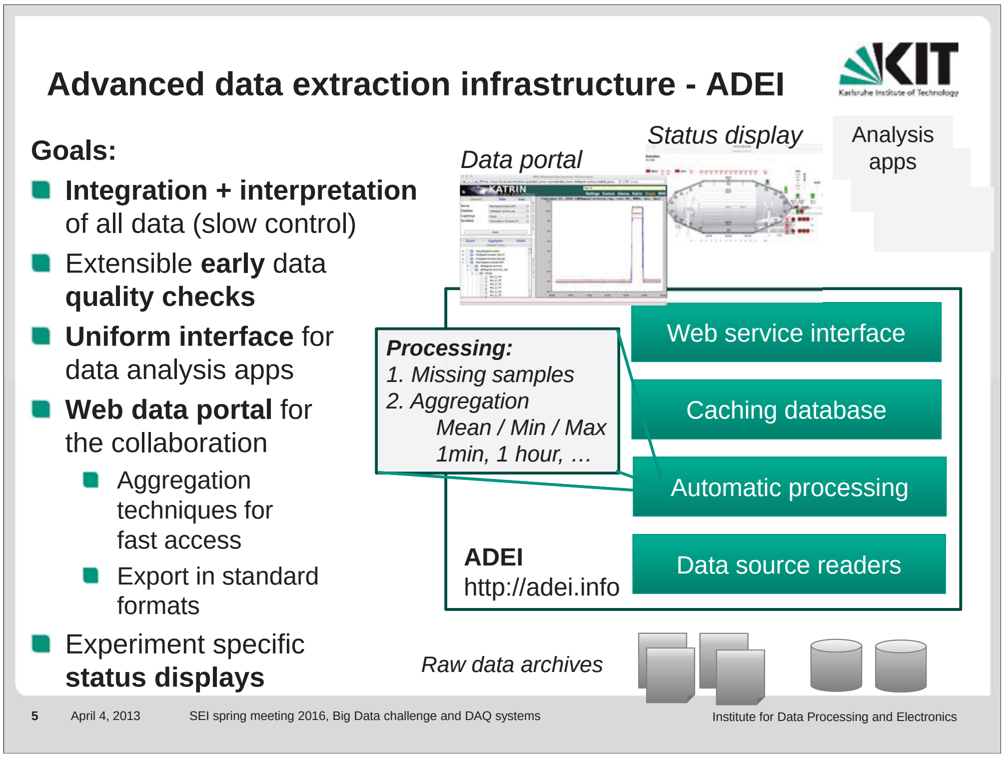
Complex & distributed setup

Slow control & fast detector readout

Security & safety

Various calibration devices

Different data formats and databases



Advanced data extraction infrastructure - ADEI

Goals:

- **Integration + interpretation** of all data (slow control)
- Extensible **early** data **quality checks**
- **Uniform interface** for data analysis apps
- **Web data portal** for the collaboration
  - Aggregation techniques for fast access
  - Export in standard formats
- Experiment specific **status displays**

Data portal

Status display

Analysis apps

Processing:
1. Missing samples
2. Aggregation
Mean / Min / Max
1min, 1 hour, …

Web service interface

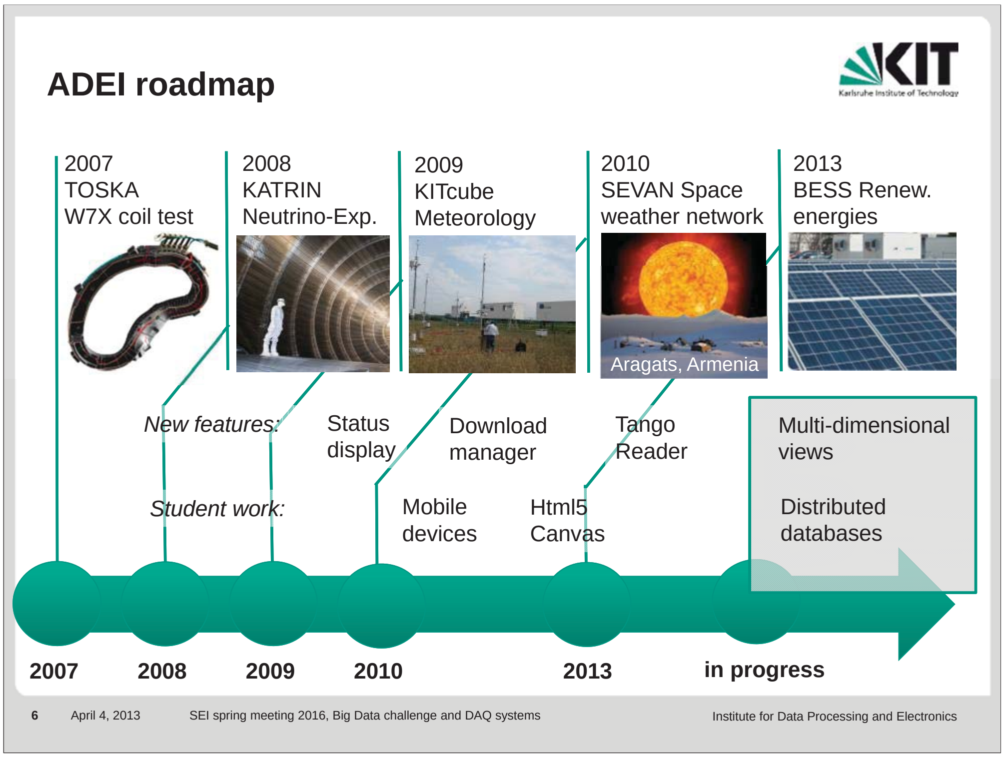
Caching database

Automatic processing

Data source readers

ADEI
http://adei.info

Raw data archives



ADEI roadmap

2007
TOSKA
W7X coil test

2008
KATRIN
Neutrino-Exp.

2009
KITcube
Meteorology

2010
SEVAN Space
weather network

Aragats, Armenia

2013
BESS Renew.
energies

New features:

Status display

Download manager

Tango Reader

Multi-dimensional views

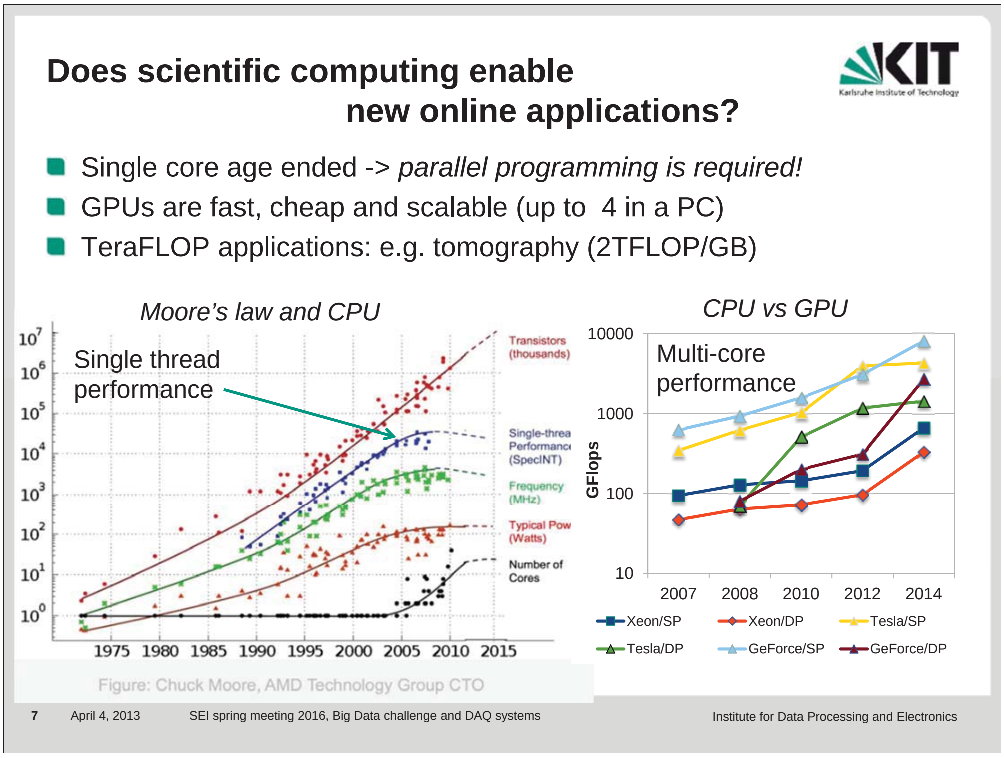
Student work:

Mobile devices

Html5 Canvas

Distributed databases

2007 **2008** **2009** **2010** **2013** **in progress**



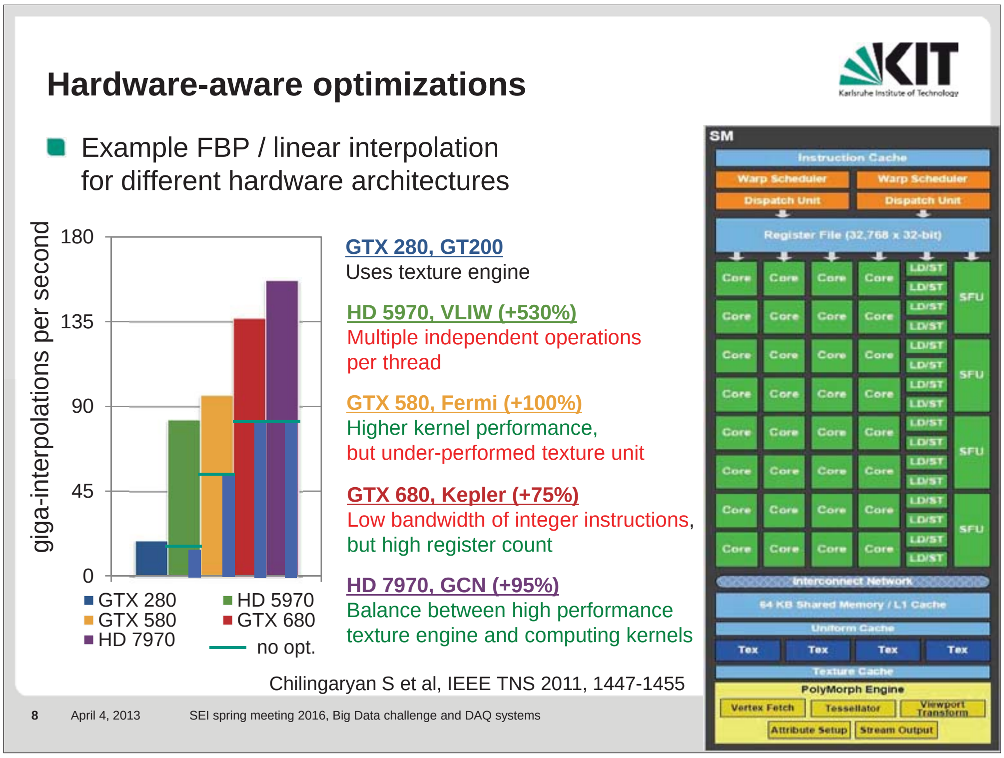
Does scientific computing enable new online applications?

- Single core age ended -> *parallel programming is required!*
- GPUs are fast, cheap and scalable (up to 4 in a PC)
- TeraFLOP applications: e.g. tomography (2TFLOP/GB)

Moore's law and CPU

Figure: Chuck Moore, AMD Technology Group CTO

CPU vs GPU



Hardware-aware optimizations

- Example FBP / linear interpolation
  for different hardware architectures

GTX 280, GT200
Uses texture engine

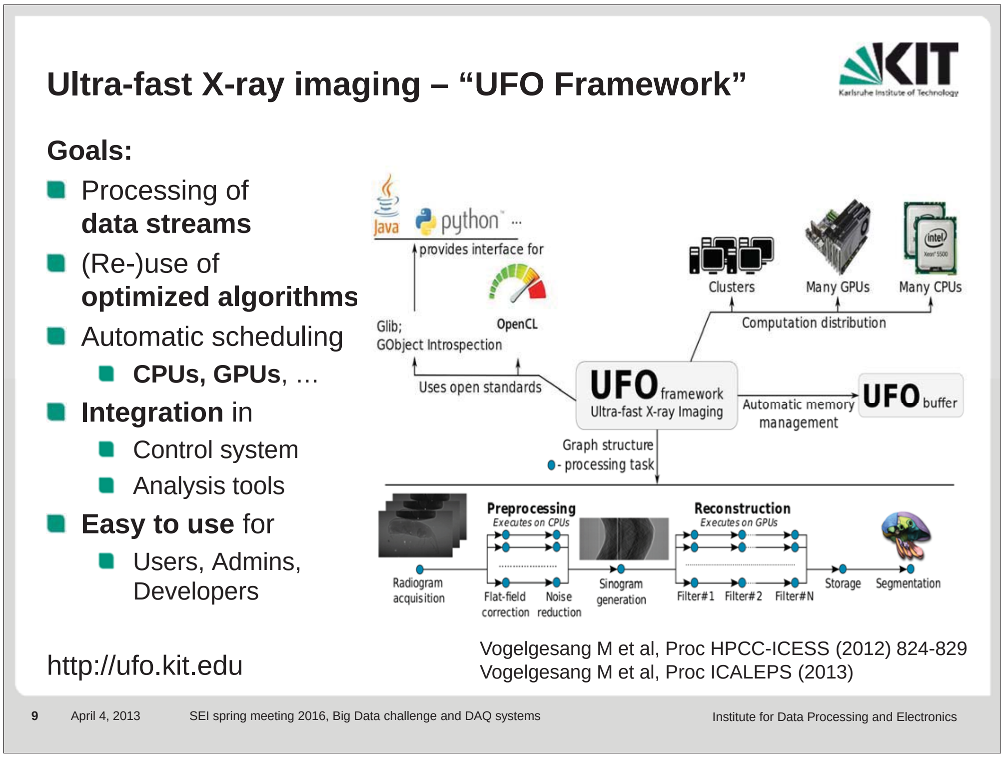
HD 5970, VLIW (+530%)
Multiple independent operations per thread

GTX 580, Fermi (+100%)
Higher kernel performance, but under-performed texture unit

GTX 680, Kepler (+75%)
Low bandwidth of integer instructions, but high register count

HD 7970, GCN (+95%)
Balance between high performance texture engine and computing kernels

Chilingaryan S et al, IEEE TNS 2011, 1447-1455



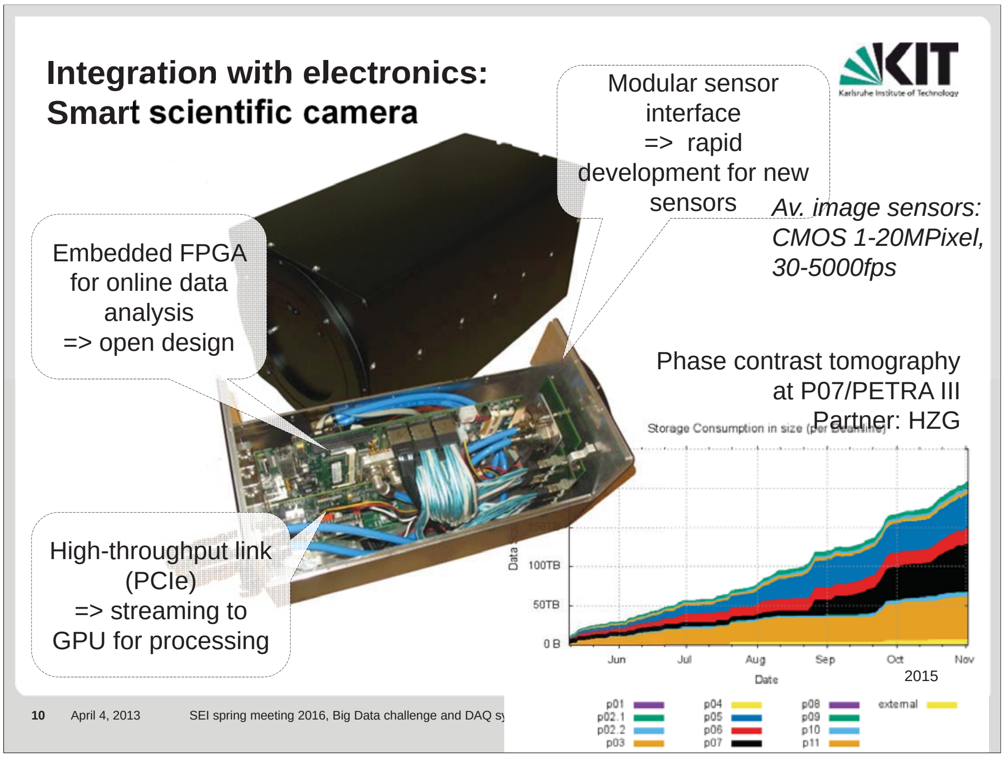
Ultra-fast X-ray imaging – “UFO Framework”

Goals:

- Processing of **data streams**
- (Re-)use of **optimized algorithms**
- Automatic scheduling
  - **CPUs, GPUs**, …
- **Integration** in
  - Control system
  - Analysis tools
- **Easy to use** for
  - Users, Admins, Developers

http://ufo.kit.edu

Vogelgesang M et al, Proc HPCC-ICESS (2012) 824-829
Vogelgesang M et al, Proc ICALEPS (2013)



Integration with electronics: Smart scientific camera

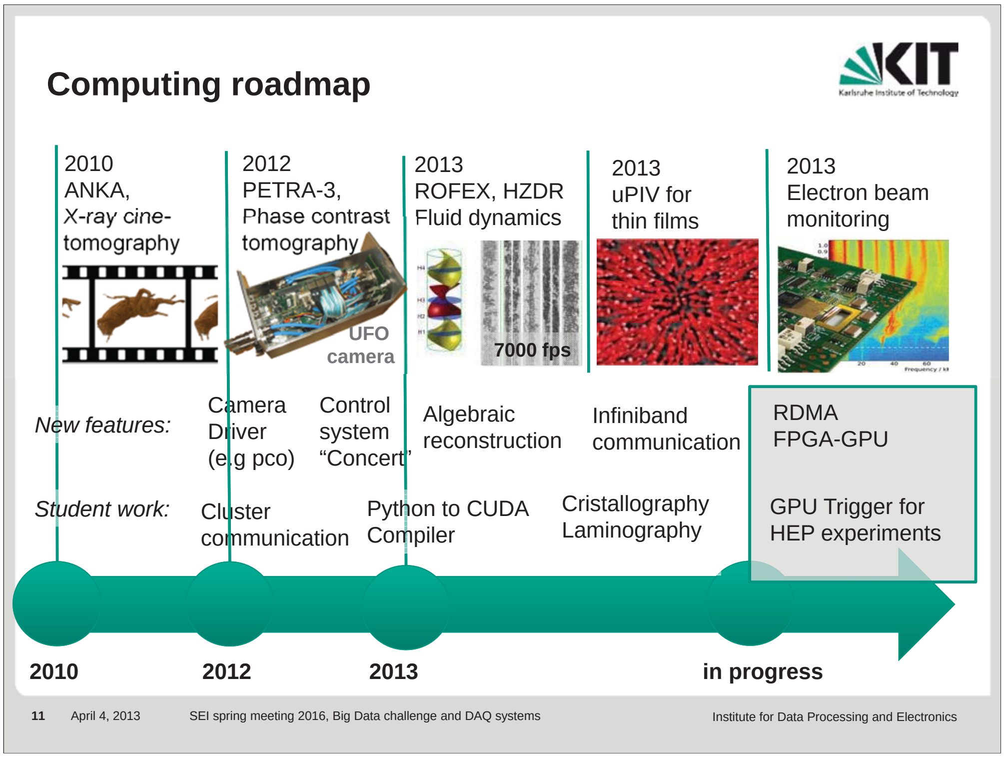
Modular sensor interface
=> rapid development for new sensors

Av. image sensors:
CMOS 1-20MPixel,
30-5000fps

Embedded FPGA for online data analysis
=> open design

High-throughput link (PCIe)
=> streaming to GPU for processing

Phase contrast tomography
at P07/PETRA III
Partner: HZG



Computing roadmap

2010
ANKA,
X-ray cine-
tomography

2012
PETRA-3,
Phase contrast
tomography

2013
ROFEX, HZDR
Fluid dynamics

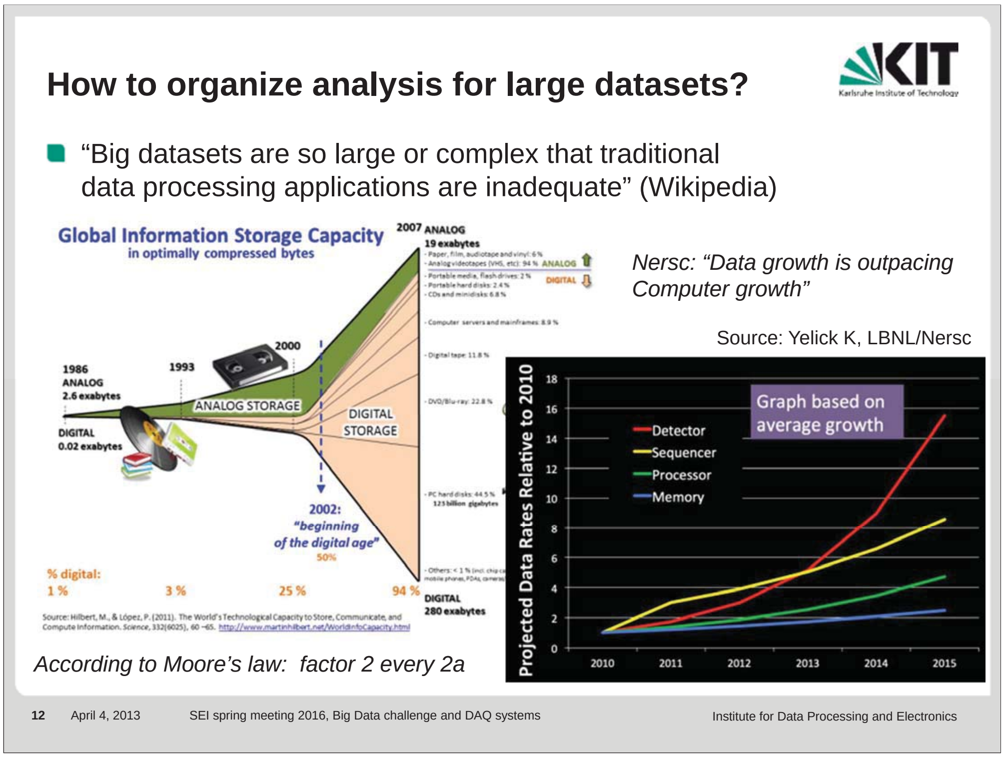
2013
uPIV for
thin films

2013
Electron beam
monitoring

New features:
Camera Driver (e.g pco)
Control system "Concert"
Algebraic reconstruction
Infiniband communication
RDMA
FPGA-GPU

Student work:
Cluster communication
Python to CUDA Compiler
Cristallography
Laminography
GPU Trigger for HEP experiments

2010 **2012** **2013** **in progress**



How to organize analysis for large datasets?

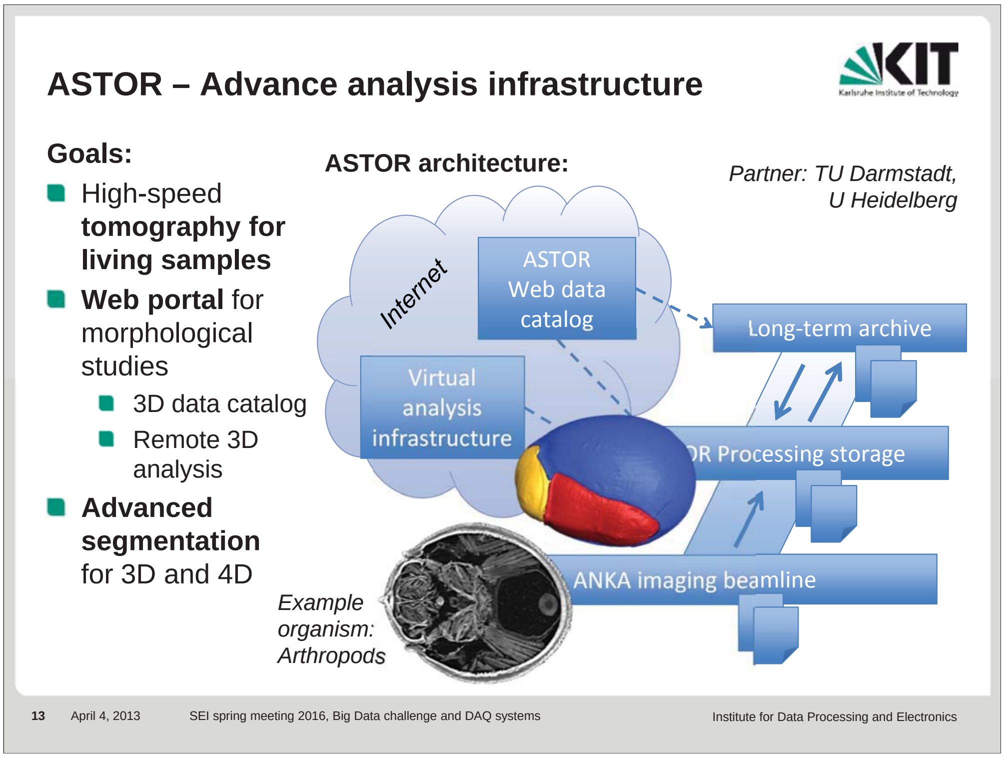
- "Big datasets are so large or complex that traditional data processing applications are inadequate" (Wikipedia)

Source: Hilbert, M., & López, P. (2011). The World's Technological Capacity to Store, Communicate, and Compute Information. Science, 332(6025), 60 –65. http://www.martinhilbert.net/WorldInfoCapacity.html

Nersc: "Data growth is outpacing Computer growth"

Source: Yelick K, LBNL/Nersc

According to Moore's law: factor 2 every 2a



ASTOR – Advance analysis infrastructure

Goals:

- High-speed **tomography for living samples**
- **Web portal** for morphological studies
  - 3D data catalog
  - Remote 3D analysis
- **Advanced segmentation** for 3D and 4D

ASTOR architecture:

Partner: TU Darmstadt,
U Heidelberg

Internet

ASTOR Web data catalog

Long-term archive

Virtual analysis infrastructure

OR Processing storage

ANKA imaging beamline

Example organism: Arthropods

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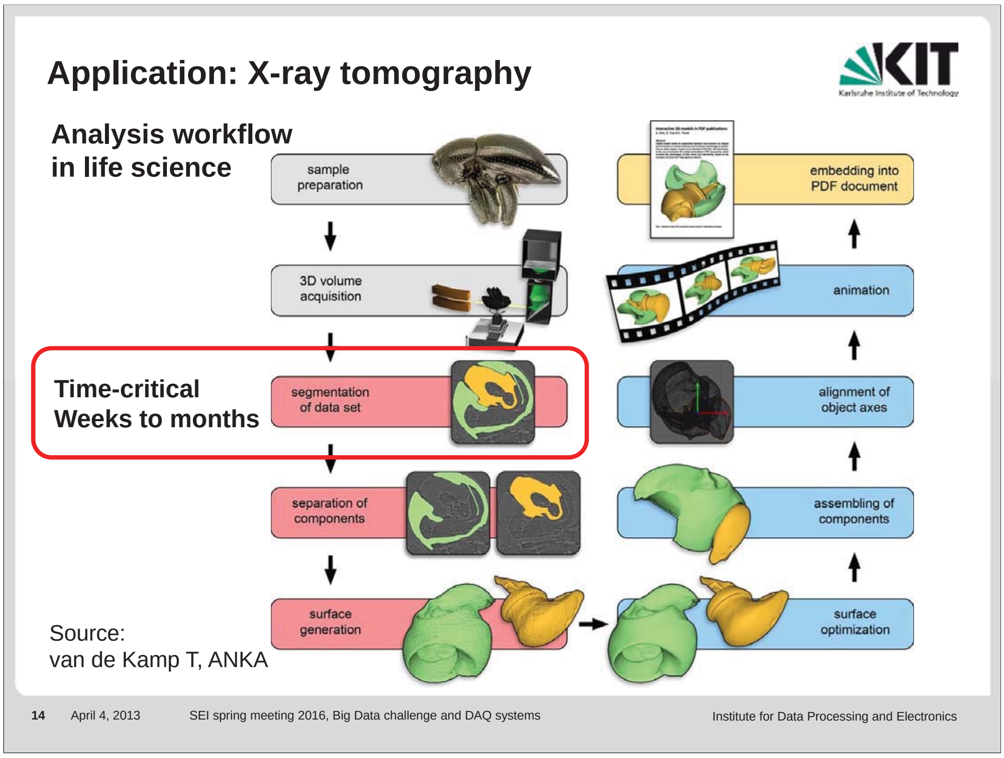

Application: X-ray tomography

Analysis workflow in life science

sample preparation

3D volume acquisition

segmentation of data set

separation of components

surface generation

surface optimization

assembling of components

alignment of object axes

animation

embedding into PDF document

Time-critical
Weeks to months

Source:
van de Kamp T, ANKA

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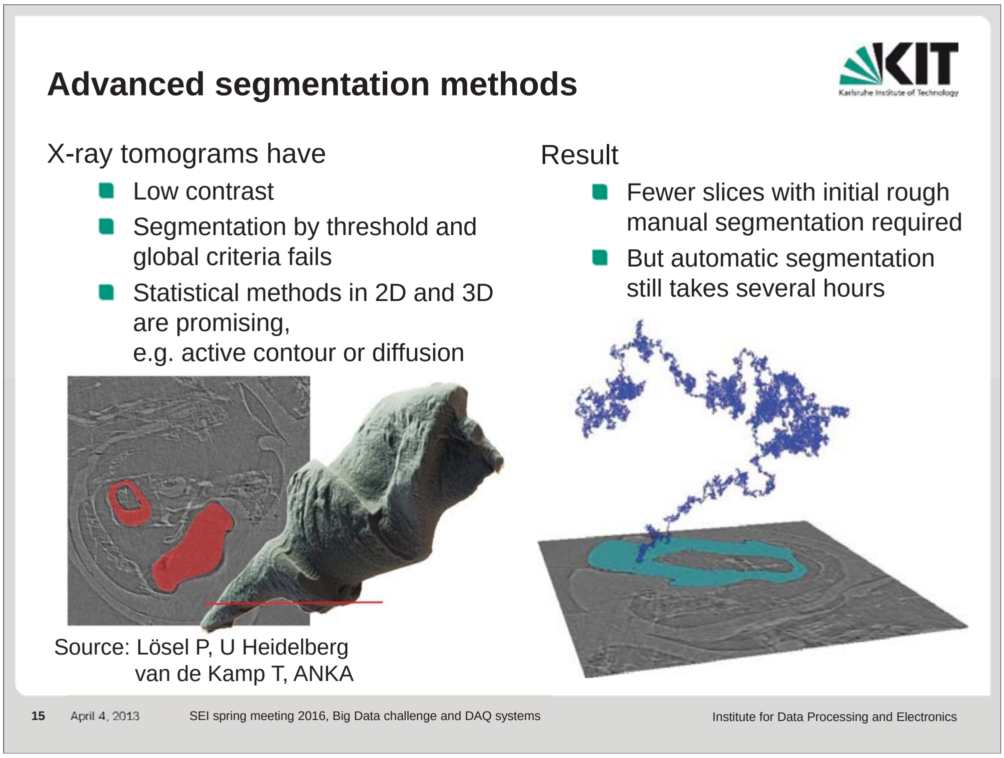


Advanced segmentation methods

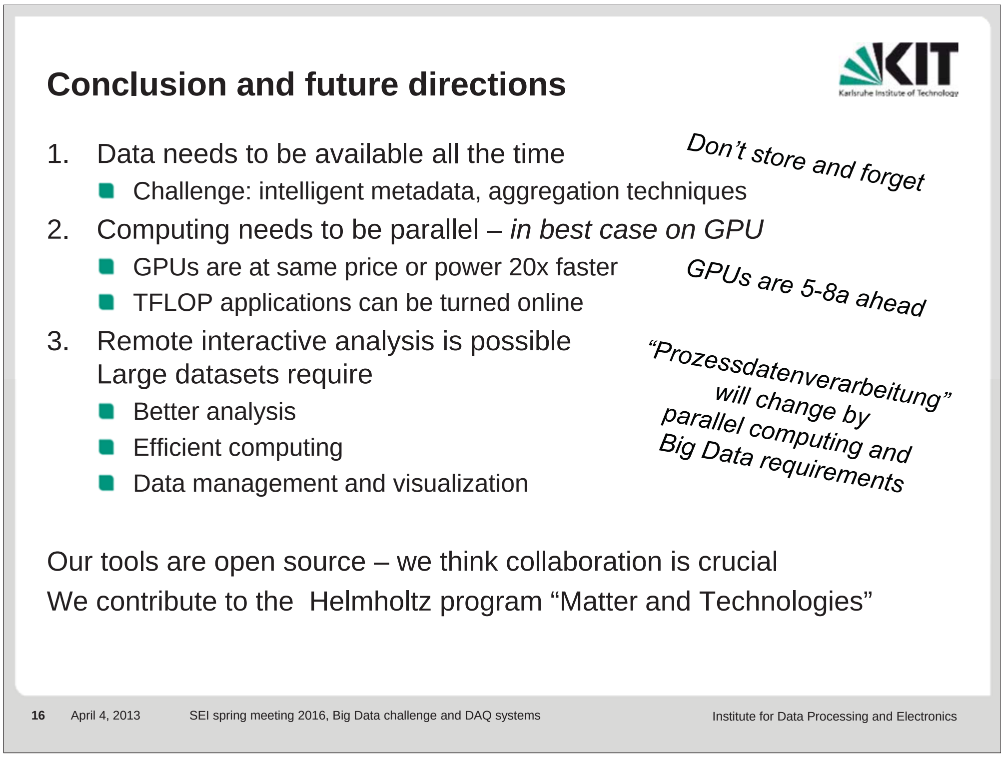
X-ray tomograms have

- Low contrast
- Segmentation by threshold and global criteria fails
- Statistical methods in 2D and 3D are promising, e.g. active contour or diffusion

Source: Lösel P, U Heidelberg
van de Kamp T, ANKA

Result

- Fewer slices with initial rough manual segmentation required
- But automatic segmentation still takes several hours



Conclusion and future directions

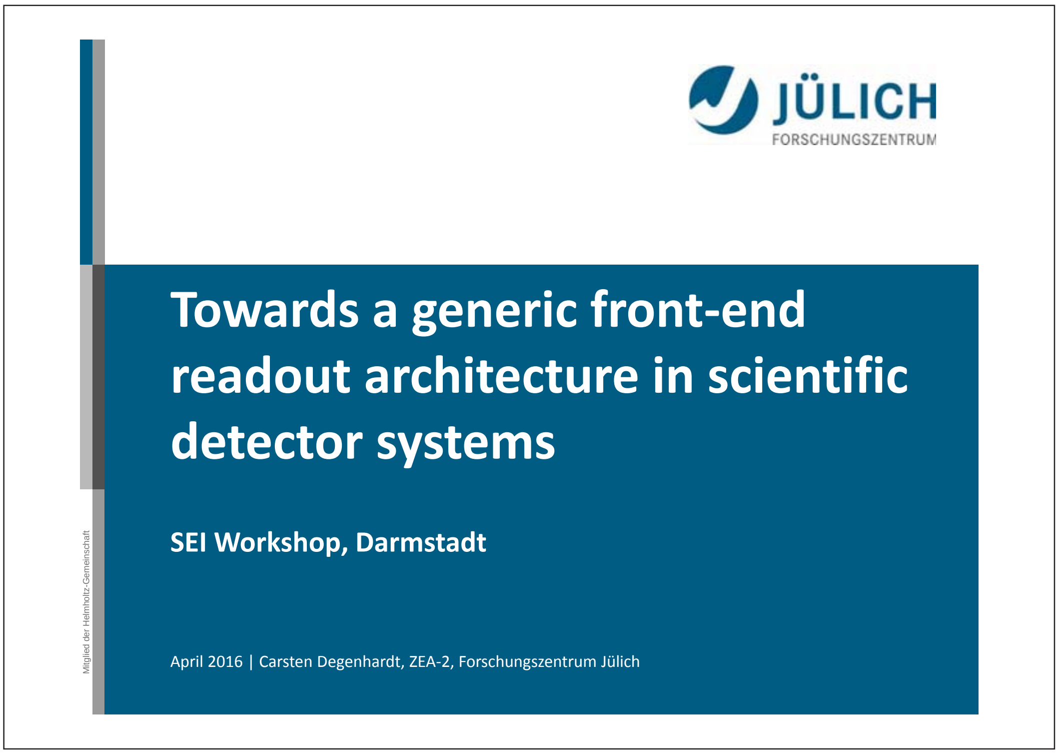
1. Data needs to be available all the time
   - Challenge: intelligent metadata, aggregation techniques
2. Computing needs to be parallel – *in best case on GPU*
   - GPUs are at same price or power 20x faster
   - TFLOP applications can be turned online
3. Remote interactive analysis is possible
   Large datasets require
   - Better analysis
   - Efficient computing
   - Data management and visualization

Don't store and forget

GPUs are 5-8a ahead

"Prozessdatenverarbeitung" will change by parallel computing and Big Data requirements

Our tools are open source – we think collaboration is crucial
We contribute to the Helmholtz program "Matter and Technologies"



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Towards a generic front-end readout architecture in scientific detector systems

SEI Workshop, Darmstadt

April 2016 | Carsten Degenhardt, ZEA-2, Forschungszentrum Jülich

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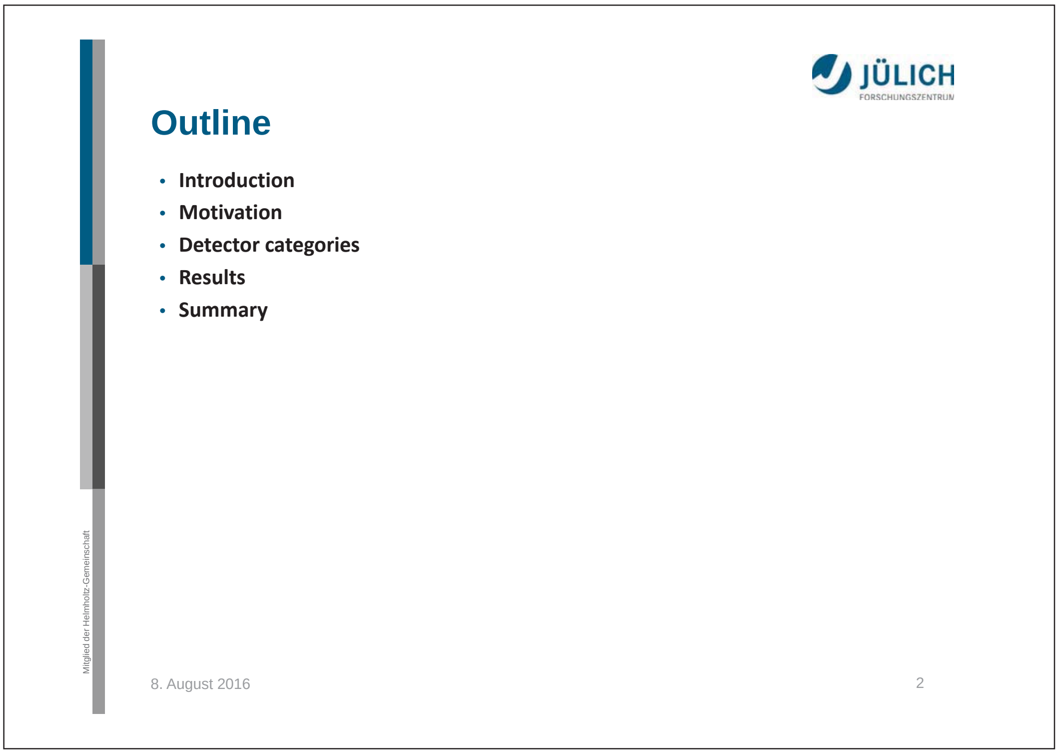

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Outline

- Introduction
- Motivation
- Detector categories
- Results
- Summary

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8. August 2016

Science Campus Jülich

ZEA-2, Central Institute of Engineering, Electronics and Analytics

**Future is Our Mission –
Research & development on 2.2km²**

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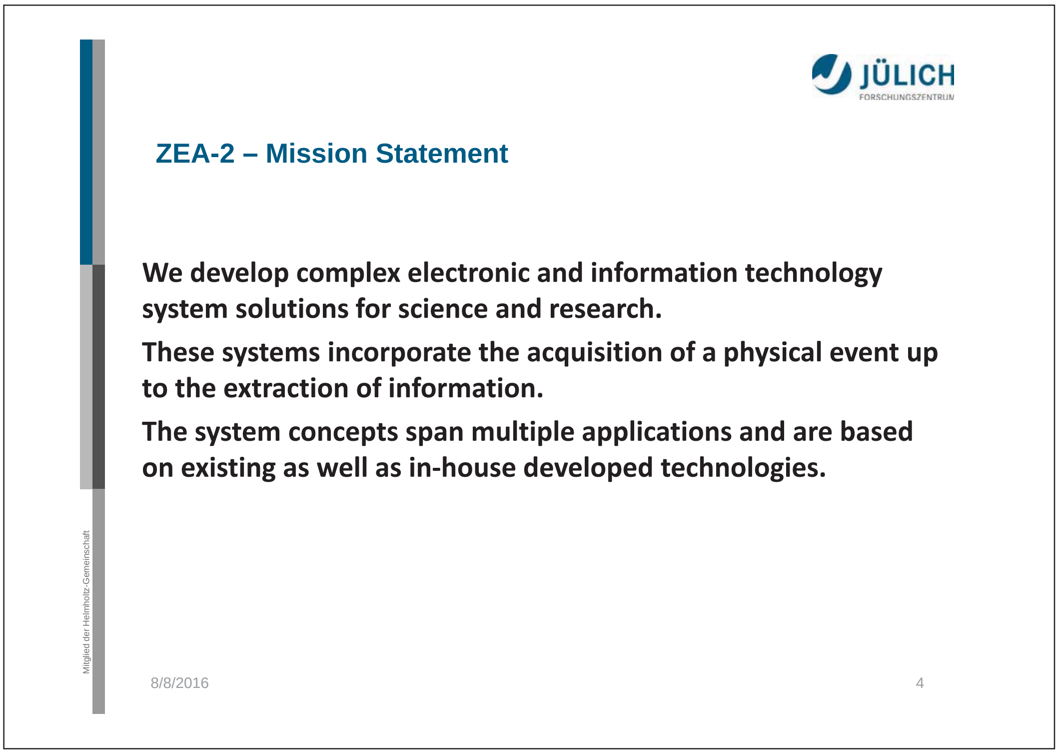

ZEA-2 – Mission Statement

We develop complex electronic and information technology system solutions for science and research.

These systems incorporate the acquisition of a physical event up to the extraction of information.

The system concepts span multiple applications and are based on existing as well as in-house developed technologies.

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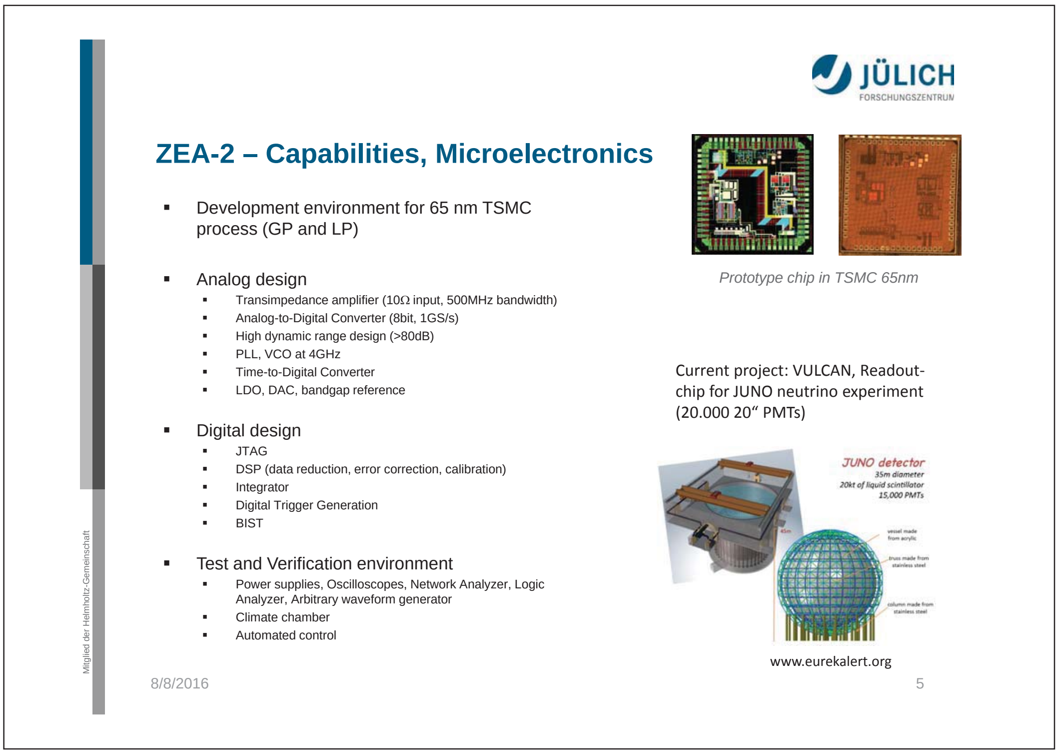


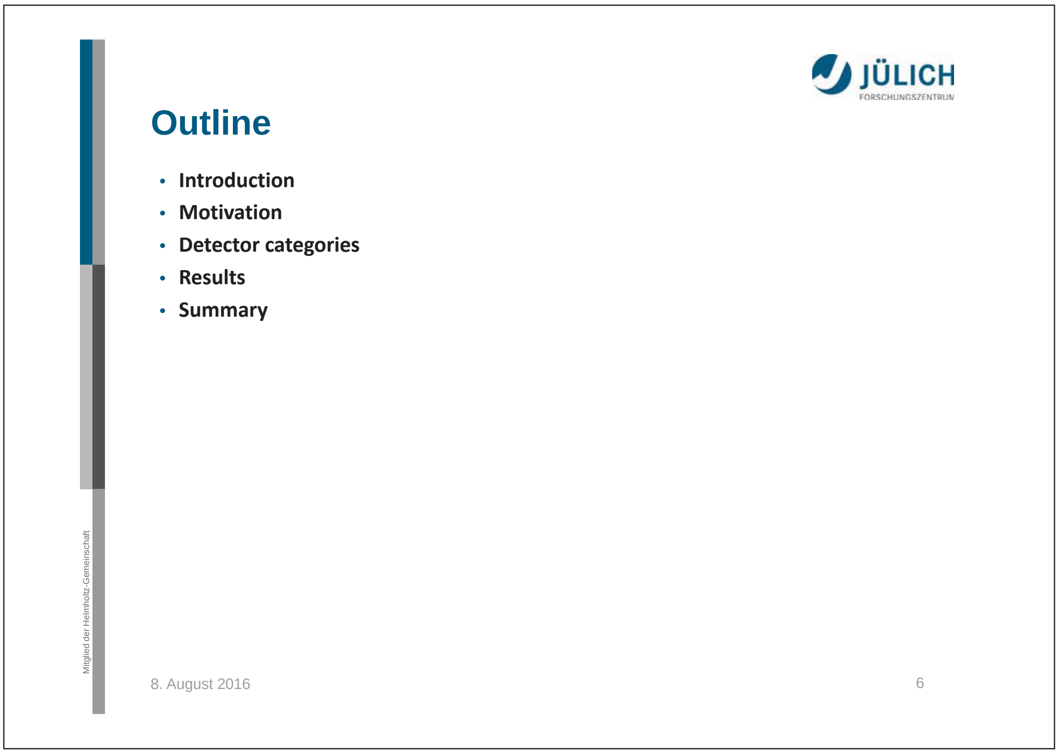
ZEA-2 – Capabilities, Microelectronics

- Development environment for 65 nm TSMC process (GP and LP)
- Analog design
  - Transimpedance amplifier (10Ω input, 500MHz bandwidth)
  - Analog-to-Digital Converter (8bit, 1GS/s)
  - High dynamic range design (>80dB)
  - PLL, VCO at 4GHz
  - Time-to-Digital Converter
  - LDO, DAC, bandgap reference
- Digital design
  - JTAG
  - DSP (data reduction, error correction, calibration)
  - Integrator
  - Digital Trigger Generation
  - BIST
- Test and Verification environment
  - Power supplies, Oscilloscopes, Network Analyzer, Logic Analyzer, Arbitrary waveform generator
  - Climate chamber
  - Automated control

Prototype chip in TSMC 65nm

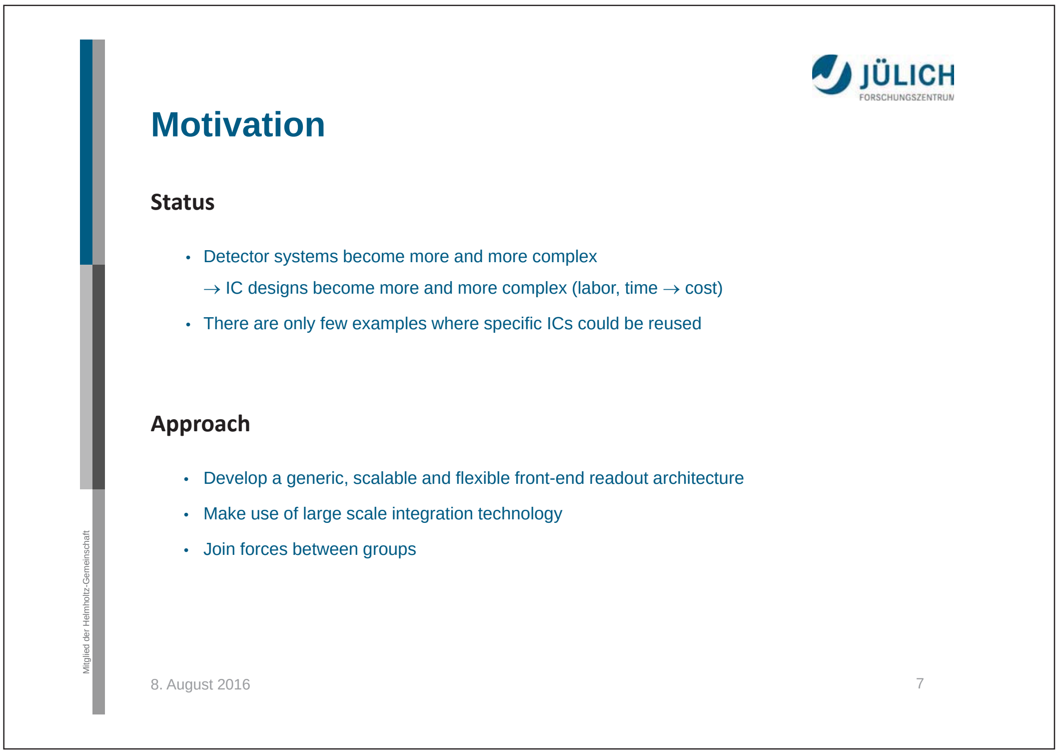
Current project: VULCAN, Readout-chip for JUNO neutrino experiment (20.000 20“ PMTs)

www.eurekalert.org



Outline

- **Introduction**
- **Motivation**
- **Detector categories**
- **Results**
- **Summary**



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Motivation

Status

- Detector systems become more and more complex
  → IC designs become more and more complex (labor, time → cost)
- There are only few examples where specific ICs could be reused

Approach

- Develop a generic, scalable and flexible front-end readout architecture
- Make use of large scale integration technology
- Join forces between groups

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Motivation

Benefits

- Allows a faster system integration into multiple applications
- Shorter development cycles
- Unified interfaces
- Reuse of existing hardware, firmware, software
- Less resources needed compared to dedicated developments
- Opens up new possibilities with respect to performance and flexibility
- Smaller form-factor
- Easier detector upgrades
- Upgrades directly benefit from advancements in large scale integration technology
- Easier (less time consuming) maintenance

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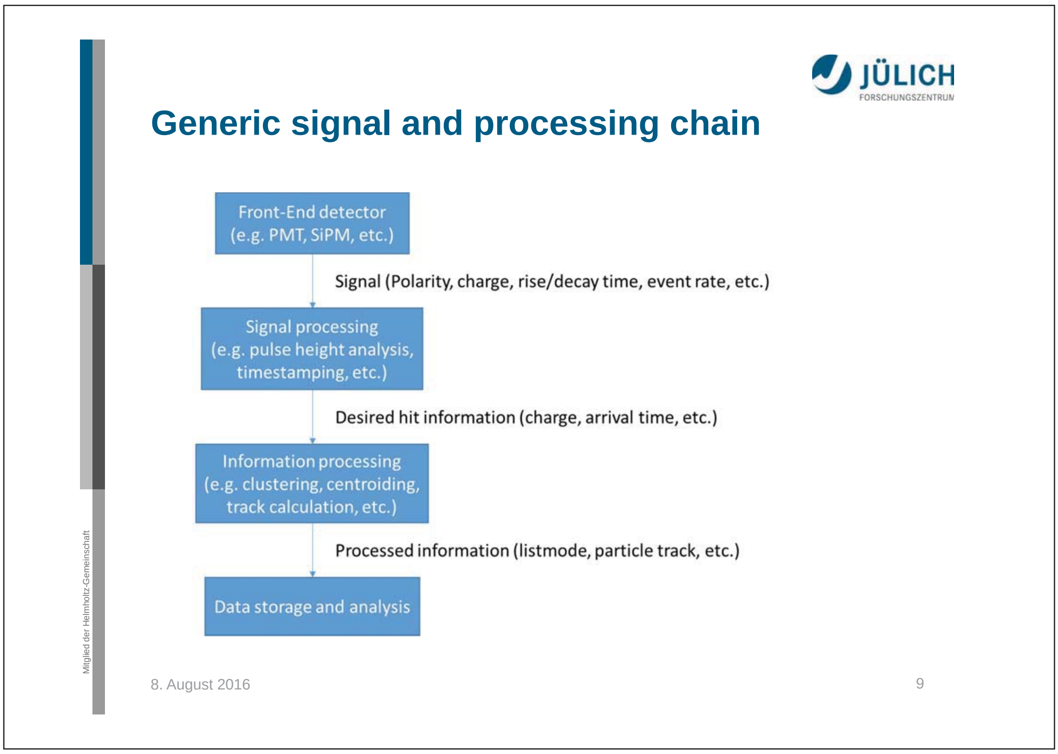


Generic signal and processing chain

Front-End detector (e.g. PMT, SiPM, etc.)

Signal (Polarity, charge, rise/decay time, event rate, etc.)

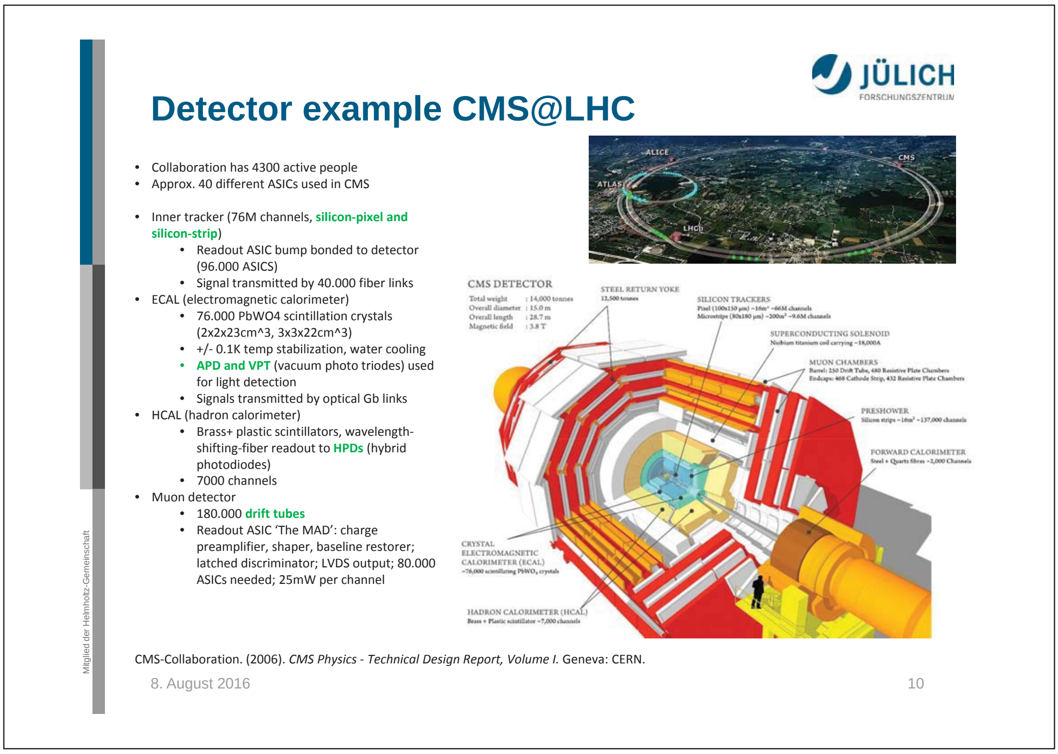
Signal processing (e.g. pulse height analysis, timestamping, etc.)

Desired hit information (charge, arrival time, etc.)

Information processing (e.g. clustering, centroiding, track calculation, etc.)

Processed information (listmode, particle track, etc.)

Data storage and analysis

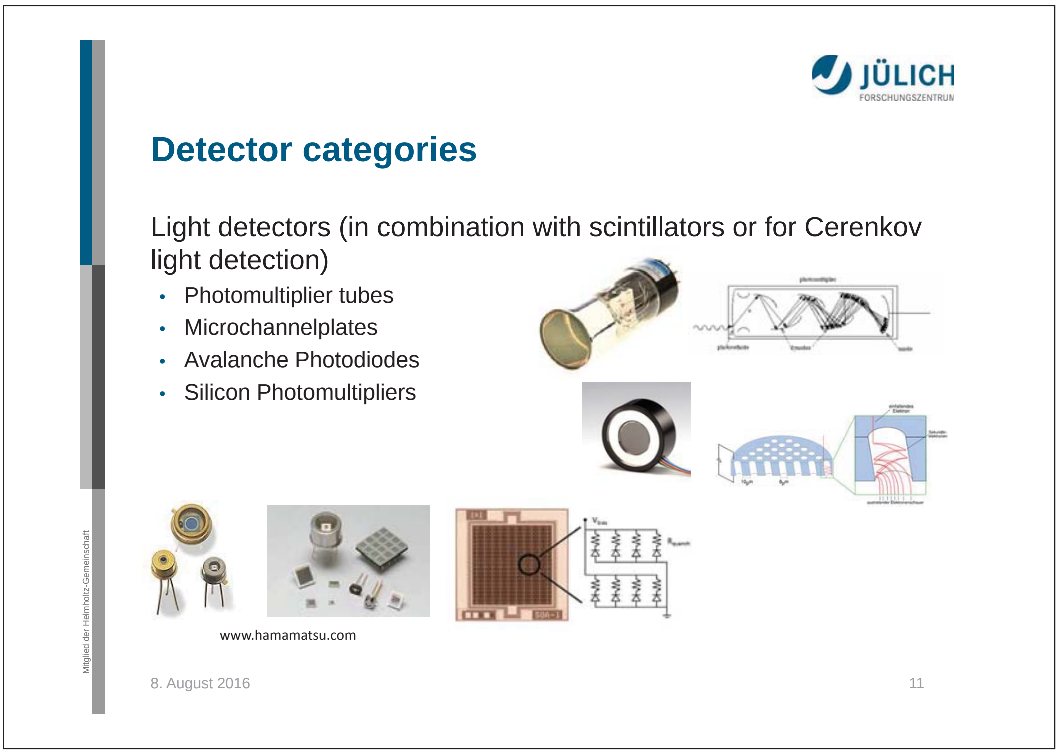


Detector example CMS@LHC

- Collaboration has 4300 active people
- Approx. 40 different ASICs used in CMS

- Inner tracker (76M channels, **silicon-pixel and silicon-strip**)
  - Readout ASIC bump bonded to detector (96.000 ASICS)
  - Signal transmitted by 40.000 fiber links
- ECAL (electromagnetic calorimeter)
  - 76.000 PbWO4 scintillation crystals (2x2x23cm^3, 3x3x22cm^3)
  - +/- 0.1K temp stabilization, water cooling
  - **APD and VPT** (vacuum photo triodes) used for light detection
  - Signals transmitted by optical Gb links
- HCAL (hadron calorimeter)
  - Brass+ plastic scintillators, wavelength-shifting-fiber readout to **HPDs** (hybrid photodiodes)
  - 7000 channels
- Muon detector
  - 180.000 **drift tubes**
  - Readout ASIC 'The MAD': charge preamplifier, shaper, baseline restorer; latched discriminator; LVDS output; 80.000 ASICs needed; 25mW per channel

CMS-Collaboration. (2006). *CMS Physics - Technical Design Report, Volume I.* Geneva: CERN.



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Detector categories

Light detectors (in combination with scintillators or for Cerenkov light detection)

- Photomultiplier tubes
- Microchannelplates
- Avalanche Photodiodes
- Silicon Photomultipliers

www.hamamatsu.com

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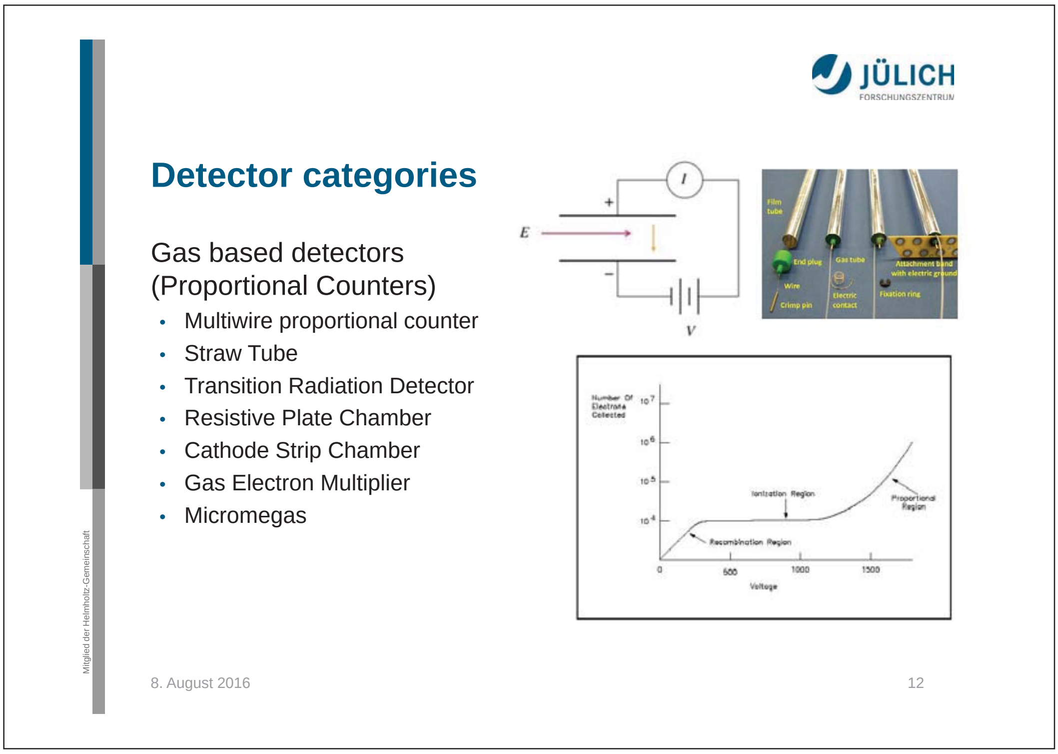

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Detector categories

Gas based detectors (Proportional Counters)

- Multiwire proportional counter
- Straw Tube
- Transition Radiation Detector
- Resistive Plate Chamber
- Cathode Strip Chamber
- Gas Electron Multiplier
- Micromegas

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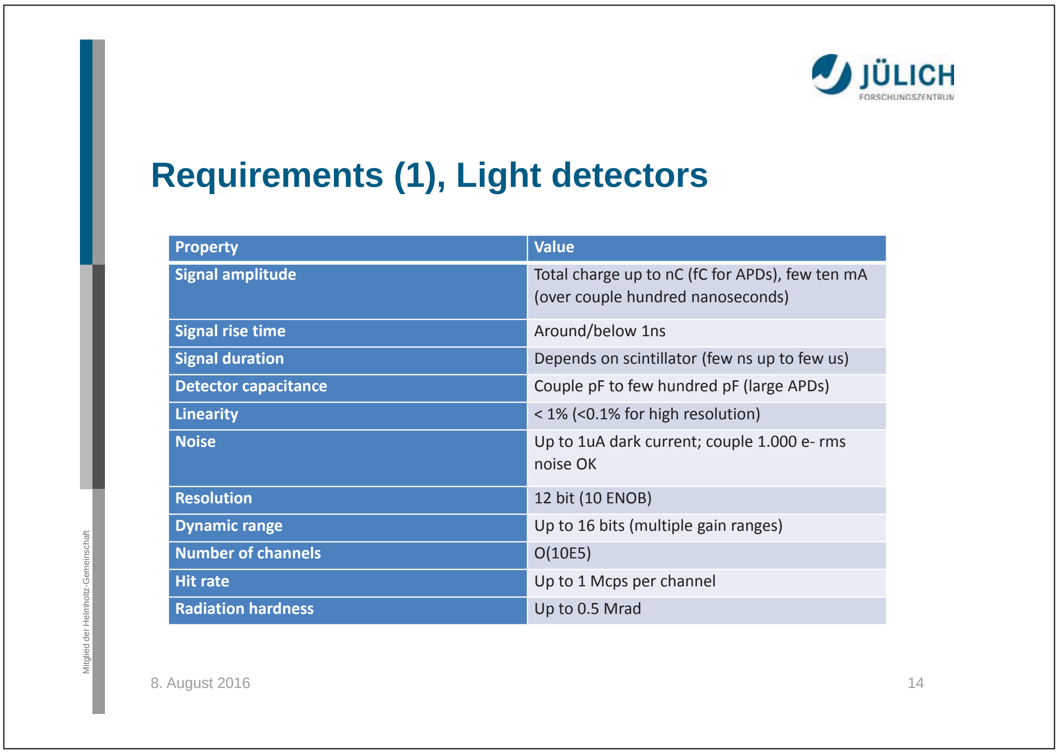
Detector categories

Silicon Direct Converter Detectors

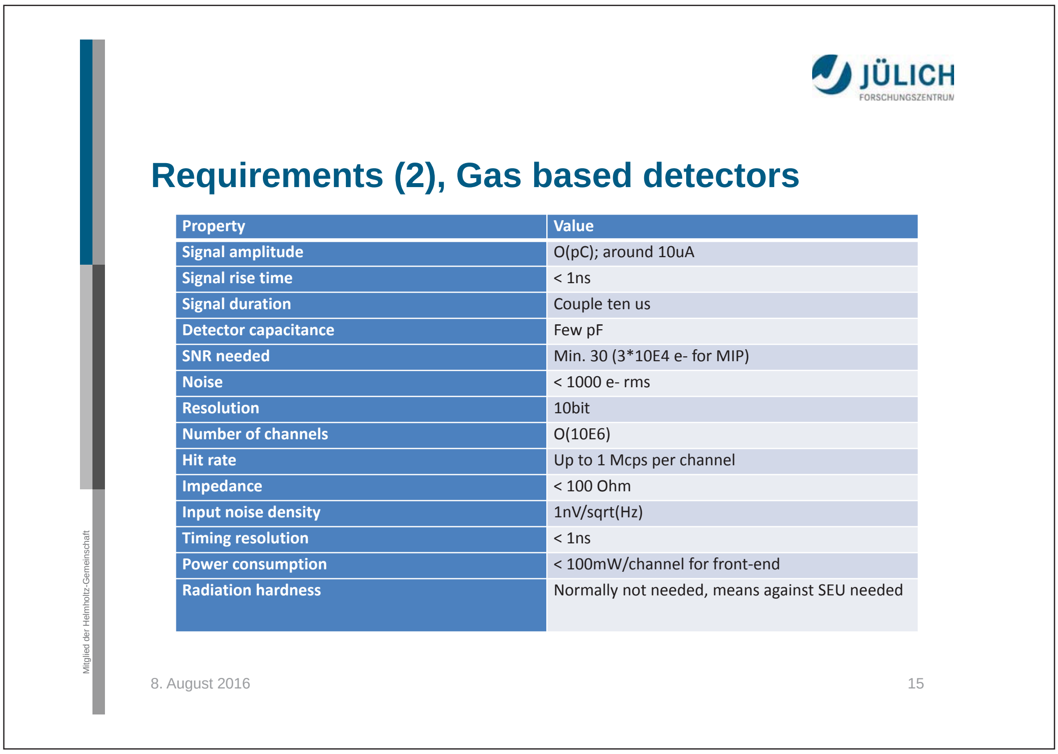
- Silicon pixel detector
- Silicon strip detector

© CERN / ATLAS



Requirements (1), Light detectors

Property	Value
Signal amplitude	Total charge up to nC (fC for APDs), few ten mA (over couple hundred nanoseconds)
Signal rise time	Around/below 1ns
Signal duration	Depends on scintillator (few ns up to few us)
Detector capacitance	Couple pF to few hundred pF (large APDs)
Linearity	< 1% (<0.1% for high resolution)
Noise	Up to 1uA dark current; couple 1.000 e- rms noise OK
Resolution	12 bit (10 ENOB)
Dynamic range	Up to 16 bits (multiple gain ranges)
Number of channels	O(10E5)
Hit rate	Up to 1 Mcps per channel
Radiation hardness	Up to 0.5 Mrad



Requirements (2), Gas based detectors

Property	Value
Signal amplitude	O(pC); around 10uA
Signal rise time	< 1ns
Signal duration	Couple ten us
Detector capacitance	Few pF
SNR needed	Min. 30 (3*10E4 e- for MIP)
Noise	< 1000 e- rms
Resolution	10bit
Number of channels	O(10E6)
Hit rate	Up to 1 Mcps per channel
Impedance	< 100 Ohm
Input noise density	1nV/sqrt(Hz)
Timing resolution	< 1ns
Power consumption	< 100mW/channel for front-end
Radiation hardness	Normally not needed, means against SEU needed

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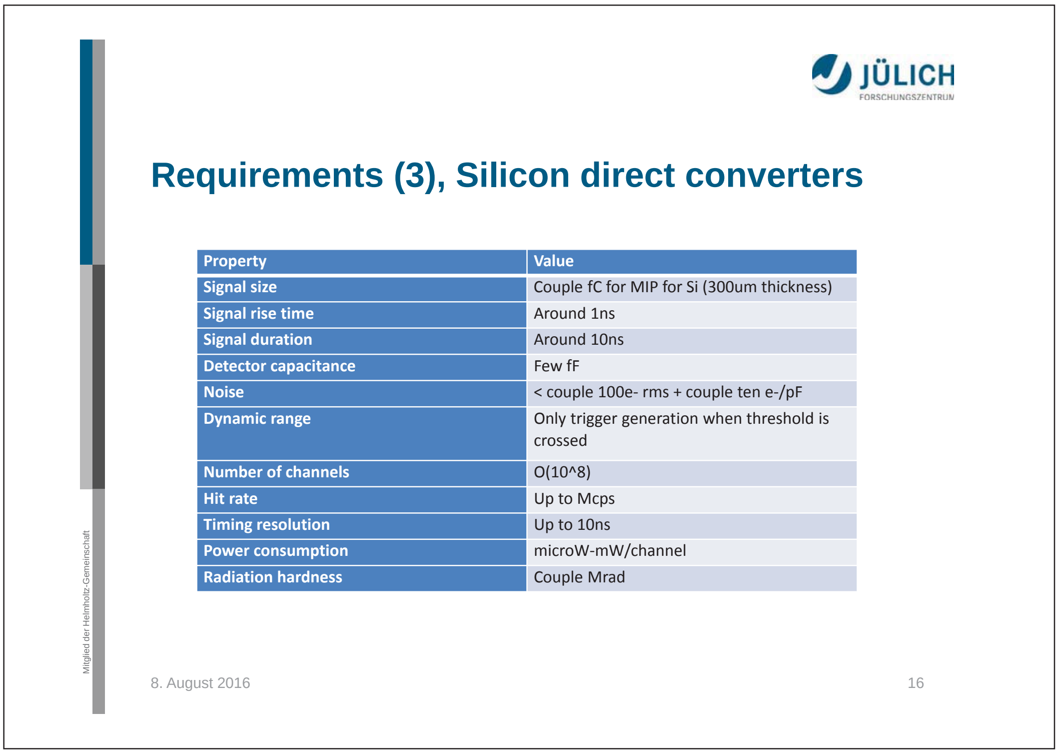

Requirements (3), Silicon direct converters

Property	Value
Signal size	Couple fC for MIP for Si (300um thickness)
Signal rise time	Around 1ns
Signal duration	Around 10ns
Detector capacitance	Few fF
Noise	< couple 100e- rms + couple ten e-/pF
Dynamic range	Only trigger generation when threshold is crossed
Number of channels	O(10^8)
Hit rate	Up to Mcps
Timing resolution	Up to 10ns
Power consumption	microW-mW/channel
Radiation hardness	Couple Mrad

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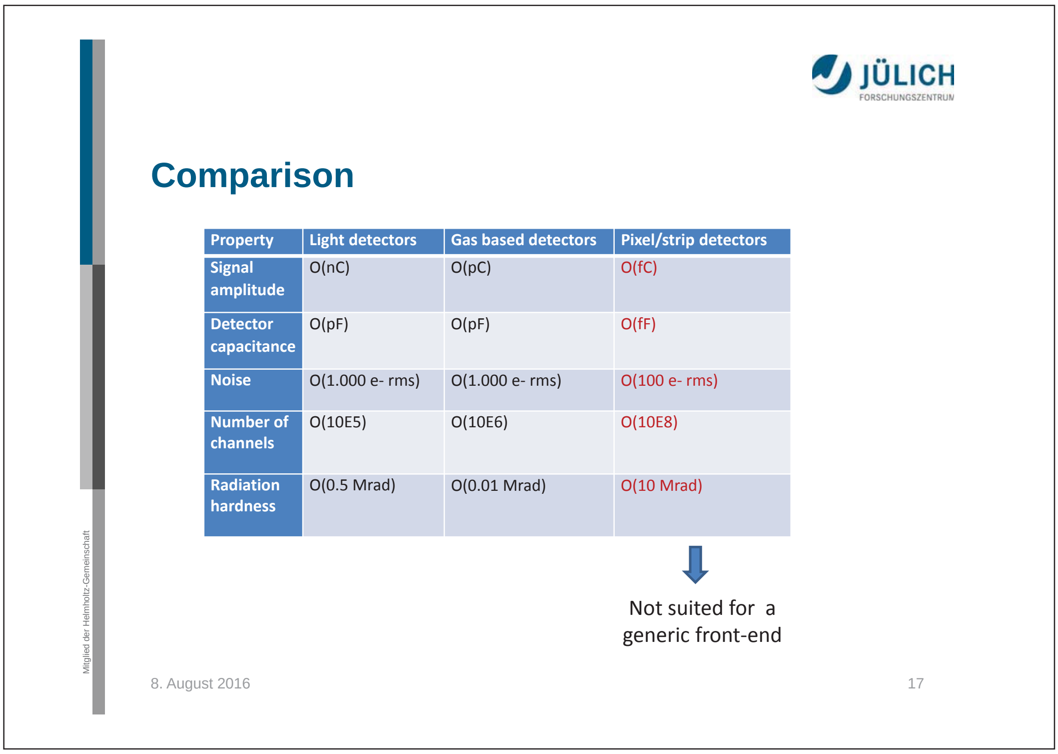
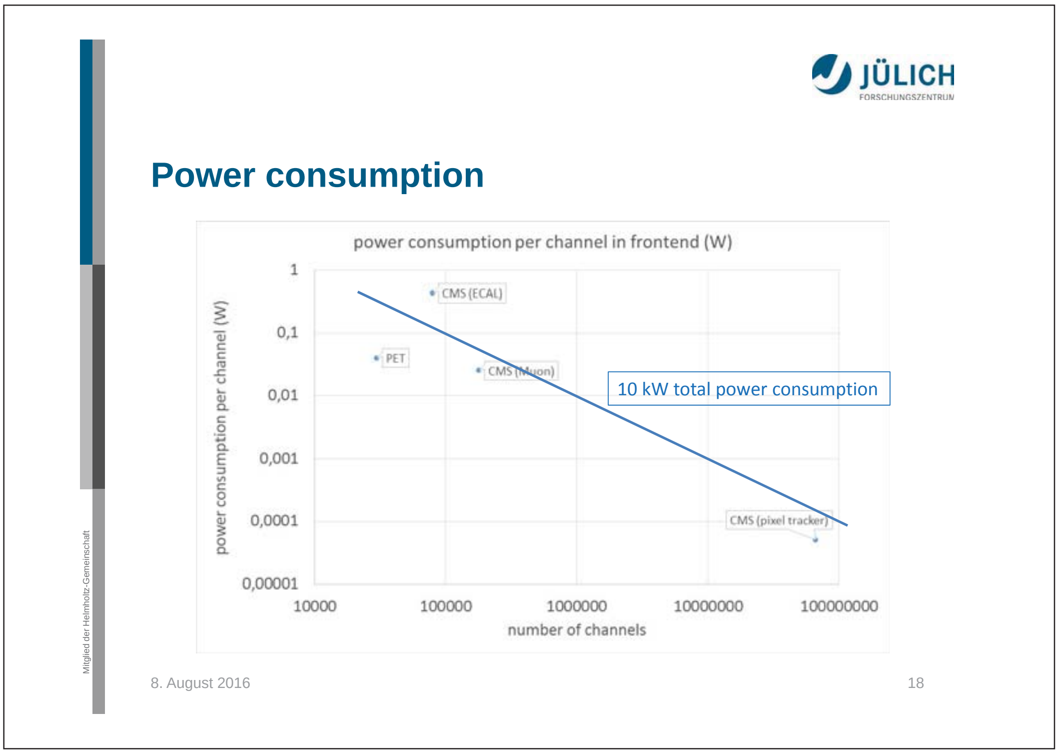


Comparison

Property	Light detectors	Gas based detectors	Pixel/strip detectors
Signal amplitude	O(nC)	O(pC)	O(fC)
Detector capacitance	O(pF)	O(pF)	O(fF)
Noise	O(1.000 e- rms)	O(1.000 e- rms)	O(100 e- rms)
Number of channels	O(10E5)	O(10E6)	O(10E8)
Radiation hardness	O(0.5 Mrad)	O(0.01 Mrad)	O(10 Mrad)

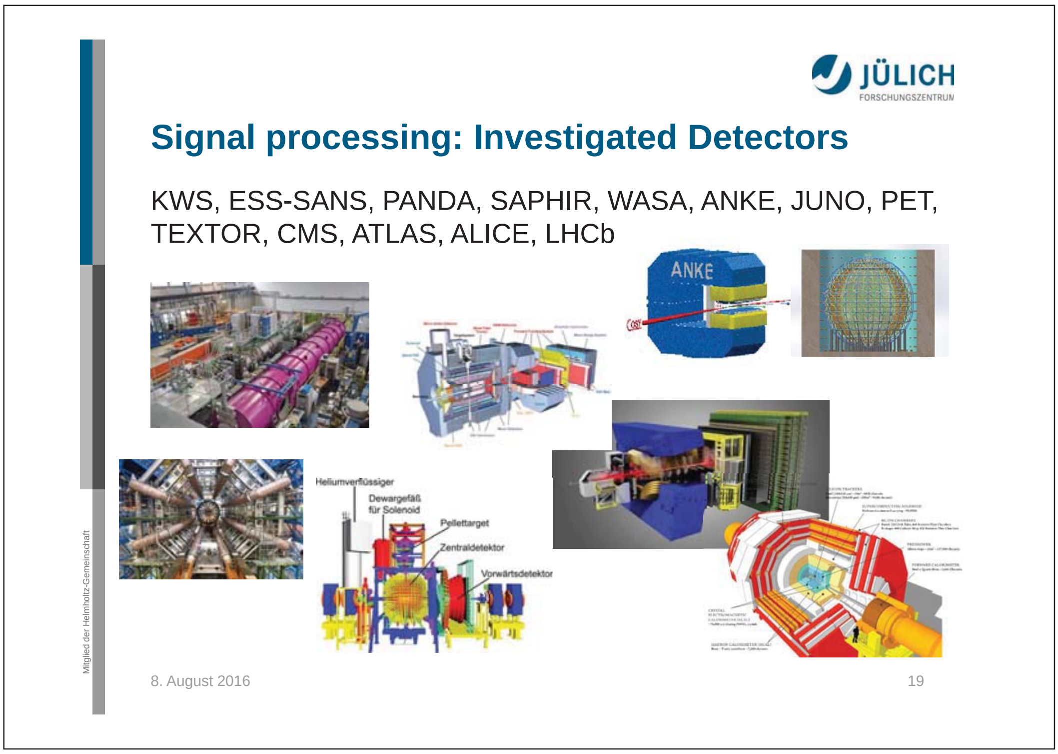
⇩

Not suited for a
generic front-end



Power consumption

10 kW total power consumption

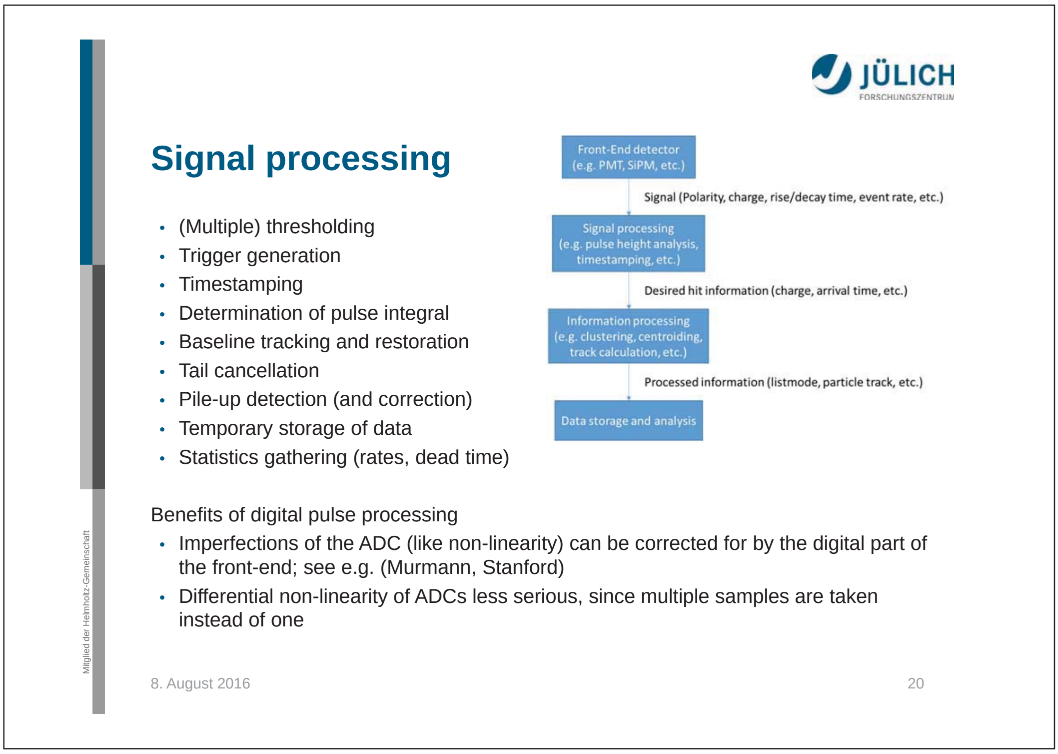


JÜLICH
FORSCHUNGSZENTRUM

Signal processing: Investigated Detectors

KWS, ESS-SANS, PANDA, SAPHIR, WASA, ANKE, JUNO, PET, TEXTOR, CMS, ATLAS, ALICE, LHCb

Mitglied der Helmholtz-Gemeinschaft



JÜLICH
FORSCHUNGSZENTRUM

Signal processing

- (Multiple) thresholding
- Trigger generation
- Timestamping
- Determination of pulse integral
- Baseline tracking and restoration
- Tail cancellation
- Pile-up detection (and correction)
- Temporary storage of data
- Statistics gathering (rates, dead time)

Front-End detector (e.g. PMT, SiPM, etc.)

Signal (Polarity, charge, rise/decay time, event rate, etc.)

Signal processing (e.g. pulse height analysis, timestamping, etc.)

Desired hit information (charge, arrival time, etc.)

Information processing (e.g. clustering, centroiding, track calculation, etc.)

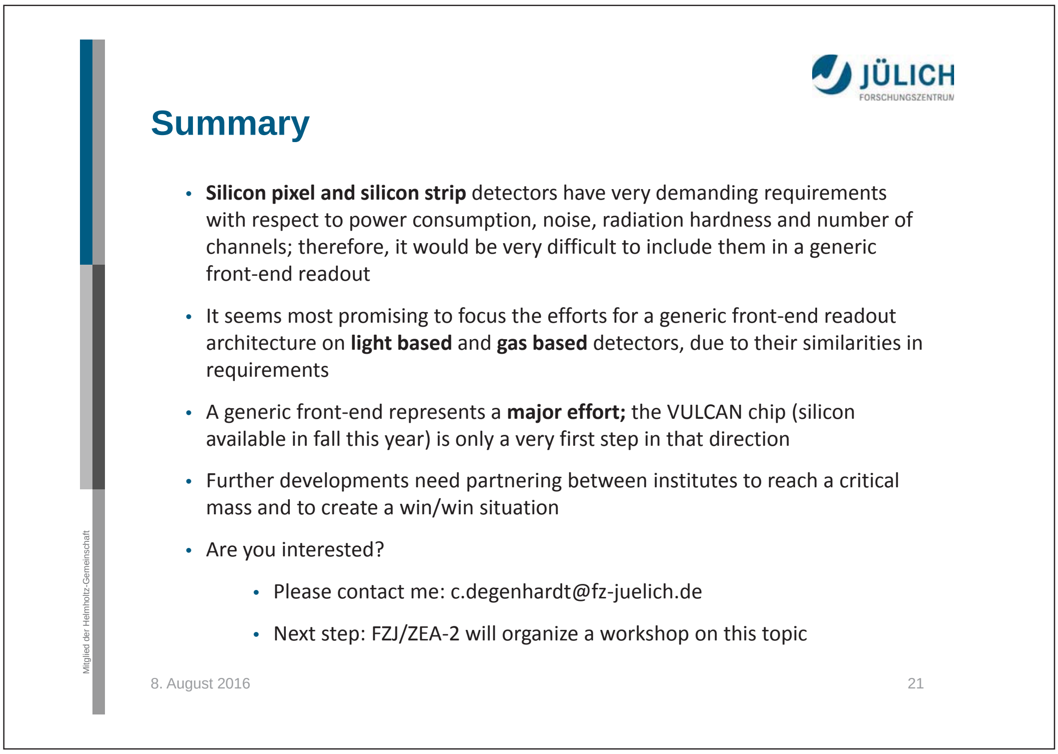
Processed information (listmode, particle track, etc.)

Data storage and analysis

Benefits of digital pulse processing

- Imperfections of the ADC (like non-linearity) can be corrected for by the digital part of the front-end; see e.g. (Murmann, Stanford)
- Differential non-linearity of ADCs less serious, since multiple samples are taken instead of one

Mitglied der Helmholtz-Gemeinschaft



Summary

- **Silicon pixel and silicon strip** detectors have very demanding requirements with respect to power consumption, noise, radiation hardness and number of channels; therefore, it would be very difficult to include them in a generic front-end readout
- It seems most promising to focus the efforts for a generic front-end readout architecture on **light based** and **gas based** detectors, due to their similarities in requirements
- A generic front-end represents a **major effort;** the VULCAN chip (silicon available in fall this year) is only a very first step in that direction
- Further developments need partnering between institutes to reach a critical mass and to create a win/win situation
- Are you interested?
  - Please contact me: c.degenhardt@fz-juelich.de
  - Next step: FZJ/ZEA-2 will organize a workshop on this topic

8. August 2016 21

Thank You for Your Attention!

SEI-Tagung, GSI, March 2016

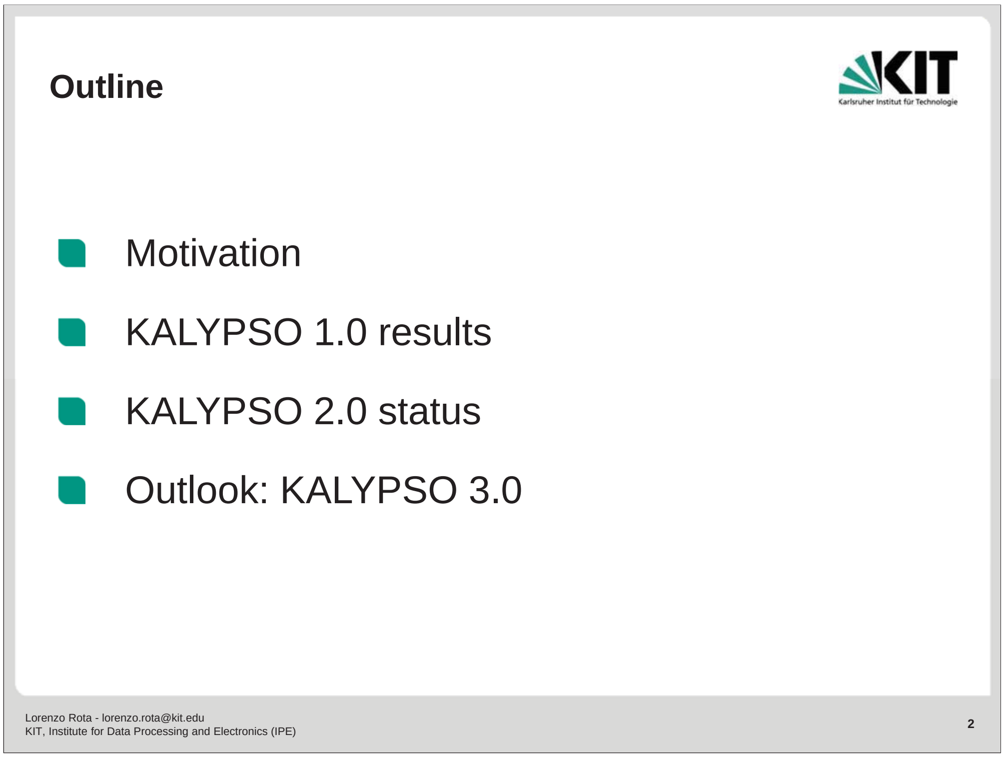
KALYPSO: a novel detection system for Single-Shot Electro-Optical bunch measurements

L. Rota, M. Balzer, M. Caselle, N. Hiller, A. Mozzanica, G. Niehues, M. J. Nasse,
P. Schönfeldt, S. Walther, M. Weber

KIT, Institute for Data Processing and Electronics (IPE)

KIT – Universität des Landes Baden-Württemberg und
nationales Forschungszentrum in der Helmholtz-Gemeinschaft

www.kit.edu



Outline

- Motivation
- KALYPSO 1.0 results
- KALYPSO 2.0 status
- Outlook: KALYPSO 3.0

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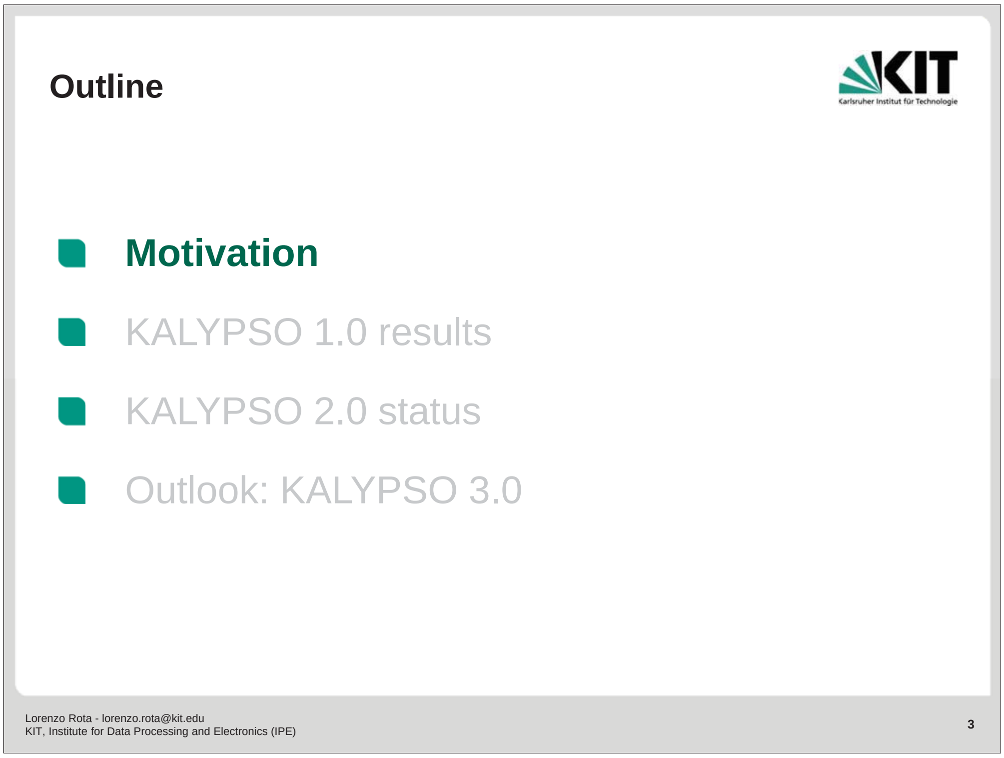
2



Outline

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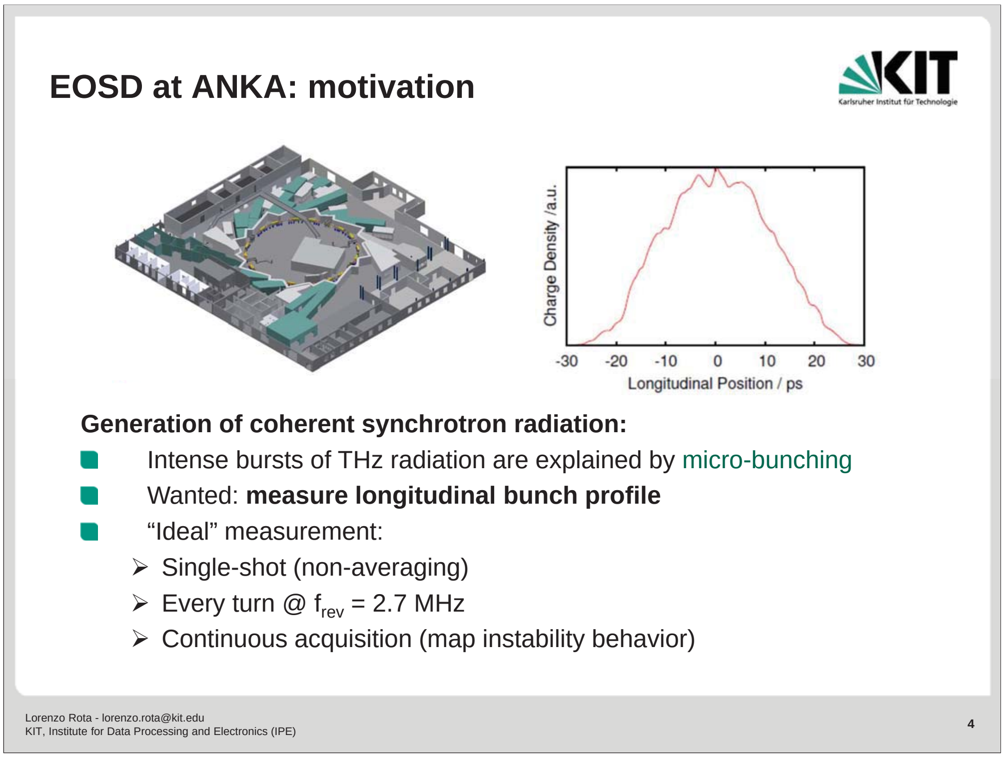
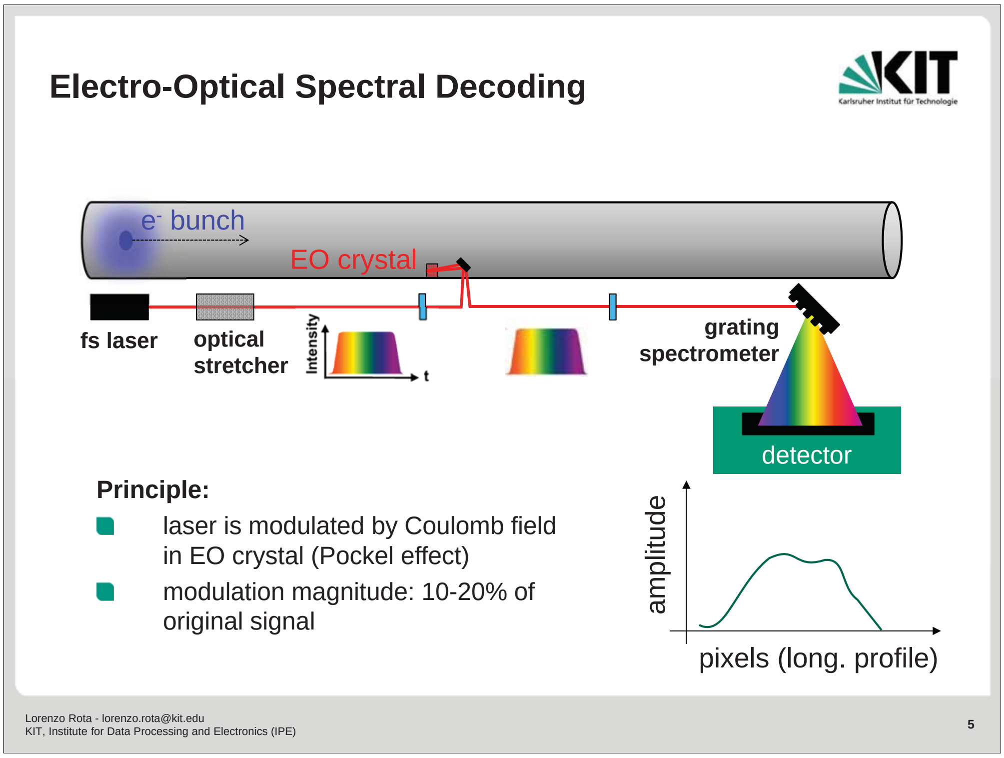


EOSD at ANKA: motivation

Generation of coherent synchrotron radiation:

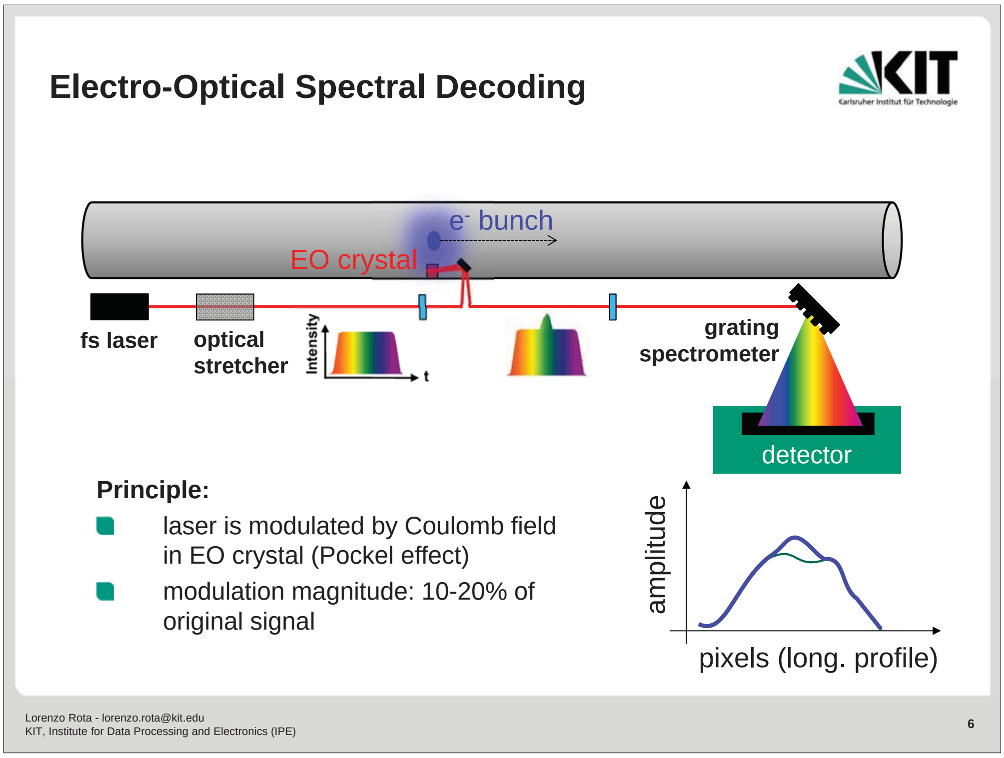
- Intense bursts of THz radiation are explained by micro-bunching
- Wanted: **measure longitudinal bunch profile**
- "Ideal" measurement:
  - Single-shot (non-averaging)
  - Every turn @ f_{rev} = 2.7 MHz
  - Continuous acquisition (map instability behavior)



Electro-Optical Spectral Decoding

Principle:

- laser is modulated by Coulomb field in EO crystal (Pockel effect)
- modulation magnitude: 10-20% of original signal



Electro-Optical Spectral Decoding

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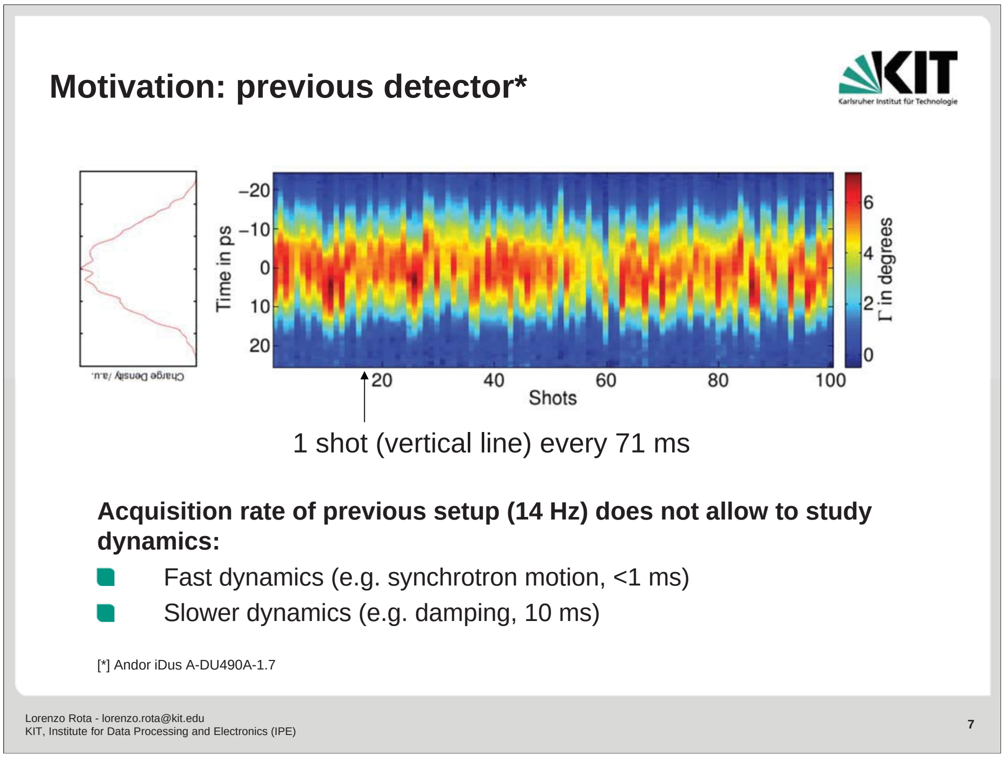

Motivation: previous detector*

1 shot (vertical line) every 71 ms

Acquisition rate of previous setup (14 Hz) does not allow to study dynamics:

- Fast dynamics (e.g. synchrotron motion, <1 ms)
- Slower dynamics (e.g. damping, 10 ms)

[*] Andor iDus A-DU490A-1.7

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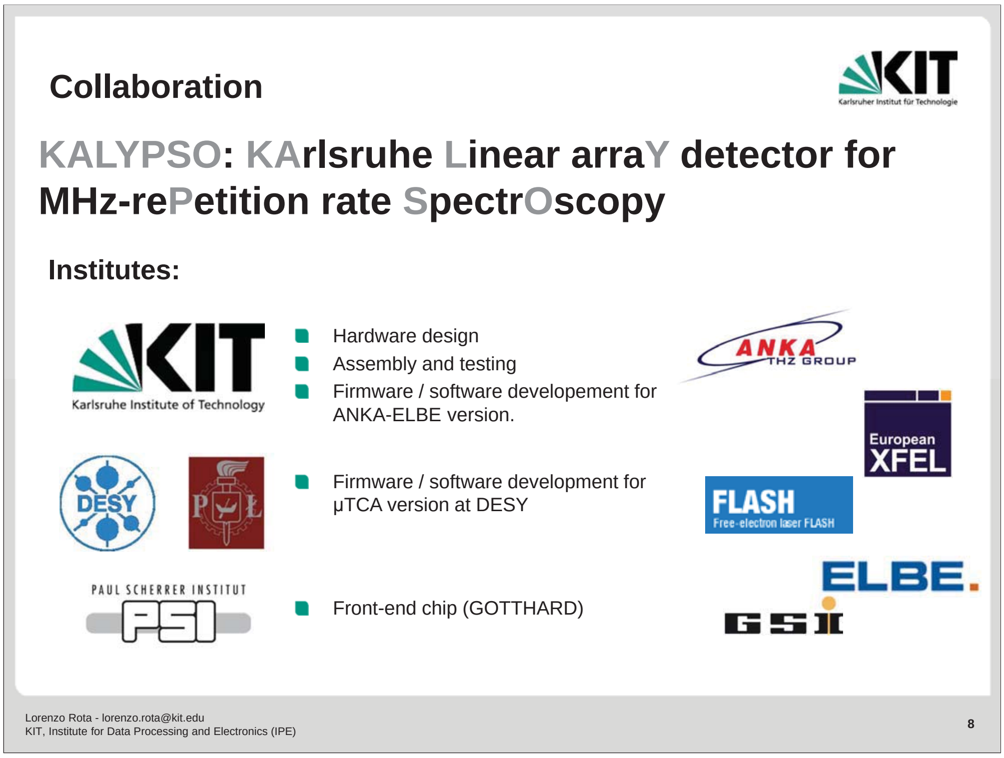

Collaboration

KALYPSO: KArlsruhe Linear arraY detector for MHz-rePetition rate SpectrOscopy

Institutes:

- Hardware design
- Assembly and testing
- Firmware / software developement for ANKA-ELBE version.

- Firmware / software development for µTCA version at DESY

- Front-end chip (GOTTHARD)

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Outline

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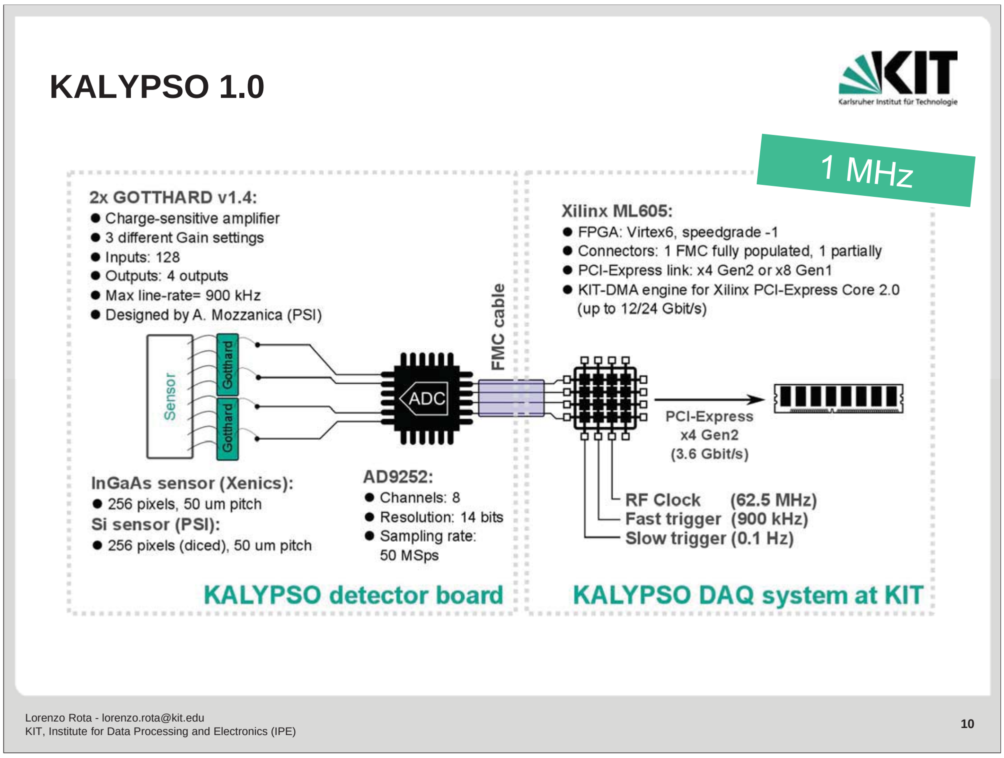


KALYPSO 1.0

1 MHz

2x GOTTHARD v1.4:
- Charge-sensitive amplifier
- 3 different Gain settings
- Inputs: 128
- Outputs: 4 outputs
- Max line-rate= 900 kHz
- Designed by A. Mozzanica (PSI)

InGaAs sensor (Xenics):
- 256 pixels, 50 um pitch

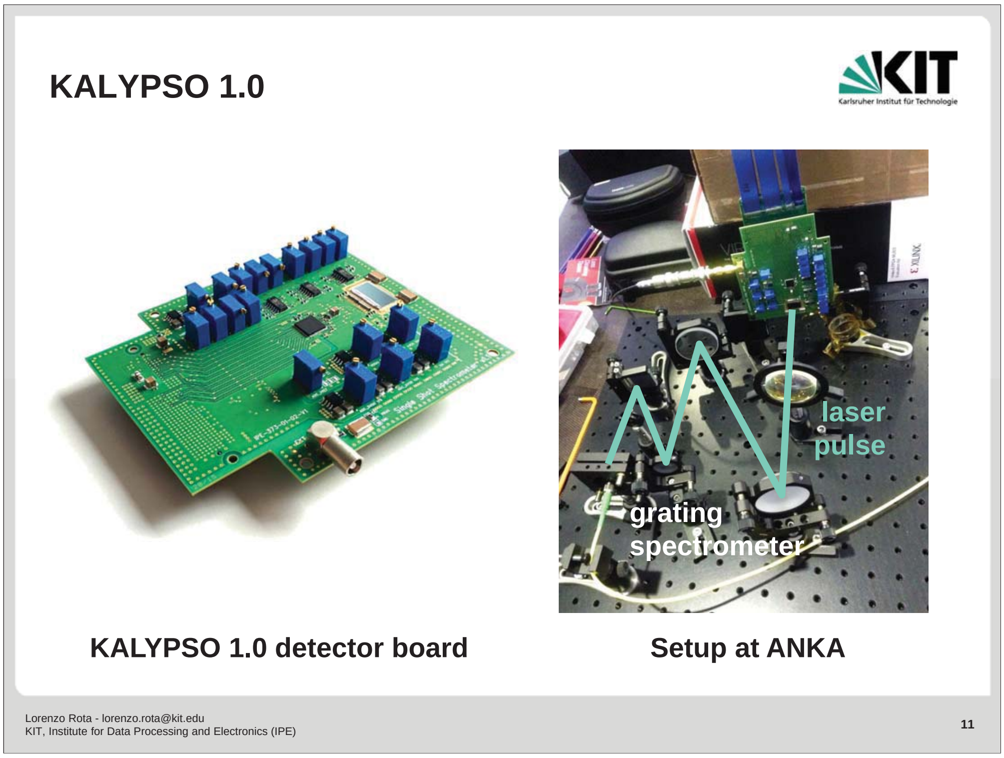
Si sensor (PSI):
- 256 pixels (diced), 50 um pitch

AD9252:
- Channels: 8
- Resolution: 14 bits
- Sampling rate: 50 MSps

KALYPSO detector board

Xilinx ML605:
- FPGA: Virtex6, speedgrade -1
- Connectors: 1 FMC fully populated, 1 partially
- PCI-Express link: x4 Gen2 or x8 Gen1
- KIT-DMA engine for Xilinx PCI-Express Core 2.0 (up to 12/24 Gbit/s)

KALYPSO DAQ system at KIT



KALYPSO 1.0

KALYPSO 1.0 detector board

Setup at ANKA

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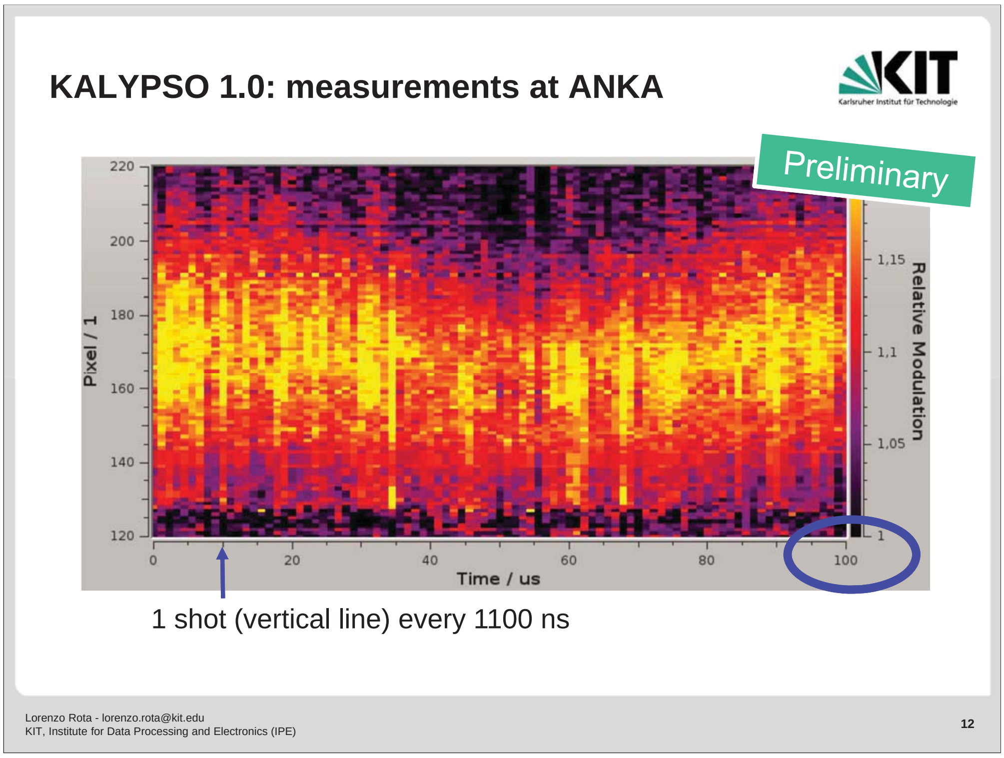

KALYPSO 1.0: measurements at ANKA

1 shot (vertical line) every 1100 ns

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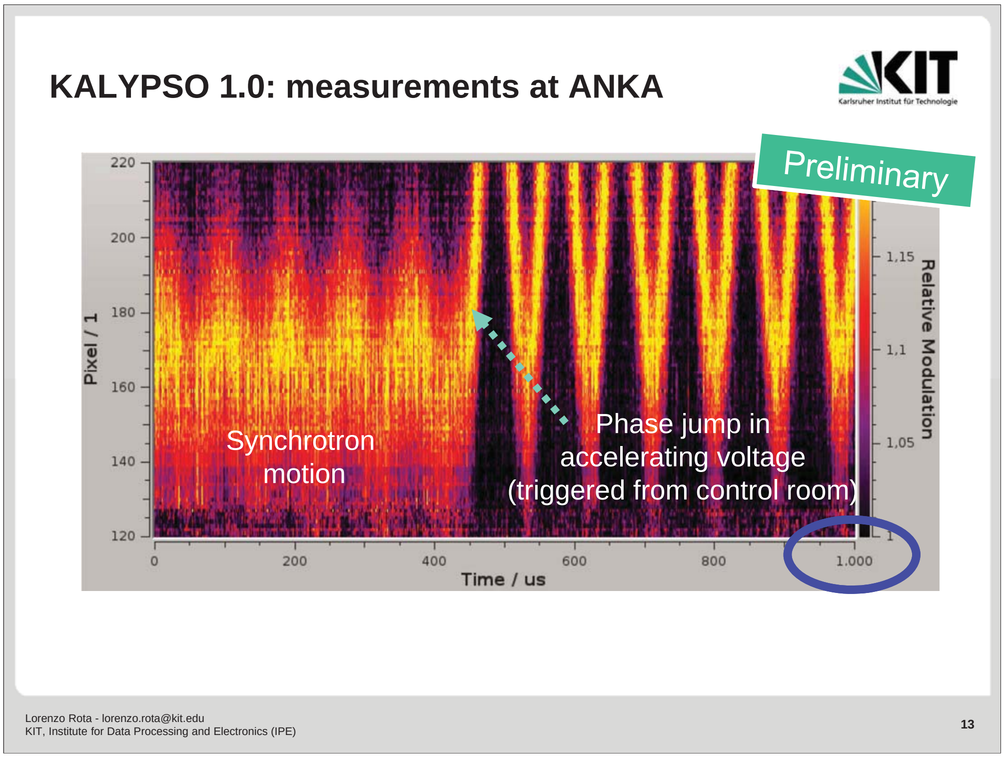

KALYPSO 1.0: measurements at ANKA

Preliminary

Synchrotron motion

Phase jump in accelerating voltage (triggered from control room)

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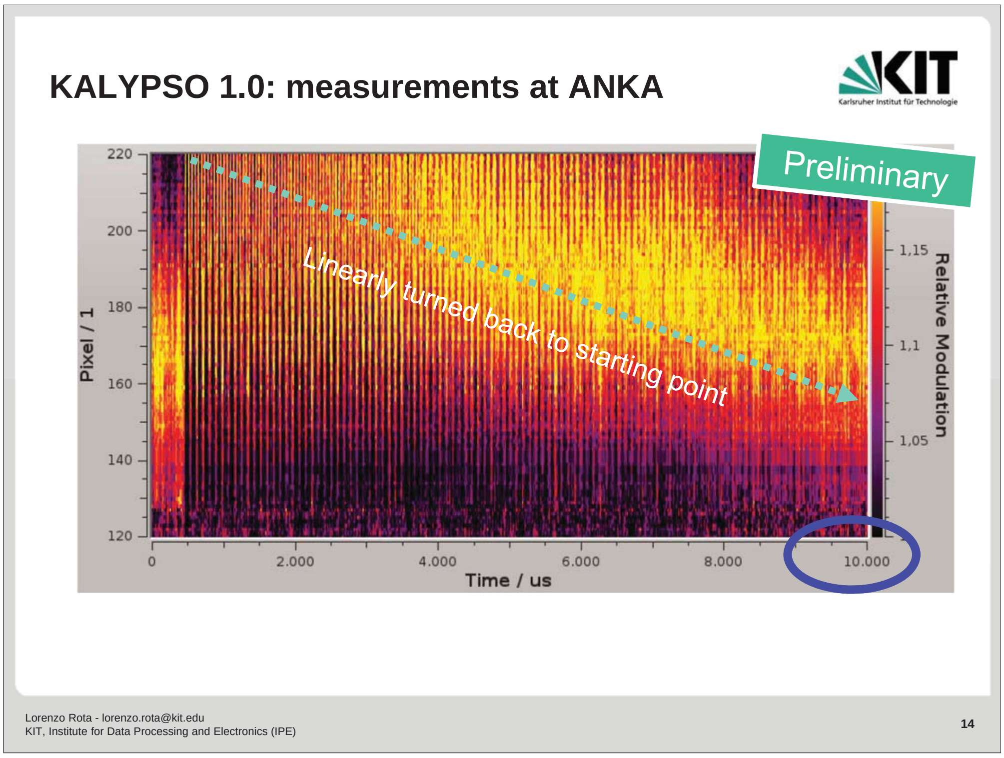

KALYPSO 1.0: measurements at ANKA

Preliminary

Linearly turned back to starting point

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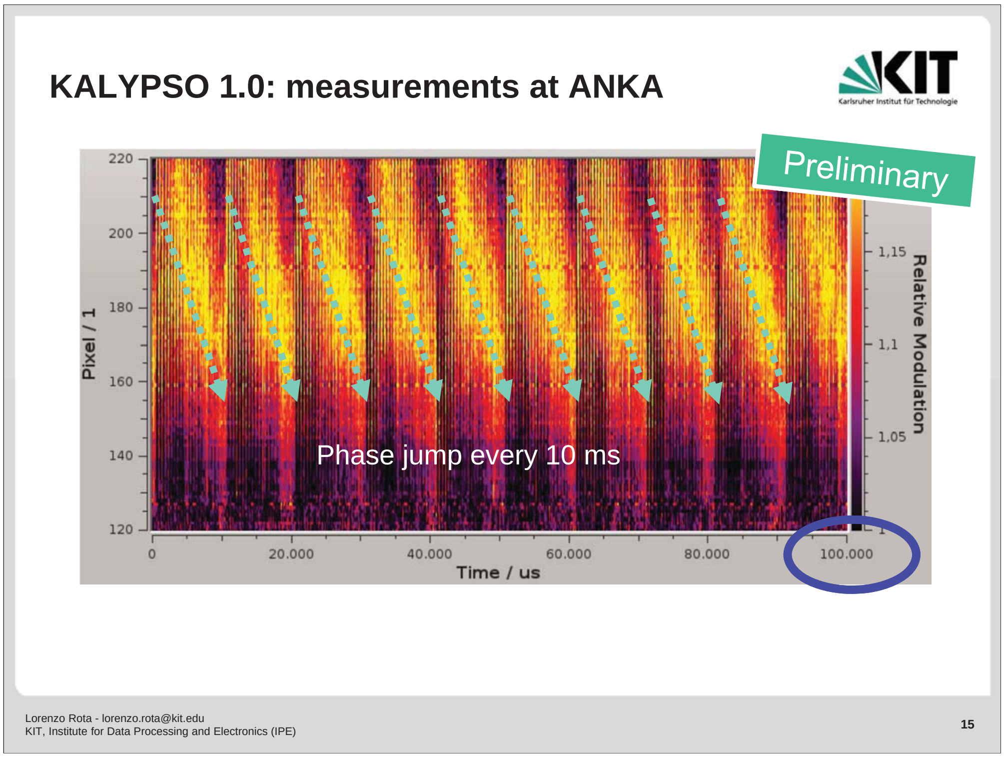
14



KALYPSO 1.0: measurements at ANKA

Preliminary

Phase jump every 10 ms

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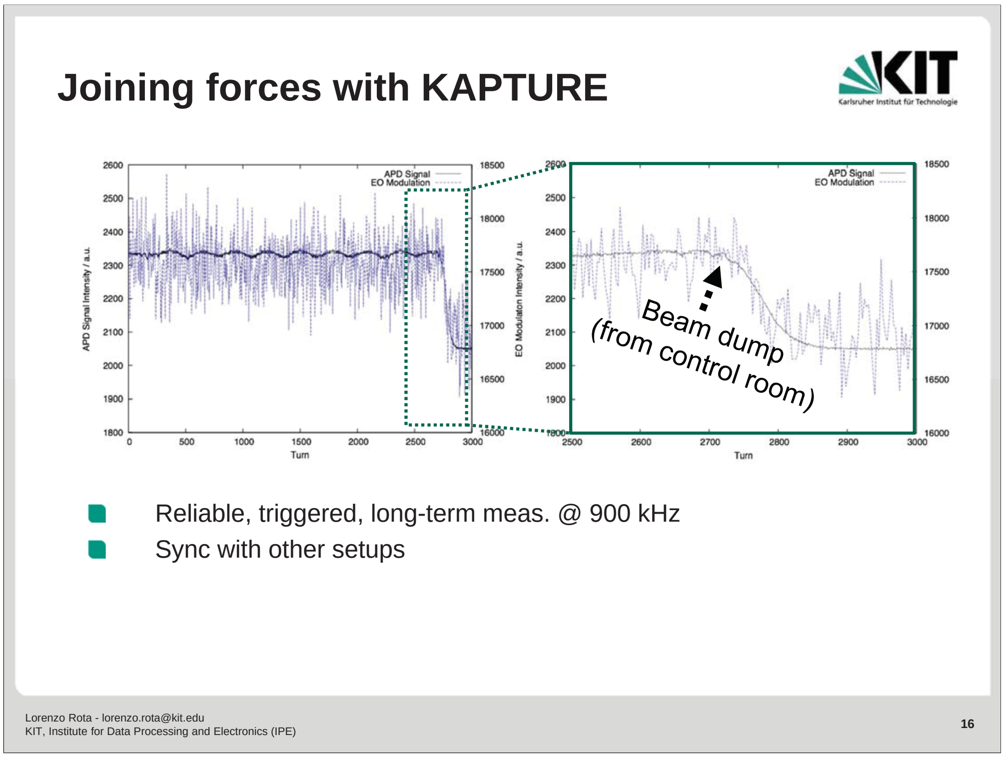

Joining forces with KAPTURE

Beam dump
(from control room)

- Reliable, triggered, long-term meas. @ 900 kHz
- Sync with other setups

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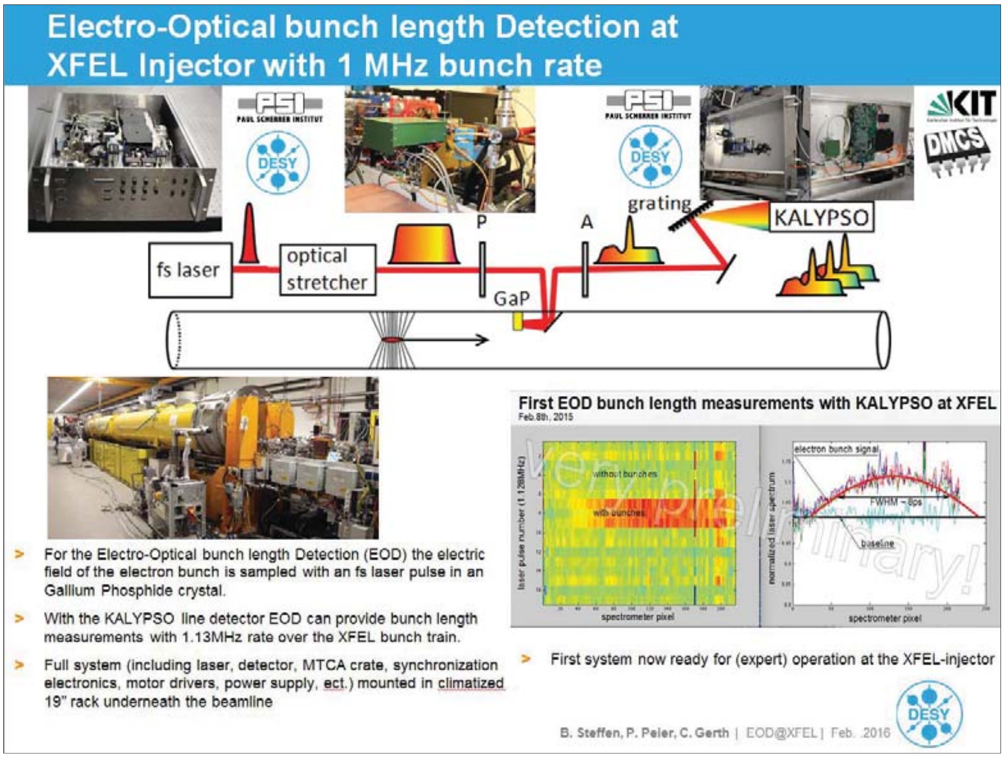
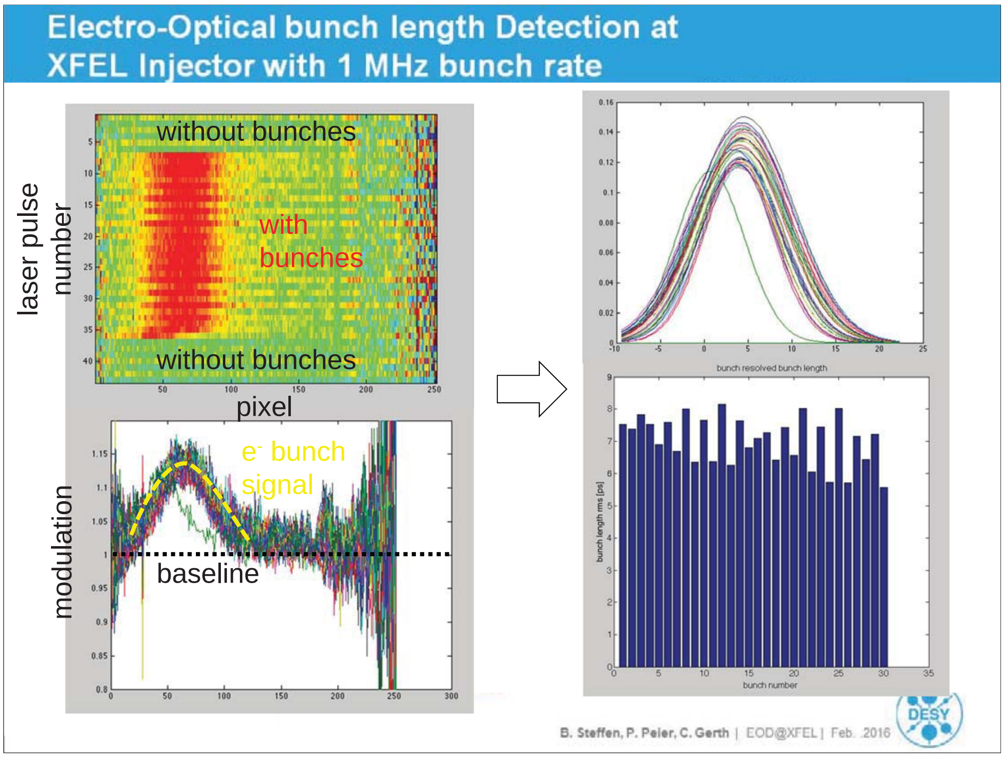


Electro-Optical bunch length Detection at XFEL Injector with 1 MHz bunch rate

- For the Electro-Optical bunch length Detection (EOD) the electric field of the electron bunch is sampled with an fs laser pulse in an Gallium Phosphide crystal.
- With the KALYPSO line detector EOD can provide bunch length measurements with 1.13MHz rate over the XFEL bunch train.
- Full system (including laser, detector, MTCA crate, synchronization electronics, motor drivers, power supply, ect.) mounted in climatized 19" rack underneath the beamline
- First system now ready for (expert) operation at the XFEL-injector

B. Steffen, P. Peier, C. Gerth | EOD@XFEL | Feb. 2016



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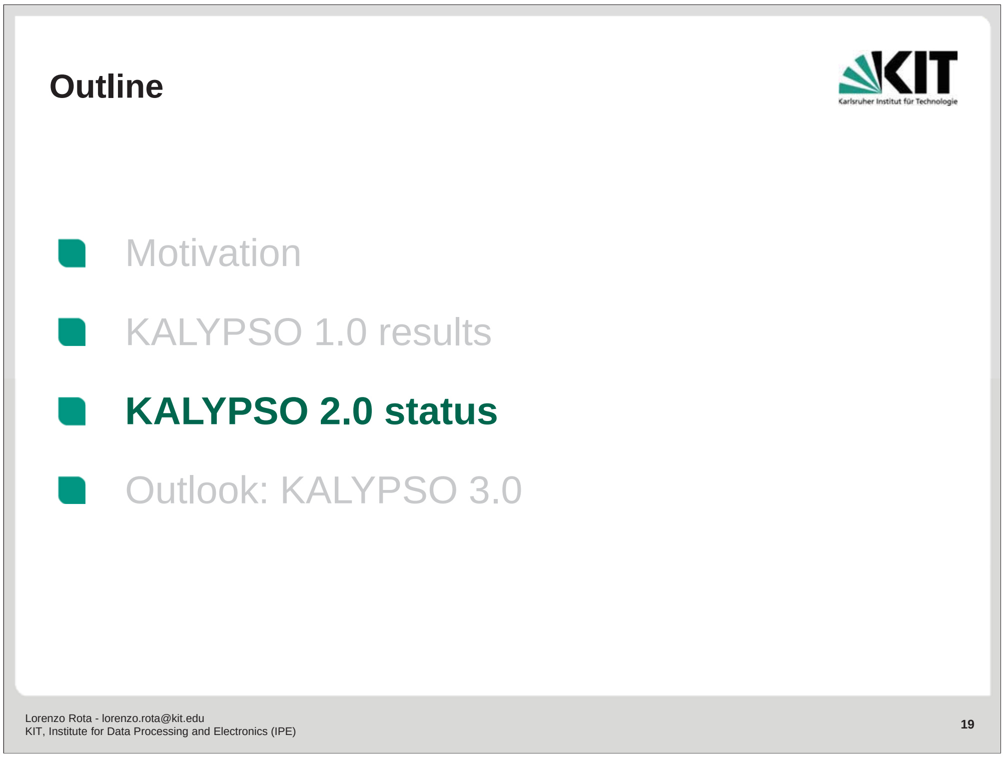

Outline

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- KALYPSO 1.0 results
- **KALYPSO 2.0 status**
- Outlook: KALYPSO 3.0

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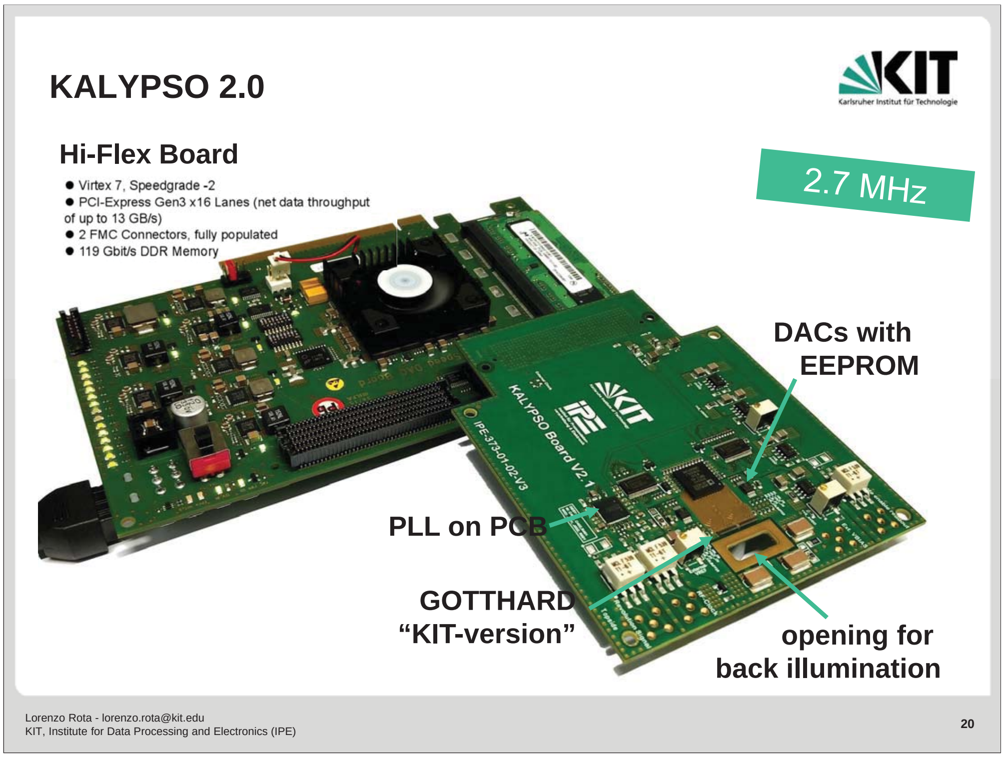

KALYPSO 2.0

Hi-Flex Board

- Virtex 7, Speedgrade -2
- PCI-Express Gen3 x16 Lanes (net data throughput of up to 13 GB/s)
- 2 FMC Connectors, fully populated
- 119 Gbit/s DDR Memory

2.7 MHz

DACs with EEPROM

PLL on PCB

GOTTHARD “KIT-version”

opening for back illumination

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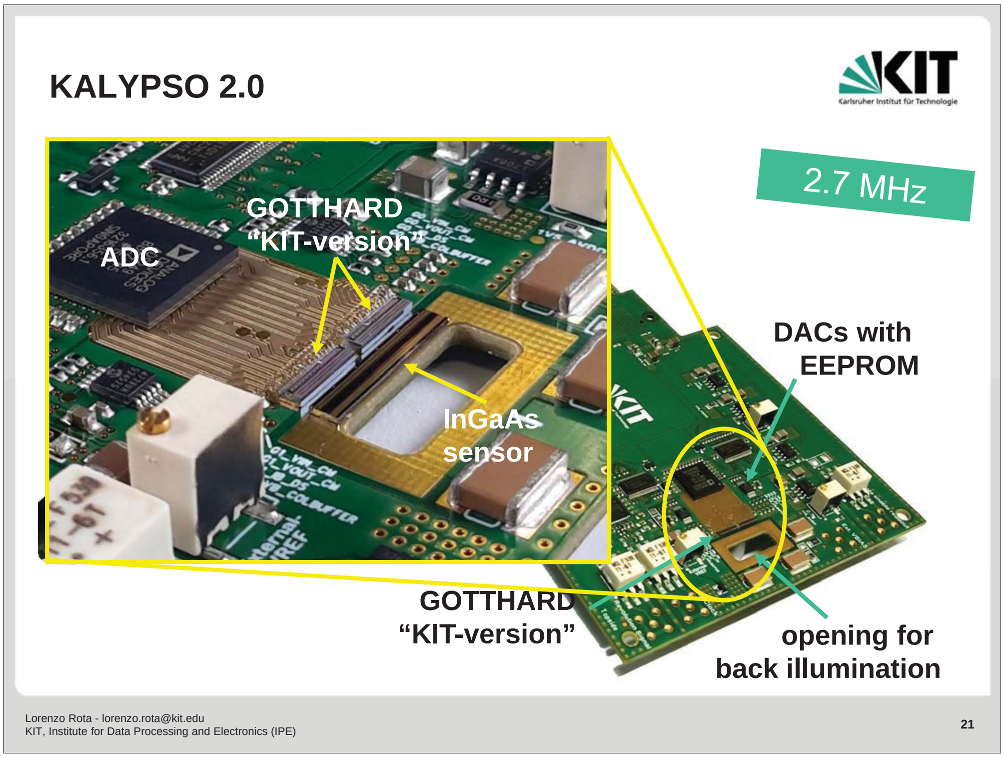

KALYPSO 2.0

2.7 MHz

ADC

GOTTHARD
“KIT-version”

InGaAs
sensor

DACs with
EEPROM

GOTTHARD
“KIT-version”

opening for
back illumination

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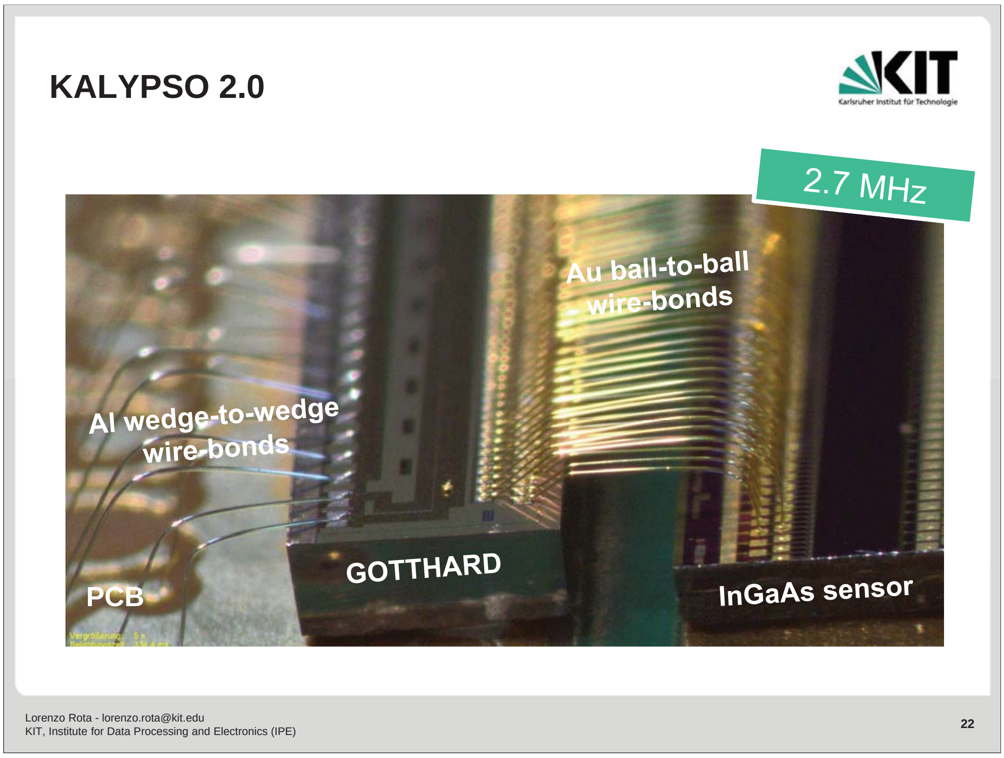

KALYPSO 2.0

2.7 MHz

Au ball-to-ball
wire-bonds

Al wedge-to-wedge
wire-bonds

GOTTHARD

PCB

InGaAs sensor

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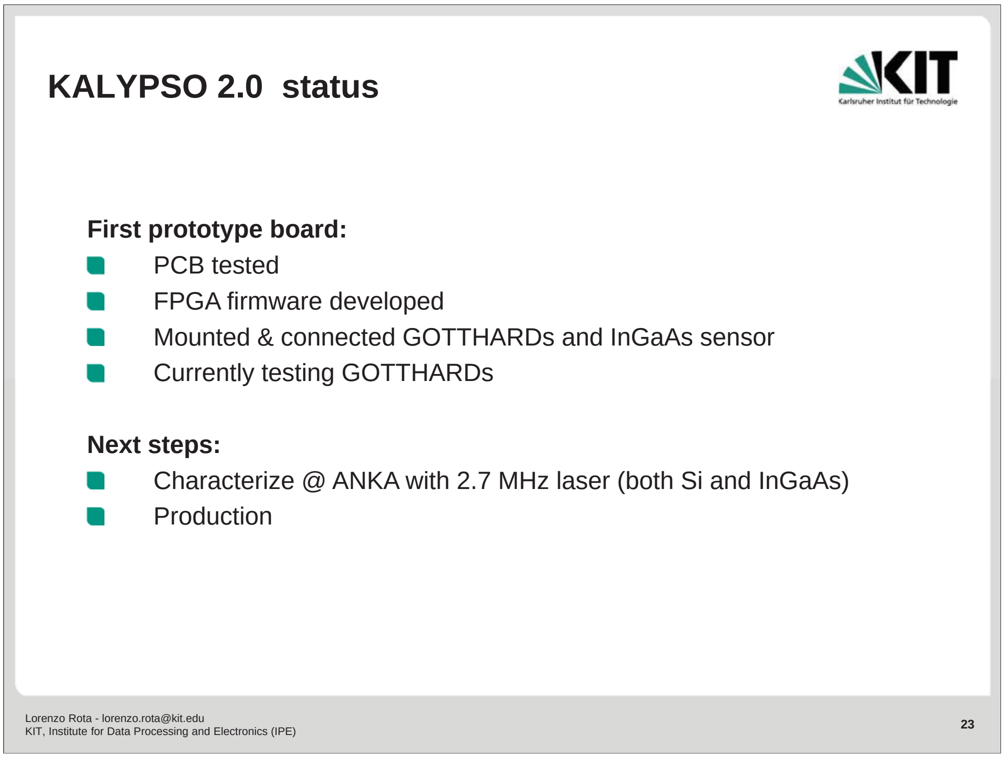


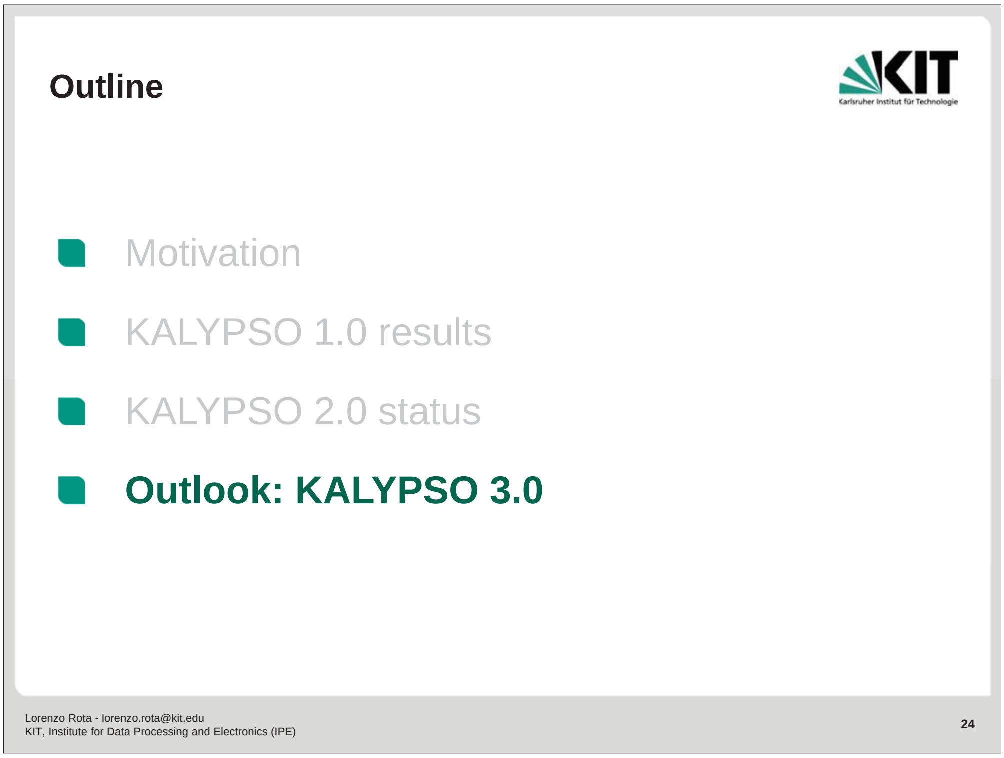
KALYPSO 2.0 status

First prototype board:

- PCB tested
- FPGA firmware developed
- Mounted & connected GOTTHARDs and InGaAs sensor
- Currently testing GOTTHARDs

Next steps:

- Characterize @ ANKA with 2.7 MHz laser (both Si and InGaAs)
- Production



Outline

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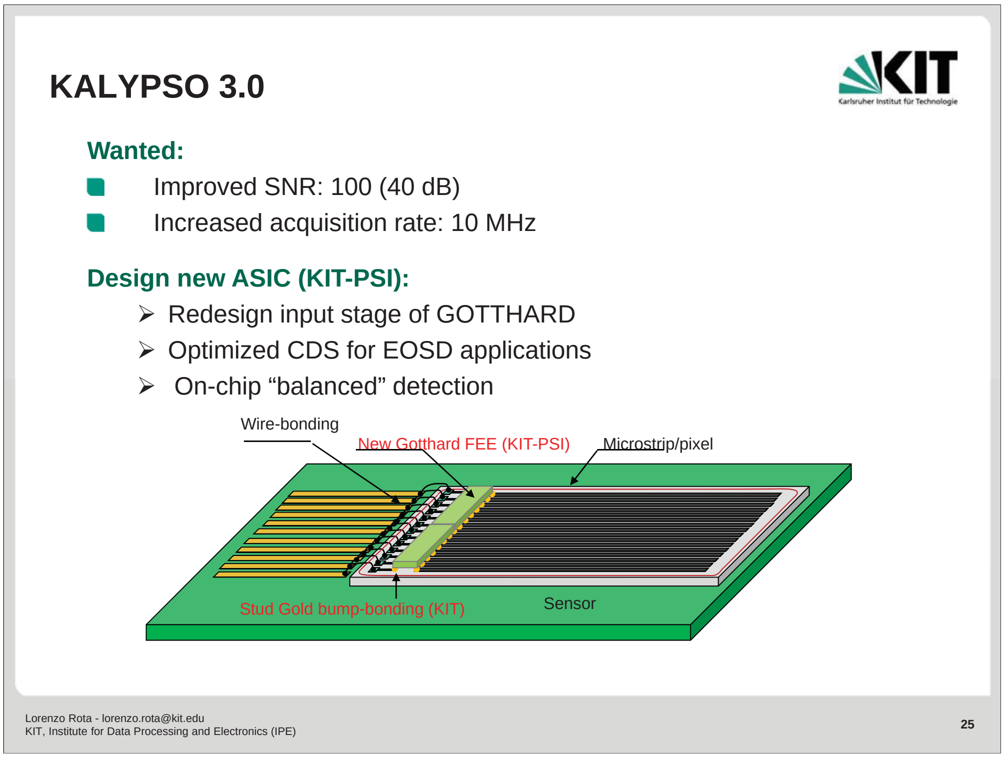
- **Outlook: KALYPSO 3.0**



KALYPSO 3.0

Wanted:

- Improved SNR: 100 (40 dB)
- Increased acquisition rate: 10 MHz

Design new ASIC (KIT-PSI):

- ➢ Redesign input stage of GOTTHARD
- ➢ Optimized CDS for EOSD applications
- ➢ On-chip “balanced” detection

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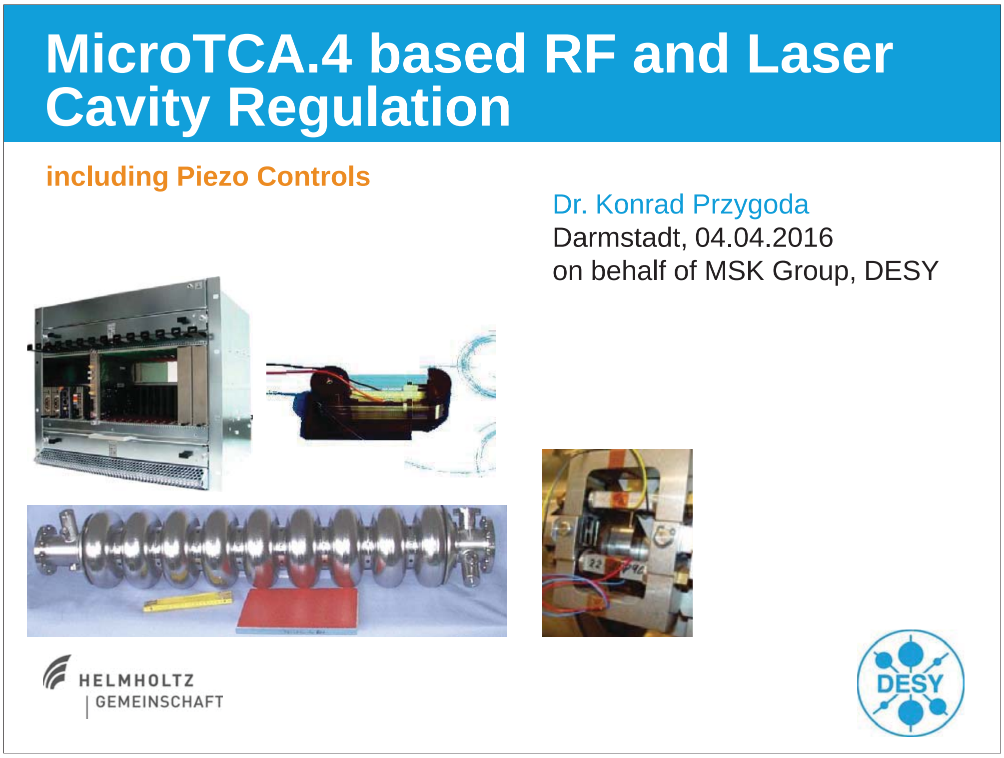
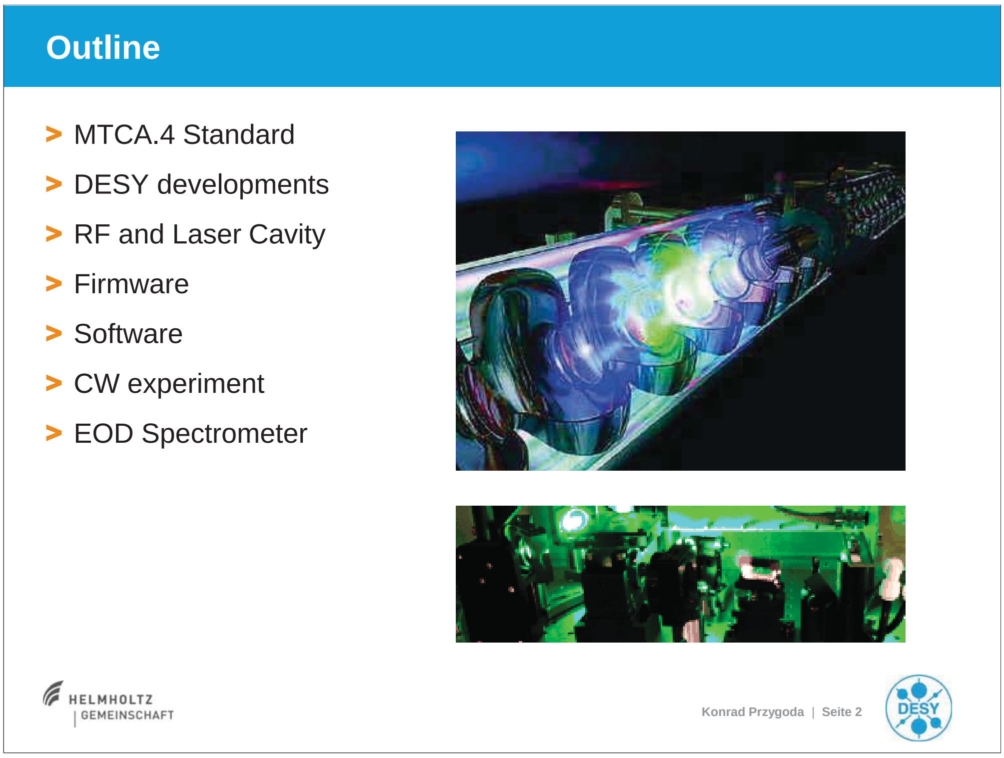


MicroTCA.4 based RF and Laser Cavity Regulation

including Piezo Controls

Dr. Konrad Przygoda
Darmstadt, 04.04.2016
on behalf of MSK Group, DESY

HELMHOLTZ
GEMEINSCHAFT



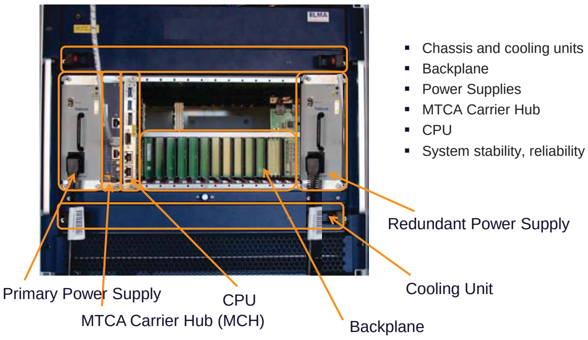
Outline

- MTCA.4 Standard
- DESY developments
- RF and Laser Cavity
- Firmware
- Software
- CW experiment
- EOD Spectrometer

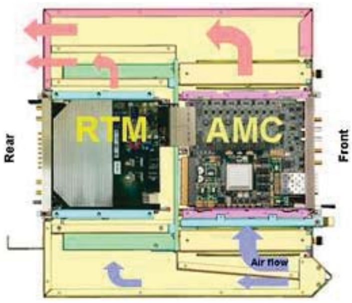
Konrad Przygoda | Seite 2

MTCA.4 Standard

- **Modular + modern architecture**
  - Reusability + PCIe + Ethernet
- **High availability**
  - Redundant power, MCH and CU
  - Well defined remote management
  - Hot plug support
- **High digital and analog performance**
  - Very low analog distortions (diff.lines)
  - 4 lanes PCIe (Gen3): 1 GByte/s/lane



- Chassis and cooling units
- Backplane
- Power Supplies
- MTCA Carrier Hub
- CPU
- System stability, reliability



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DESY-MSK Developments

- FMC carriers:
  - DAMC-FMC20
  - DAMC-FMC25
- FMC modules:
  - DFMC-MD22
  - DFMC-SFP4
  - DFMC-AD16
  - DFMC-UNIO
- Backplanes:
  - RF Backplane
- AMC
  - DAMC-TCK7
  - DAMC-DS800
- RTM
  - DRTM-DWC10
  - DRTM-DWC8VM1
  - DRTM-DS8VM1
  - DRTM-uLOG
  - DRTM-VM
  - DRTM-AD84
  - DRTM-PZT4

15 boards developed (industry licensed or direct sale), several more under development

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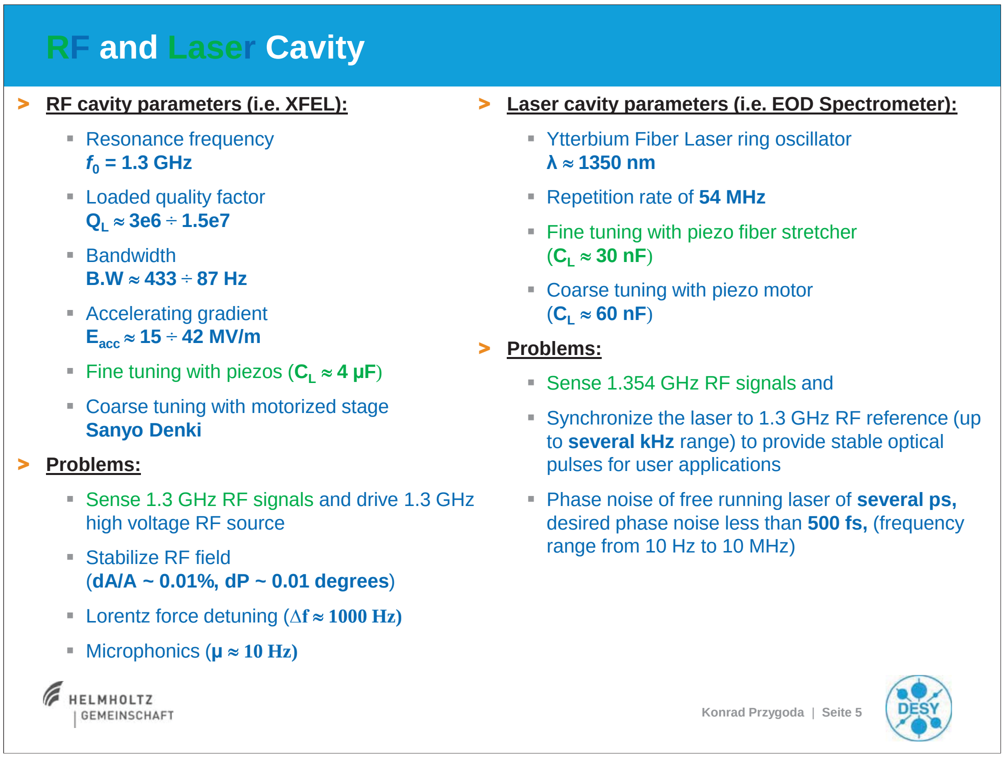
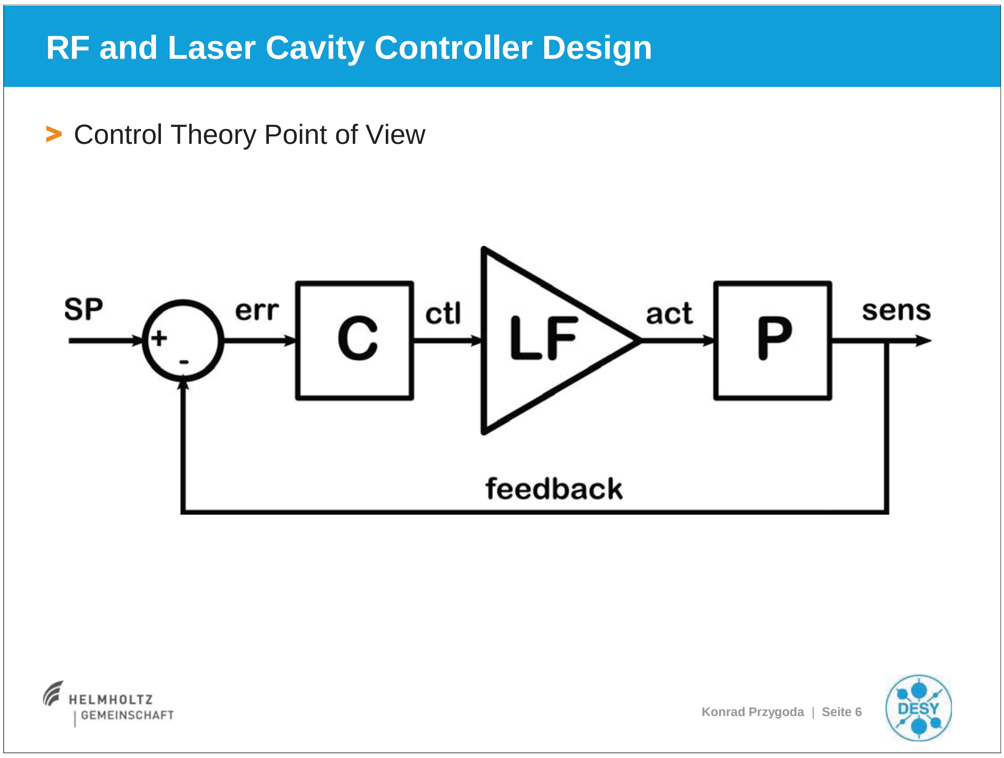


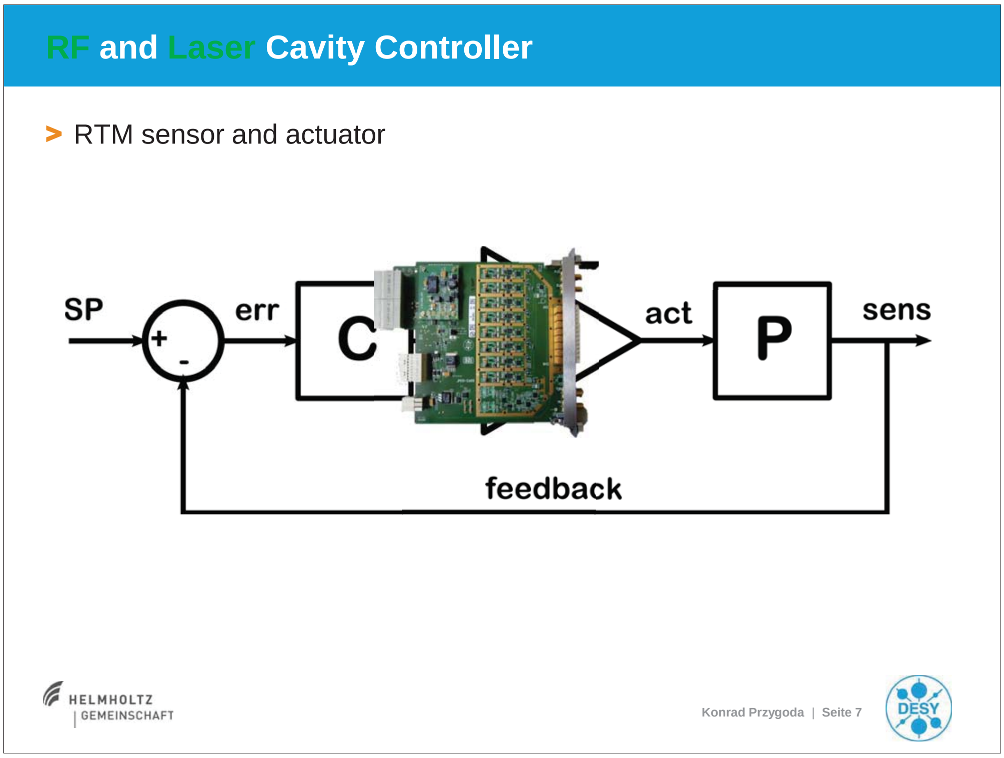
RF and Laser Cavity

- **RF cavity parameters (i.e. XFEL):**
  - Resonance frequency
f_0 = 1.3 GHz
  - Loaded quality factor
$Q_L \approx$ 3e6 ÷ 1.5e7
  - Bandwidth
B.W ≈ 433 ÷ 87 Hz
  - Accelerating gradient
$E_{acc} \approx$ 15 ÷ 42 MV/m
  - Fine tuning with piezos (**$C_L \approx$ 4 μF**)
  - Coarse tuning with motorized stage
Sanyo Denki
- **Problems:**
  - Sense 1.3 GHz RF signals and drive 1.3 GHz high voltage RF source
  - Stabilize RF field
(**dA/A ~ 0.01%, dP ~ 0.01 degrees**)
  - Lorentz force detuning (**Δf ≈ 1000 Hz**)
  - Microphonics (**μ ≈ 10 Hz**)
- **Laser cavity parameters (i.e. EOD Spectrometer):**
  - Ytterbium Fiber Laser ring oscillator
λ ≈ 1350 nm
  - Repetition rate of **54 MHz**
  - Fine tuning with piezo fiber stretcher
(**$C_L \approx$ 30 nF**)
  - Coarse tuning with piezo motor
(**$C_L \approx$ 60 nF**)
- **Problems:**
  - Sense 1.354 GHz RF signals and
  - Synchronize the laser to 1.3 GHz RF reference (up to **several kHz** range) to provide stable optical pulses for user applications
  - Phase noise of free running laser of **several ps,** desired phase noise less than **500 fs,** (frequency range from 10 Hz to 10 MHz)



RF and Laser Cavity Controller Design

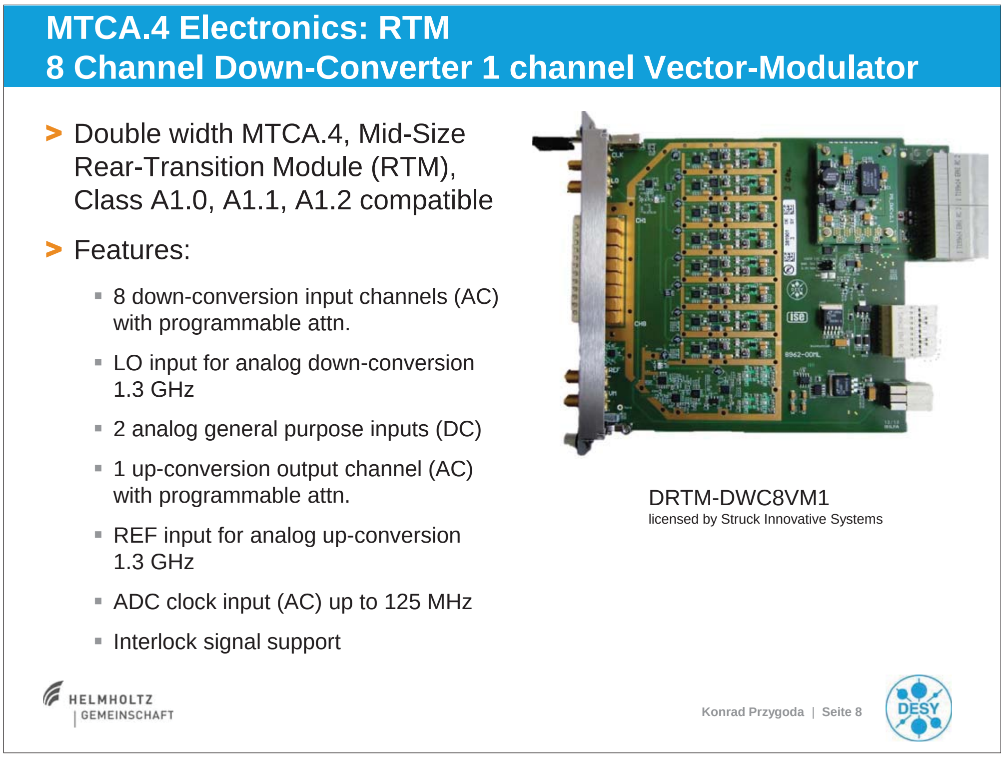
- Control Theory Point of View



RF and Laser Cavity Controller

- RTM sensor and actuator

Konrad Przygoda | Seite 7

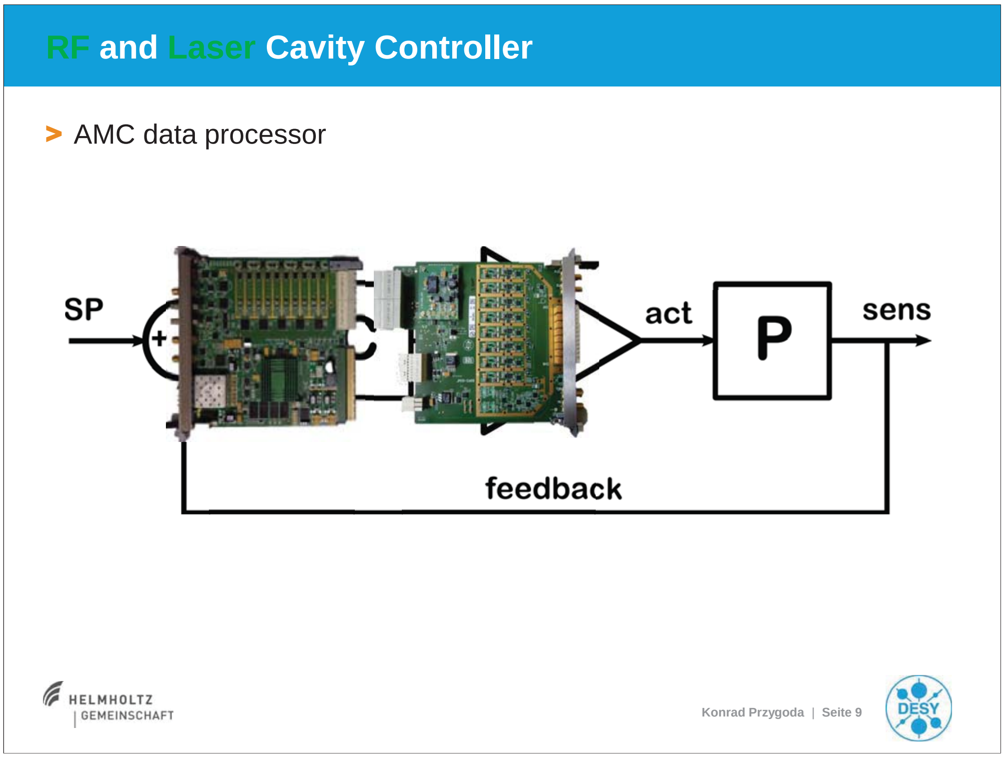


MTCA.4 Electronics: RTM
8 Channel Down-Converter 1 channel Vector-Modulator

- Double width MTCA.4, Mid-Size Rear-Transition Module (RTM), Class A1.0, A1.1, A1.2 compatible
- Features:
  - 8 down-conversion input channels (AC) with programmable attn.
  - LO input for analog down-conversion 1.3 GHz
  - 2 analog general purpose inputs (DC)
  - 1 up-conversion output channel (AC) with programmable attn.
  - REF input for analog up-conversion 1.3 GHz
  - ADC clock input (AC) up to 125 MHz
  - Interlock signal support

DRTM-DWC8VM1
licensed by Struck Innovative Systems

Konrad Przygoda | Seite 8



RF and Laser Cavity Controller

- AMC data processor

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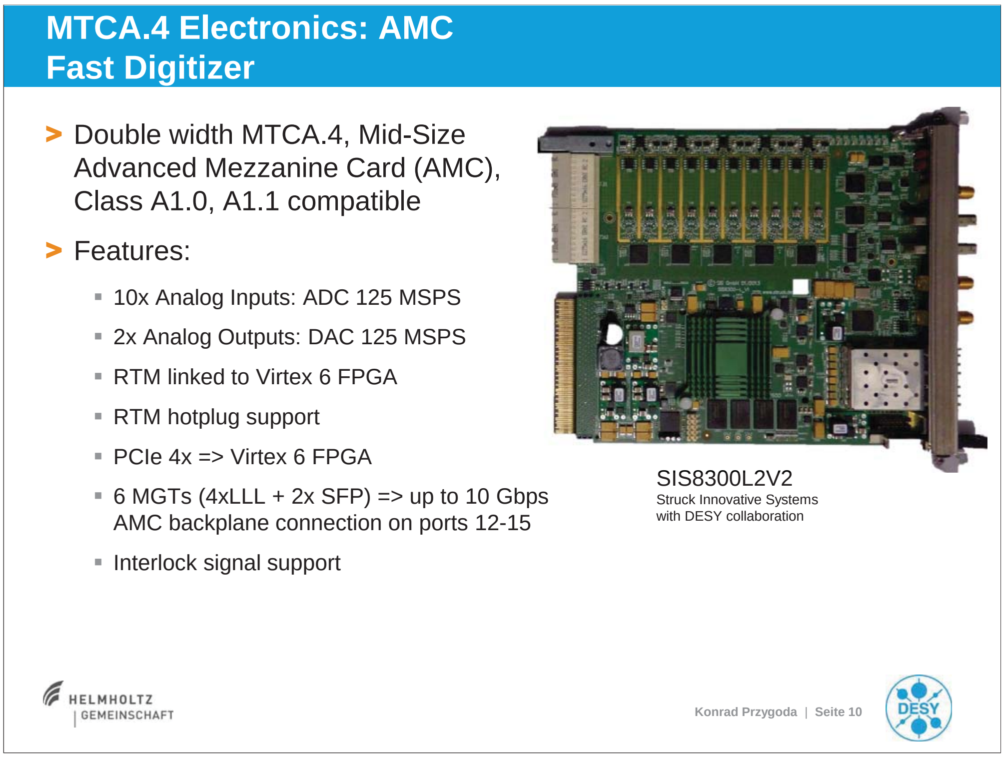
Konrad Przygoda | Seite 9



MTCA.4 Electronics: AMC Fast Digitizer

- Double width MTCA.4, Mid-Size Advanced Mezzanine Card (AMC), Class A1.0, A1.1 compatible
- Features:
  - 10x Analog Inputs: ADC 125 MSPS
  - 2x Analog Outputs: DAC 125 MSPS
  - RTM linked to Virtex 6 FPGA
  - RTM hotplug support
  - PCIe 4x => Virtex 6 FPGA
  - 6 MGTs (4xLLL + 2x SFP) => up to 10 Gbps AMC backplane connection on ports 12-15
  - Interlock signal support

SIS8300L2V2
Struck Innovative Systems
with DESY collaboration

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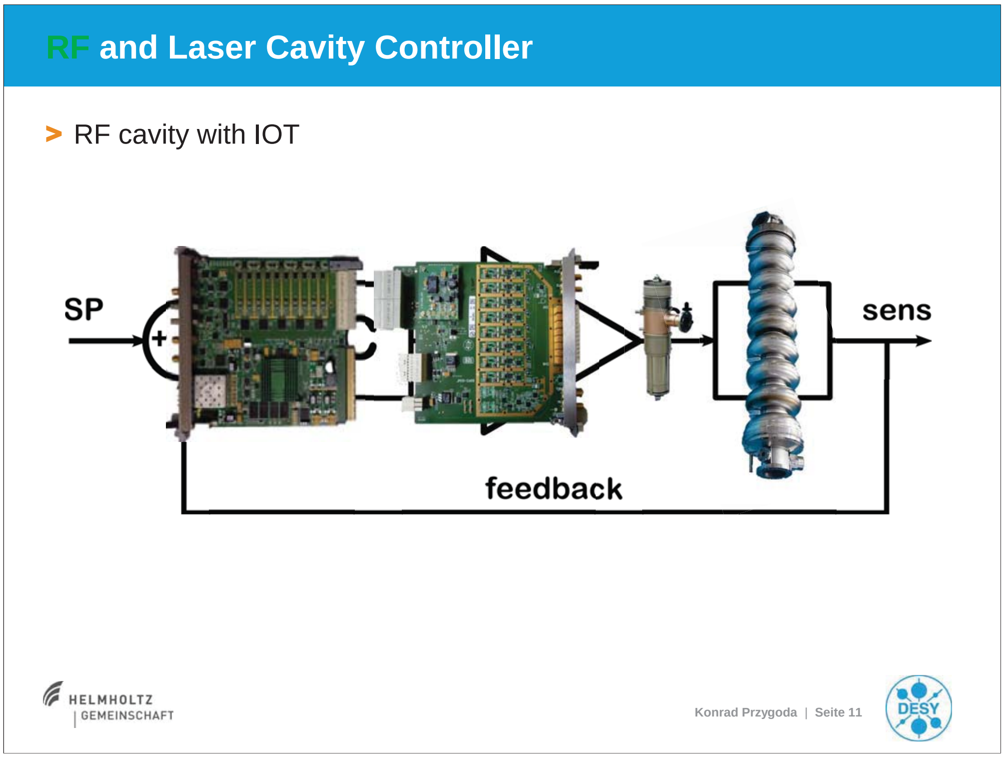

RF and Laser Cavity Controller

- RF cavity with IOT

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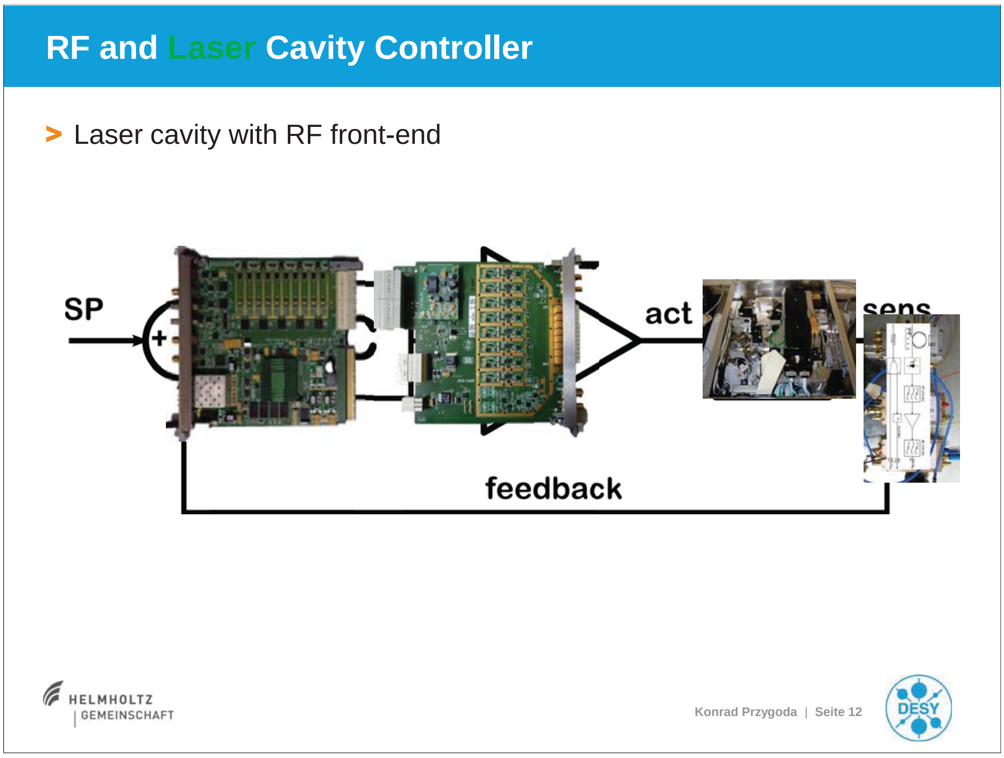

RF and Laser Cavity Controller

- Laser cavity with RF front-end

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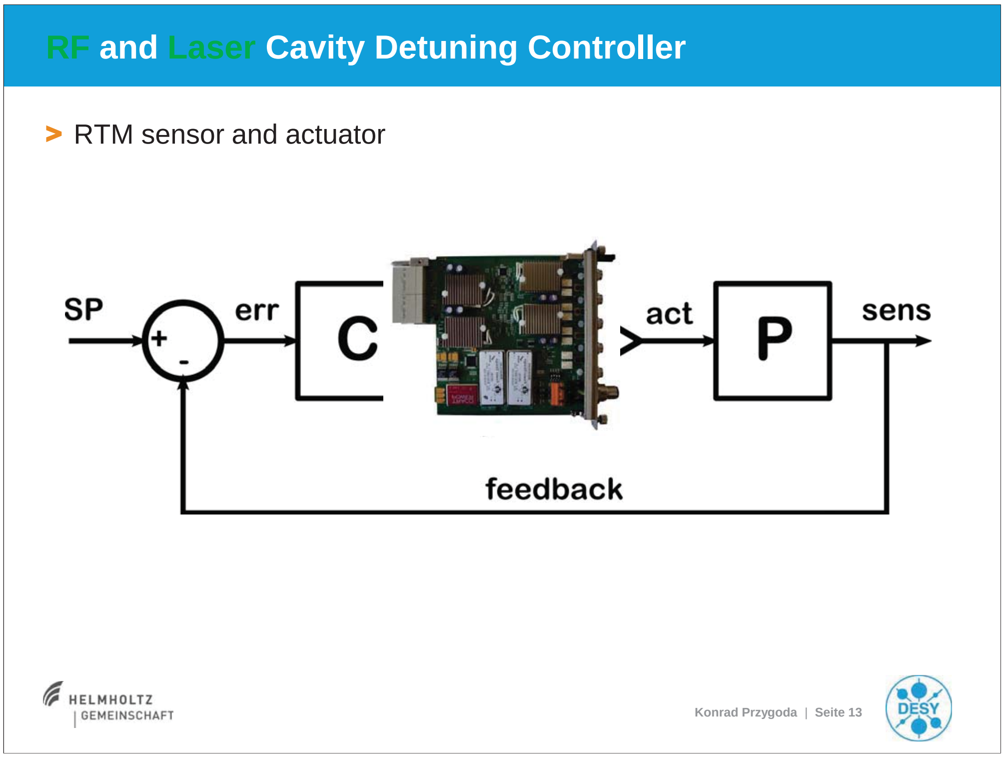
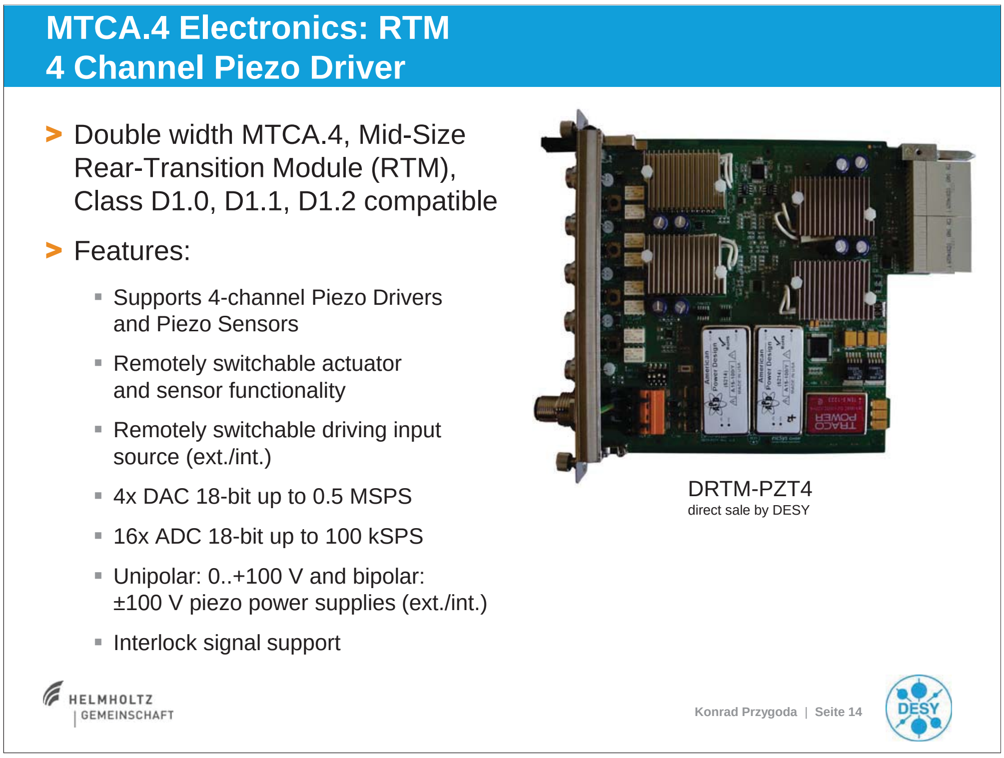


RF and Laser Cavity Detuning Controller

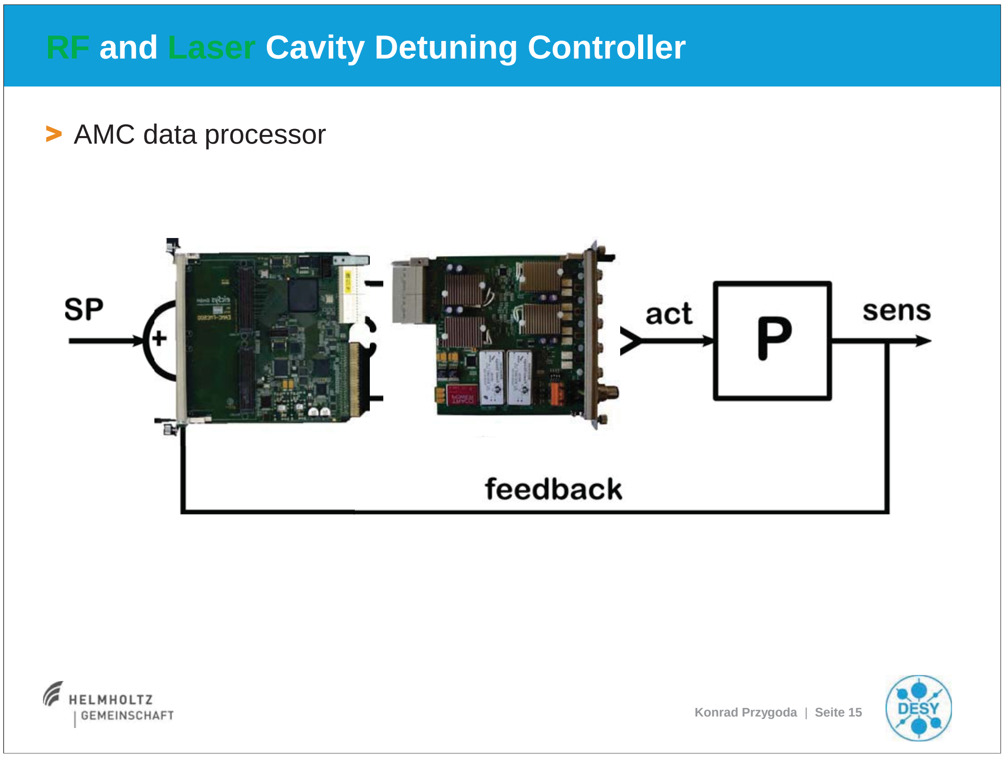
- RTM sensor and actuator



MTCA.4 Electronics: RTM 4 Channel Piezo Driver

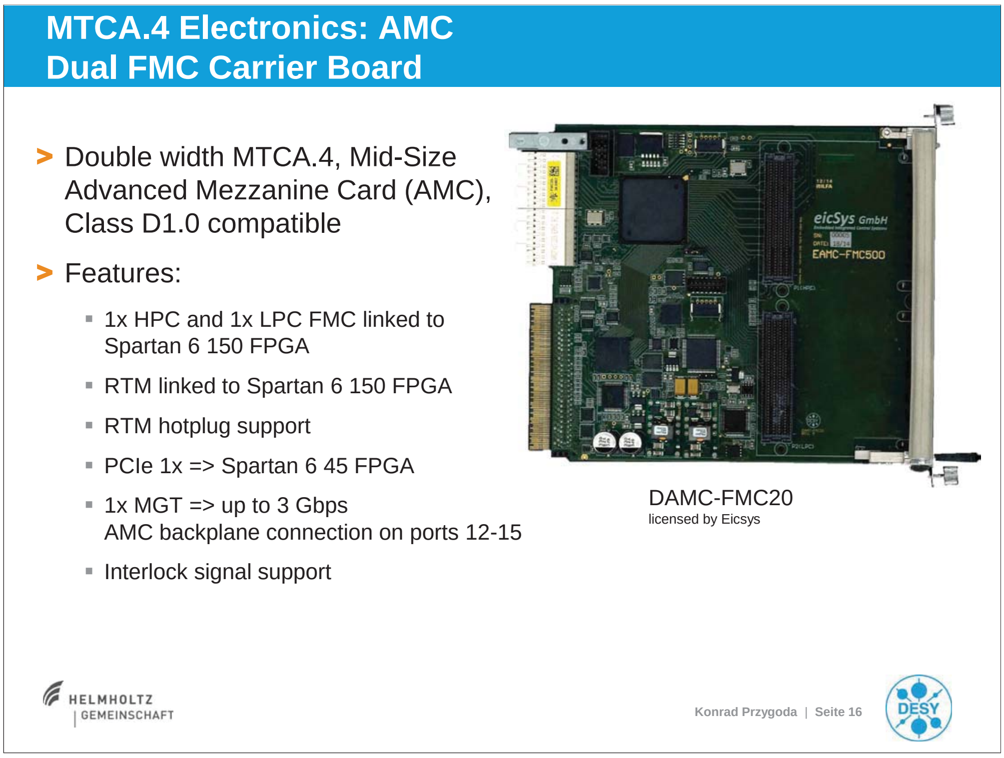
- Double width MTCA.4, Mid-Size Rear-Transition Module (RTM), Class D1.0, D1.1, D1.2 compatible
- Features:
  - Supports 4-channel Piezo Drivers and Piezo Sensors
  - Remotely switchable actuator and sensor functionality
  - Remotely switchable driving input source (ext./int.)
  - 4x DAC 18-bit up to 0.5 MSPS
  - 16x ADC 18-bit up to 100 kSPS
  - Unipolar: 0..+100 V and bipolar: ±100 V piezo power supplies (ext./int.)
  - Interlock signal support

DRTM-PZT4
direct sale by DESY



RF and Laser Cavity Detuning Controller

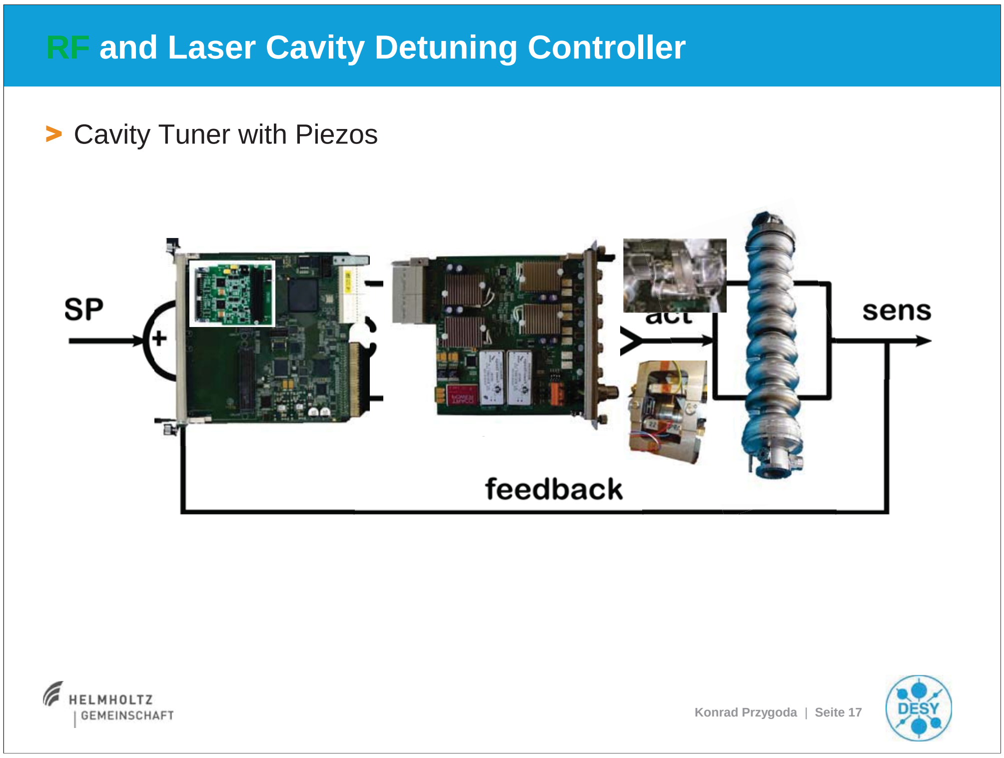
- AMC data processor



MTCA.4 Electronics: AMC Dual FMC Carrier Board

- Double width MTCA.4, Mid-Size Advanced Mezzanine Card (AMC), Class D1.0 compatible
- Features:
  - 1x HPC and 1x LPC FMC linked to Spartan 6 150 FPGA
  - RTM linked to Spartan 6 150 FPGA
  - RTM hotplug support
  - PCIe 1x => Spartan 6 45 FPGA
  - 1x MGT => up to 3 Gbps
    AMC backplane connection on ports 12-15
  - Interlock signal support

DAMC-FMC20
licensed by Eicsys



RF and Laser Cavity Detuning Controller

- Cavity Tuner with Piezos

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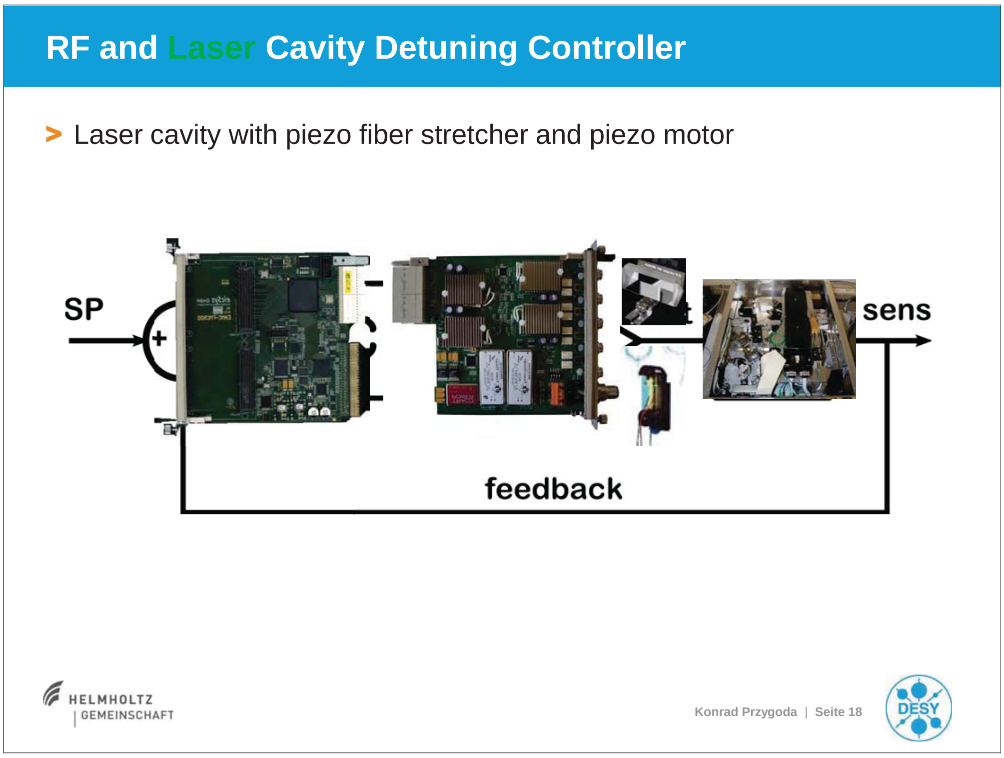

RF and Laser Cavity Detuning Controller

- Laser cavity with piezo fiber stretcher and piezo motor

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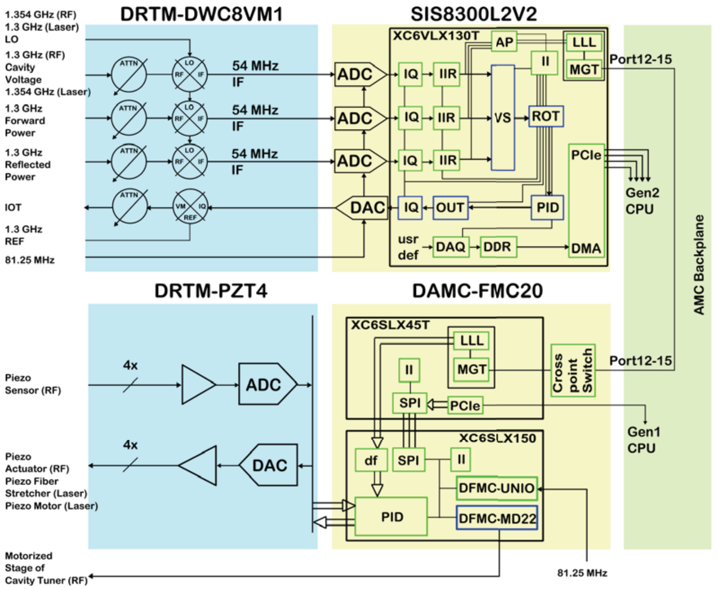
RF and Laser Cavity and Detuning Controller (Firmware)



RF and Laser Cavity and Detuning Controller (Software)

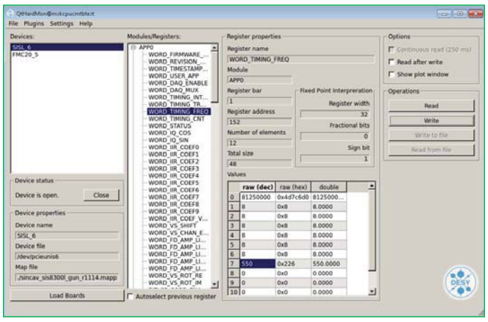
rf_c=mtca4u('SISL_6')
pzt_c = mtca4u('FMC20_5')

rf_ctl_init(rf_c)

rf_ctl_ff(rf_c,val)

rf_ctl_sp(rf_c,val)

rf_ctl_fb(rc_c,val)



Devices:
SISL_6
FMC20_5

Device status
Device is open.

Device properties
Device name: SISL_6
Device file: /dev/pcieunis6
Map file: ./sincav_sis8300l_gun_r1114.mapp

Modules/Registers:
APP0
WORD_FIRMWARE_...
WORD_REVISION_...
WORD_TIMESTAMP...
WORD_USER_APP
WORD_DAQ_ENABLE
WORD_DAQ_MUX
WORD_TIMING_INT...
WORD_TIMING_TR...
WORD_TIMING_FREQ
WORD_TIMING_CNT
WORD_STATUS
WORD_IQ_COS
WORD_IQ_SIN
WORD_IIR_COEF0
WORD_IIR_COEF1
WORD_IIR_COEF2
WORD_IIR_COEF3
WORD_IIR_COEF4
WORD_IIR_COEF5
WORD_IIR_COEF6
WORD_IIR_COEF7
WORD_IIR_COEF8
WORD_IIR_COEF9
WORD_IIR_COEF_V...
WORD_VS_SHIFT
WORD_VS_CHAN_E...
WORD_FD_AMP_LI...
WORD_FD_AMP_LI...
WORD_FD_AMP_LI...
WORD_FD_AMP_LI...
WORD_FD_AMP_LI...
WORD_VS_ROT_RE
WORD_VS_ROT_IM

☐ Autoselect previous register

Register properties
Register name: WORD_TIMING_FREQ
Module: APP0
Register bar: 1
Register address: 152
Number of elements: 12
Total size: 48

Fixed Point Interpreration
Register width: 32
Fractional bits: 0
Sign bit: 1

Values

	raw (dec)	raw (hex)	double
0	81250000	0x4d7c6d0	8125000...
1	8	0x8	8.0000
2	8	0x8	8.0000
3	8	0x8	8.0000
4	8	0x8	8.0000
5	8	0x8	8.0000
6	8	0x8	8.0000
7	550	0x226	550.0000
8	0	0x0	0.0000
9	0	0x0	0.0000
10	0	0x0	0.0000

Options
☐ Continuous read (250 ms)
☐ Read after write
☐ Show plot window

Operations

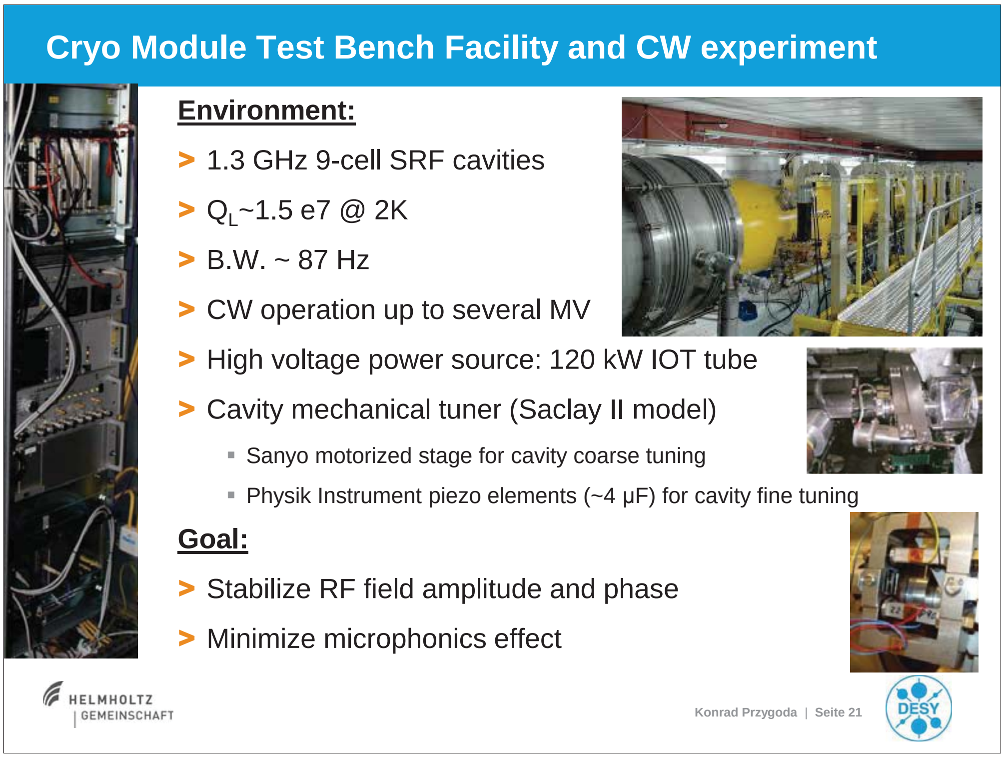
piezo_ctl_init(pzt_c)

piezo_ctl_ff(pzt_c,val)

piezo_ctl_sp(pzt_c,val)

piezo_ctl_fb(pzt_c,val)

[a b] = read_dma_daq({rf_c;pzt_c},no_chan, no_samp, addr)



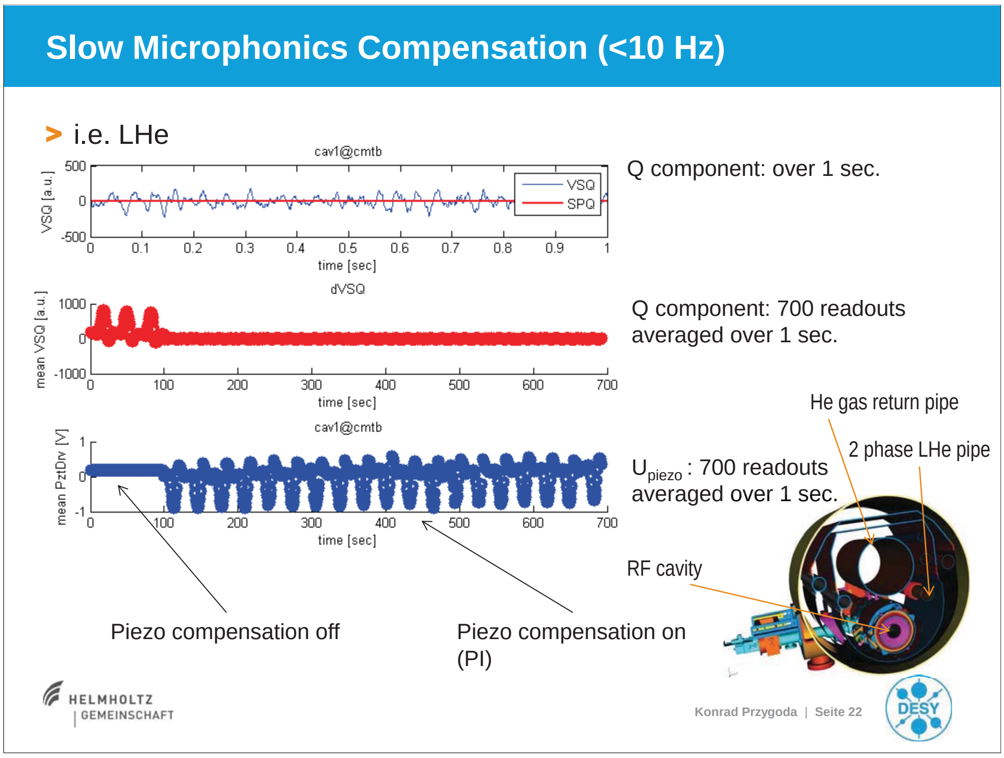
Cryo Module Test Bench Facility and CW experiment

Environment:

- 1.3 GHz 9-cell SRF cavities
- Q_L~1.5 e7 @ 2K
- B.W. ~ 87 Hz
- CW operation up to several MV
- High voltage power source: 120 kW IOT tube
- Cavity mechanical tuner (Saclay II model)
  - Sanyo motorized stage for cavity coarse tuning
  - Physik Instrument piezo elements (~4 μF) for cavity fine tuning

Goal:

- Stabilize RF field amplitude and phase
- Minimize microphonics effect



Slow Microphonics Compensation (<10 Hz)

- i.e. LHe

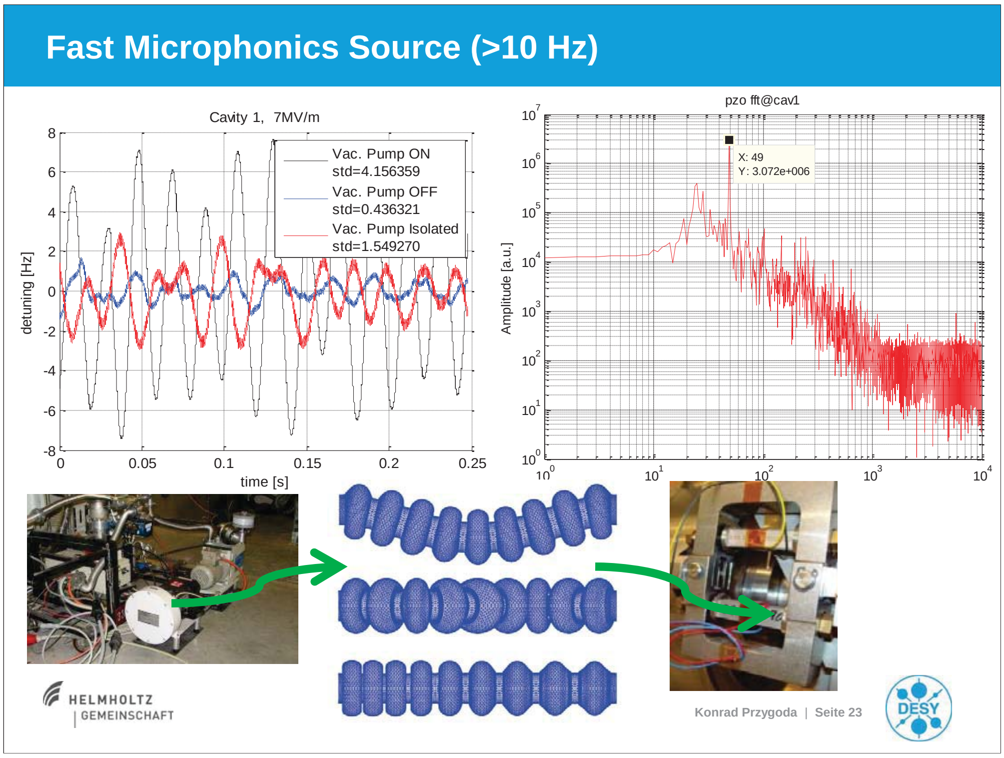
Q component: over 1 sec.

Q component: 700 readouts averaged over 1 sec.

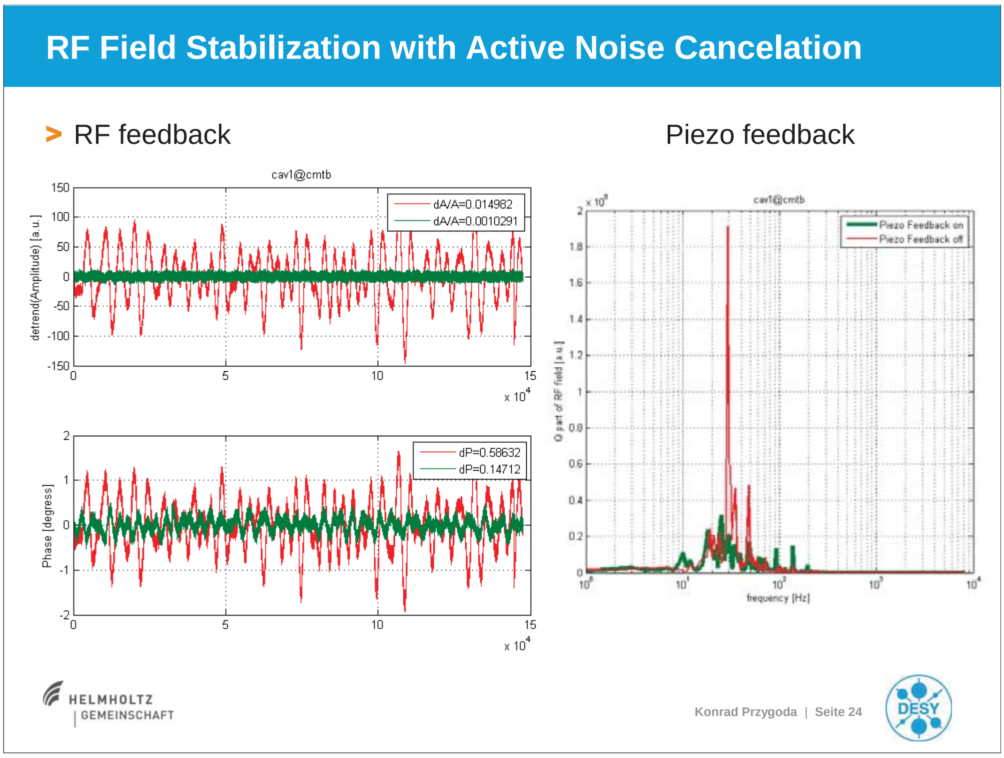
U_{piezo} : 700 readouts averaged over 1 sec.

Piezo compensation off

Piezo compensation on (PI)



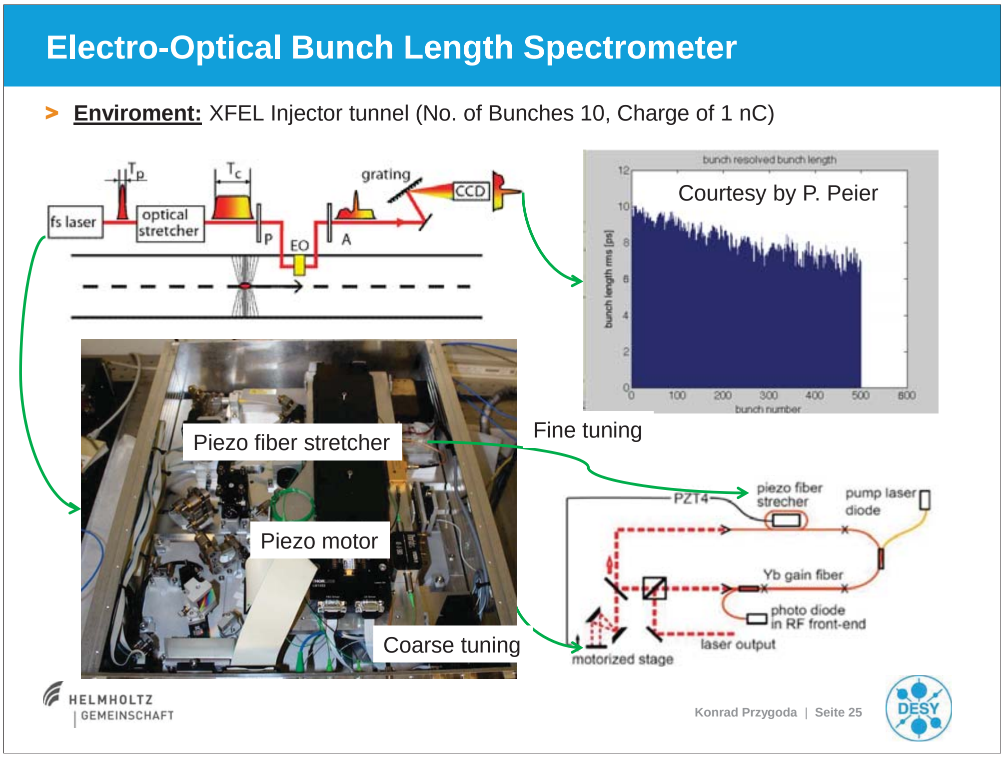
Fast Microphonics Source (>10 Hz)



RF Field Stabilization with Active Noise Cancelation

> RF feedback

Piezo feedback



Electro-Optical Bunch Length Spectrometer

> **Enviroment:** XFEL Injector tunnel (No. of Bunches 10, Charge of 1 nC)

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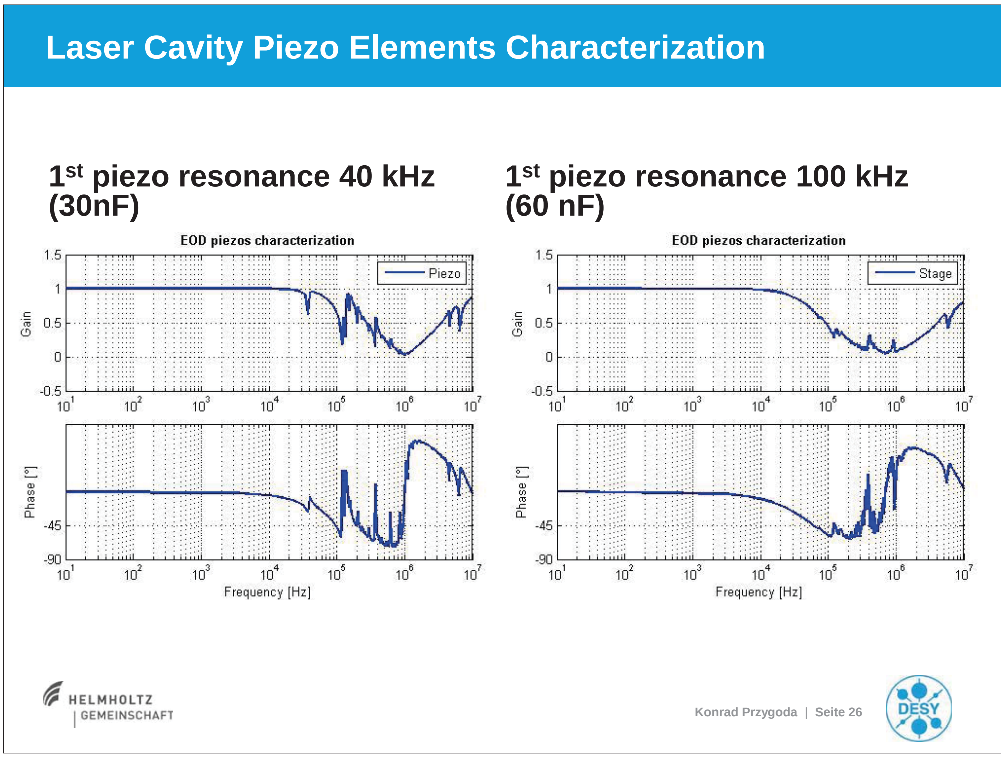

Laser Cavity Piezo Elements Characterization

1st piezo resonance 40 kHz (30nF)

1st piezo resonance 100 kHz (60 nF)

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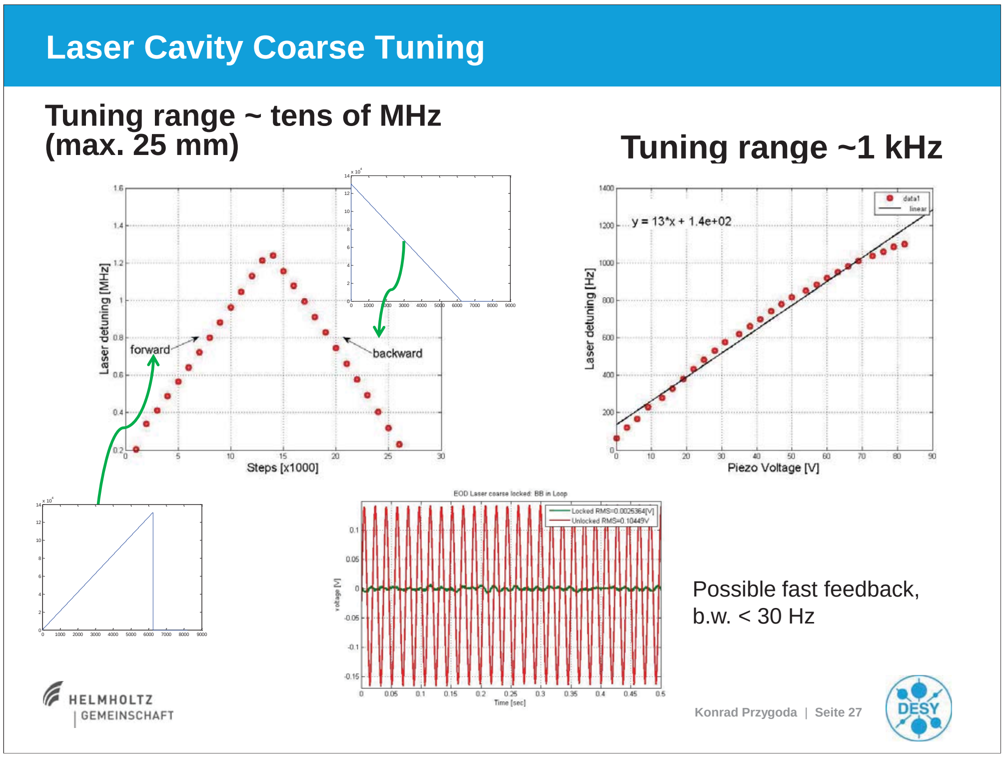

Laser Cavity Coarse Tuning

Tuning range ~ tens of MHz (max. 25 mm)

Tuning range ~1 kHz

Possible fast feedback, b.w. < 30 Hz

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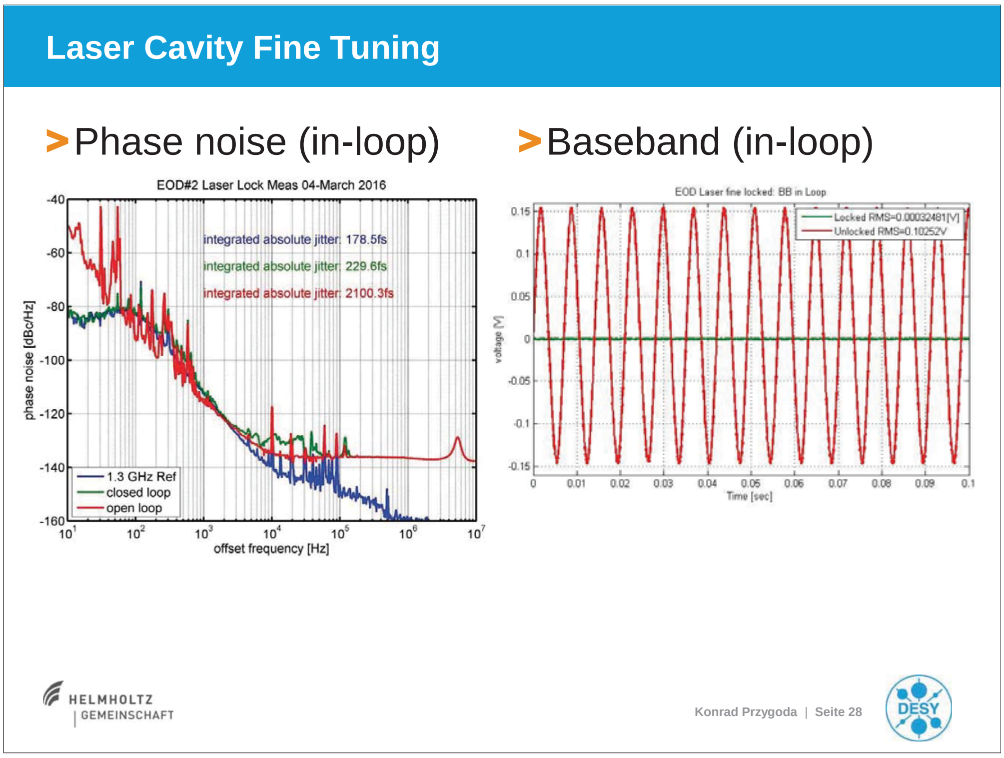

Laser Cavity Fine Tuning

> Phase noise (in-loop)

> Baseband (in-loop)

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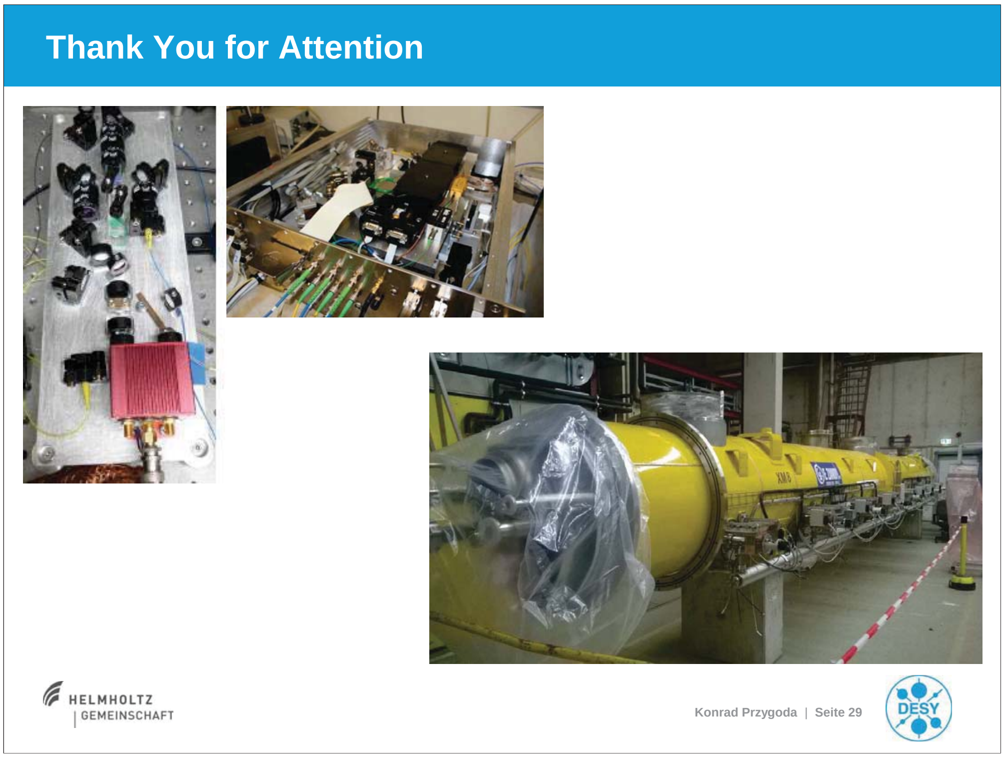

Thank You for Attention

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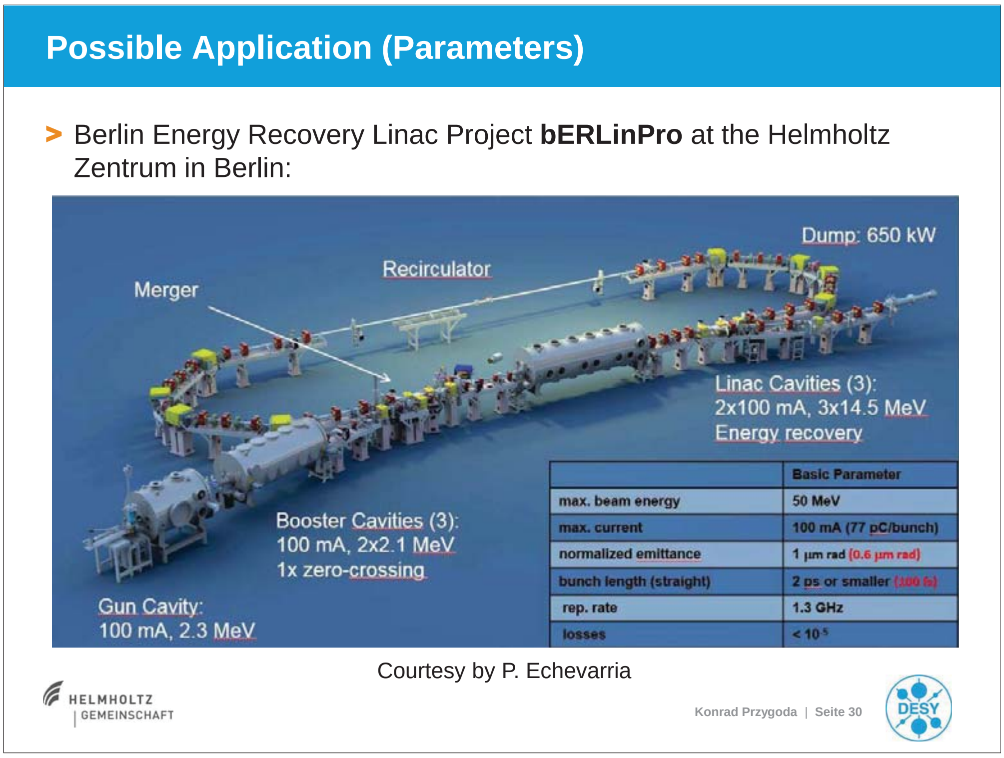

Possible Application (Parameters)

> Berlin Energy Recovery Linac Project **bERLinPro** at the Helmholtz Zentrum in Berlin:

Dump: 650 kW

Recirculator

Merger

Linac Cavities (3):
2x100 mA, 3x14.5 MeV
Energy recovery

Booster Cavities (3):
100 mA, 2x2.1 MeV
1x zero-crossing

Gun Cavity:
100 mA, 2.3 MeV

	Basic Parameter
max. beam energy	50 MeV
max. current	100 mA (77 pC/bunch)
normalized emittance	1 µm rad (0.6 µm rad)
bunch length (straight)	2 ps or smaller (100 fs)
rep. rate	1.3 GHz
losses	$< 10^{-5}$

Courtesy by P. Echevarria

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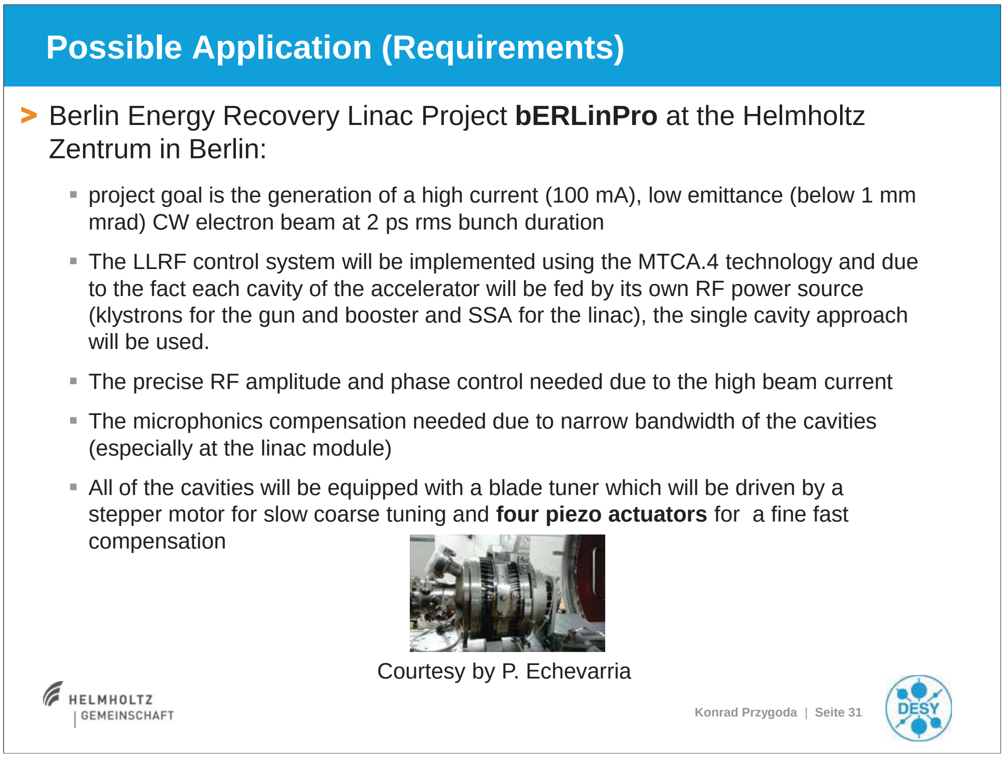
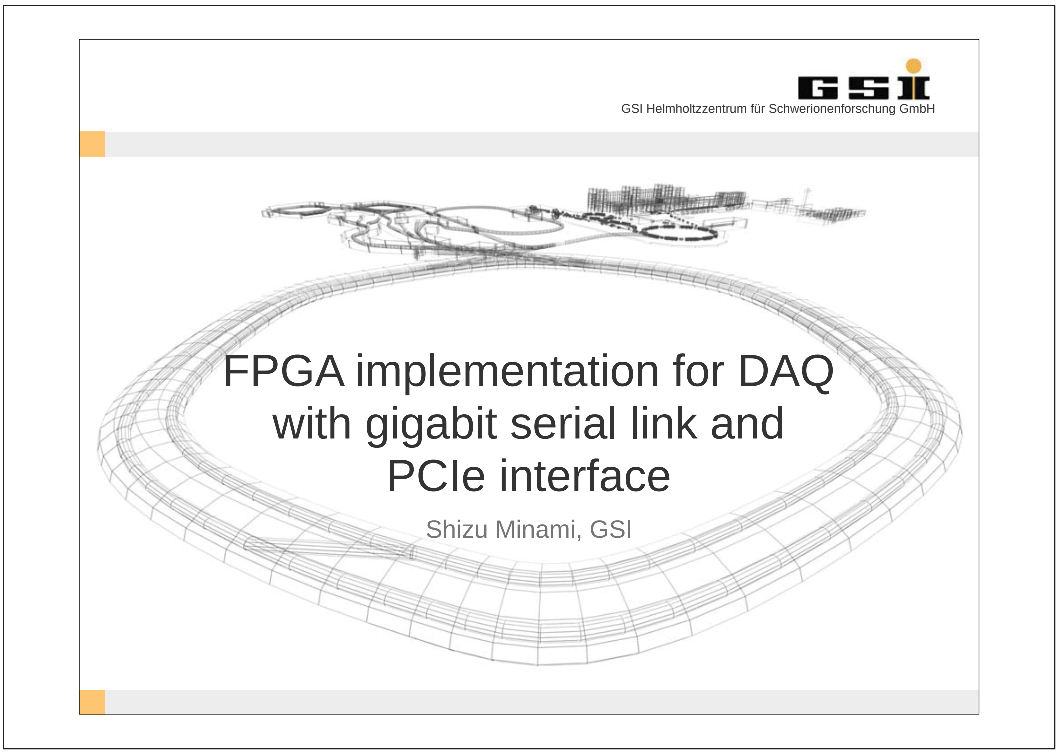


Possible Application (Requirements)

> Berlin Energy Recovery Linac Project **bERLinPro** at the Helmholtz Zentrum in Berlin:

- project goal is the generation of a high current (100 mA), low emittance (below 1 mm mrad) CW electron beam at 2 ps rms bunch duration
- The LLRF control system will be implemented using the MTCA.4 technology and due to the fact each cavity of the accelerator will be fed by its own RF power source (klystrons for the gun and booster and SSA for the linac), the single cavity approach will be used.
- The precise RF amplitude and phase control needed due to the high beam current
- The microphonics compensation needed due to narrow bandwidth of the cavities (especially at the linac module)
- All of the cavities will be equipped with a blade tuner which will be driven by a stepper motor for slow coarse tuning and **four piezo actuators** for a fine fast compensation

Courtesy by P. Echevarria



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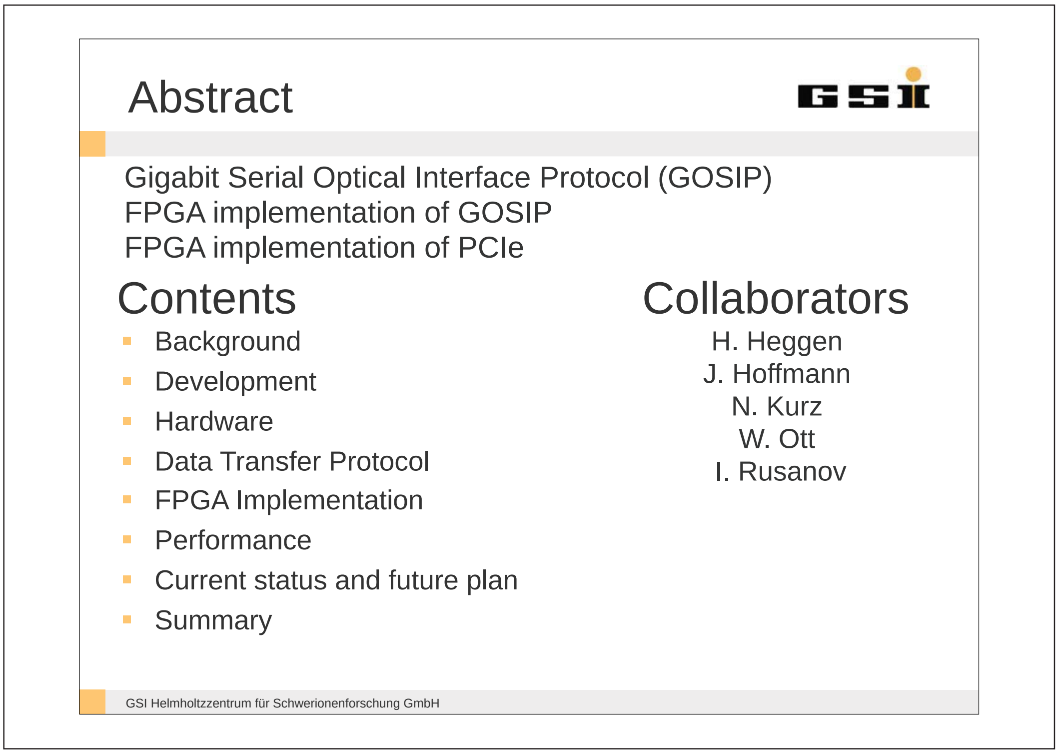
FPGA implementation for DAQ with gigabit serial link and PCIe interface

Shizu Minami, GSI



Abstract

Gigabit Serial Optical Interface Protocol (GOSIP)
FPGA implementation of GOSIP
FPGA implementation of PCIe

Contents

- Background
- Development
- Hardware
- Data Transfer Protocol
- FPGA Implementation
- Performance
- Current status and future plan
- Summary

Collaborators

H. Heggen
J. Hoffmann
N. Kurz
W. Ott
I. Rusanov

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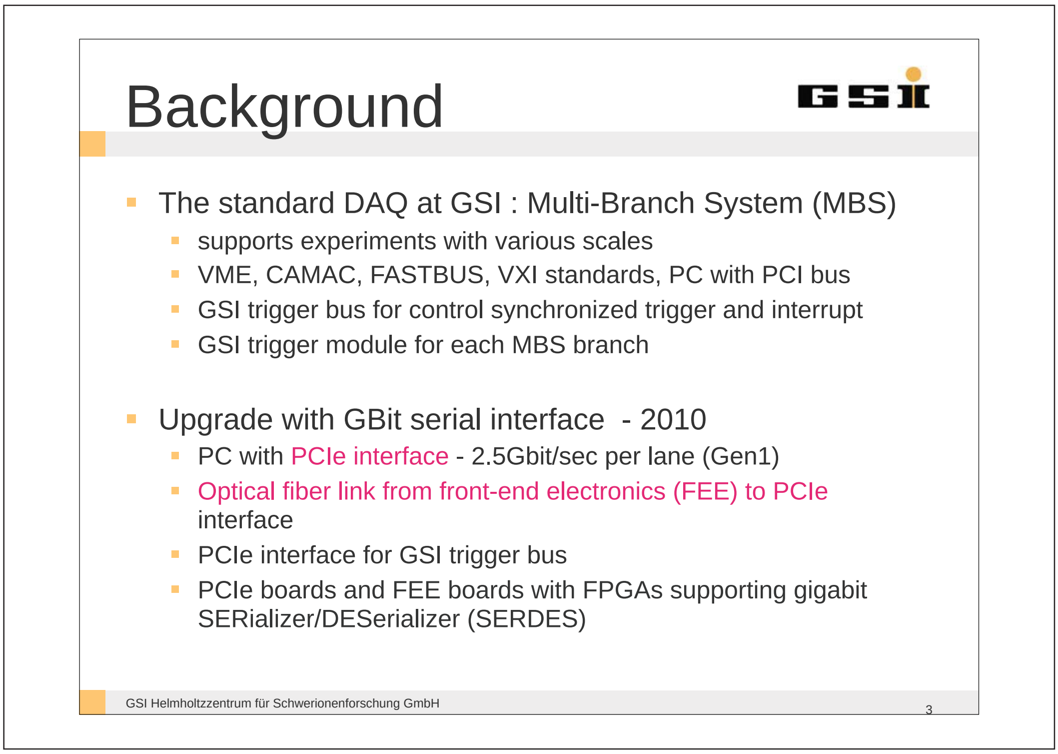
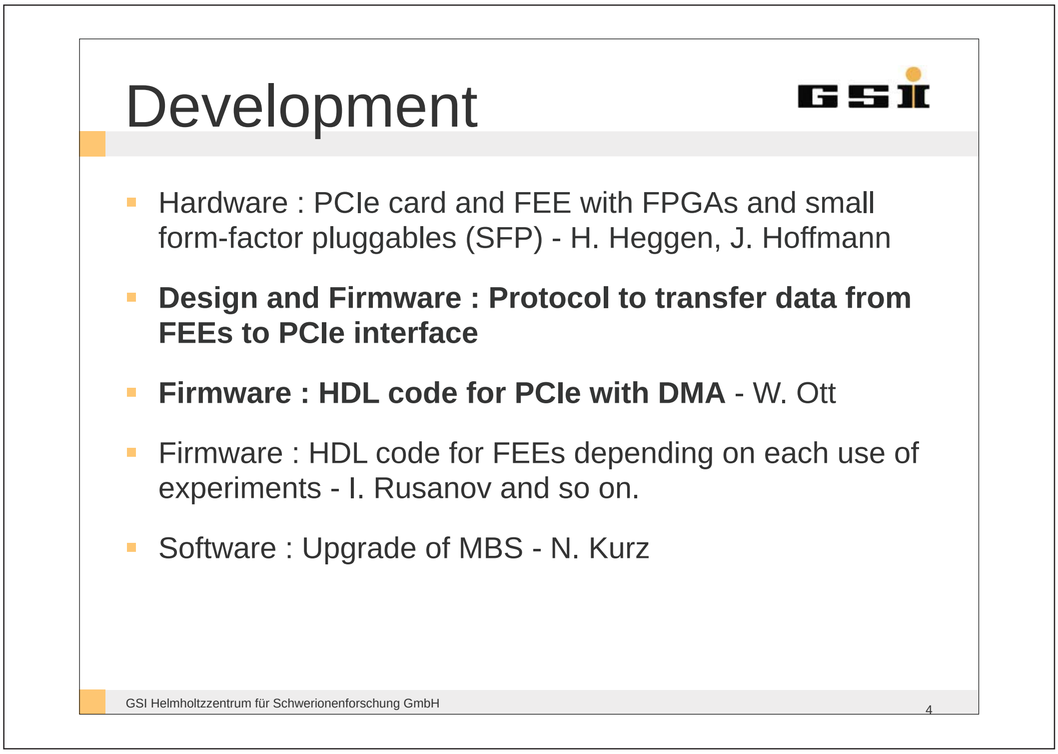


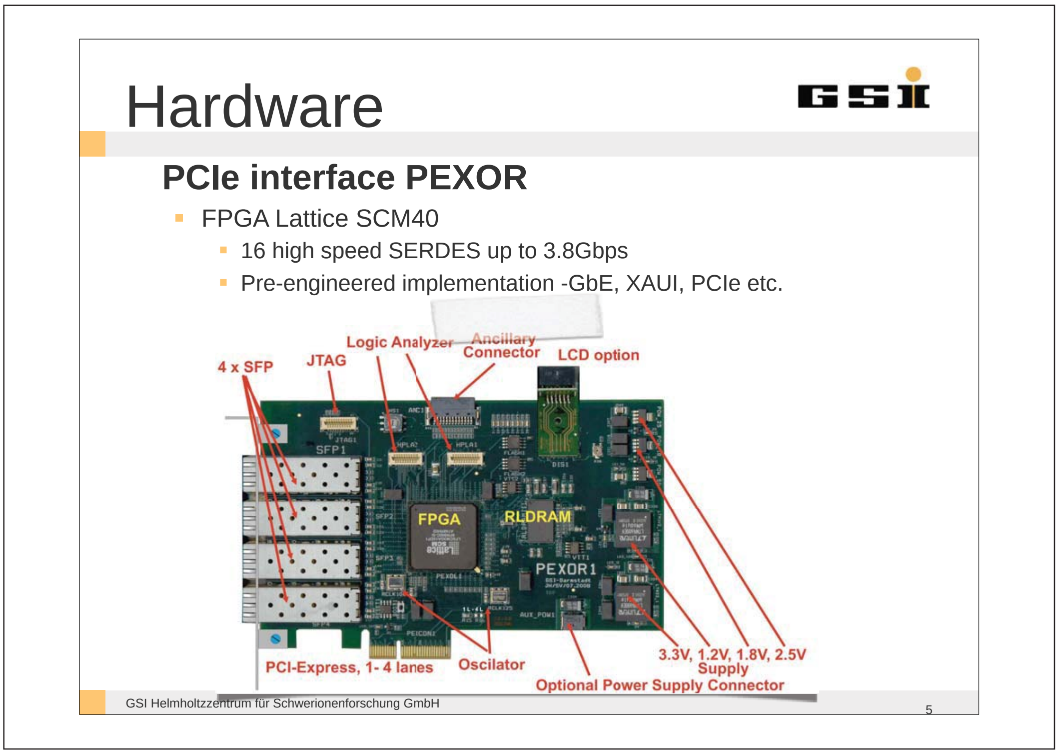
Background

- The standard DAQ at GSI : Multi-Branch System (MBS)
  - supports experiments with various scales
  - VME, CAMAC, FASTBUS, VXI standards, PC with PCI bus
  - GSI trigger bus for control synchronized trigger and interrupt
  - GSI trigger module for each MBS branch
- Upgrade with GBit serial interface - 2010
  - PC with PCIe interface - 2.5Gbit/sec per lane (Gen1)
  - Optical fiber link from front-end electronics (FEE) to PCIe interface
  - PCIe interface for GSI trigger bus
  - PCIe boards and FEE boards with FPGAs supporting gigabit SERializer/DESerializer (SERDES)



Development

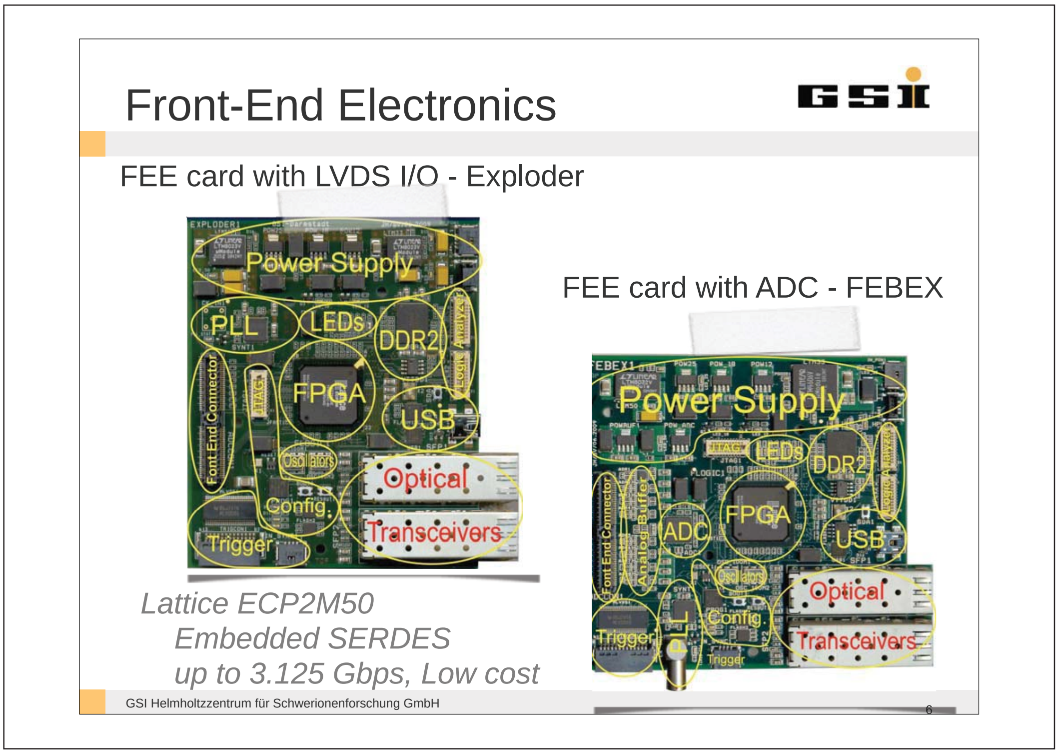
- Hardware : PCIe card and FEE with FPGAs and small form-factor pluggables (SFP) - H. Heggen, J. Hoffmann
- **Design and Firmware : Protocol to transfer data from FEEs to PCIe interface**
- **Firmware : HDL code for PCIe with DMA** - W. Ott
- Firmware : HDL code for FEEs depending on each use of experiments - I. Rusanov and so on.
- Software : Upgrade of MBS - N. Kurz



Hardware

PCIe interface PEXOR

- FPGA Lattice SCM40
  - 16 high speed SERDES up to 3.8Gbps
  - Pre-engineered implementation -GbE, XAUI, PCIe etc.

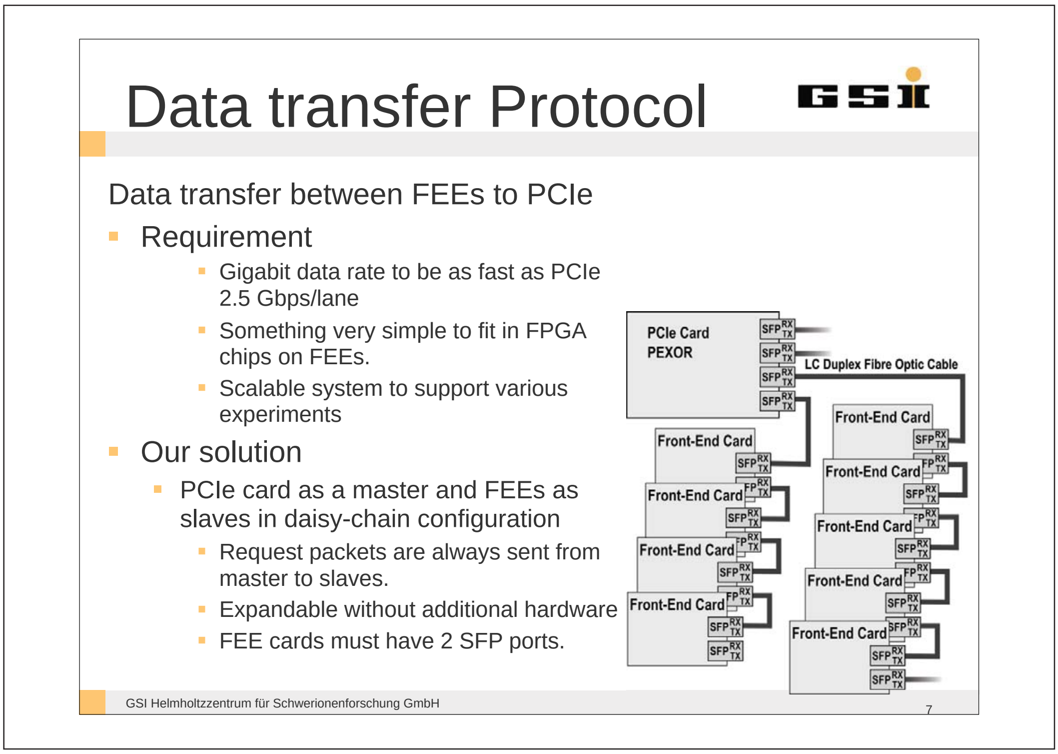


Front-End Electronics

FEE card with LVDS I/O - Exploder

Lattice ECP2M50
Embedded SERDES
up to 3.125 Gbps, Low cost

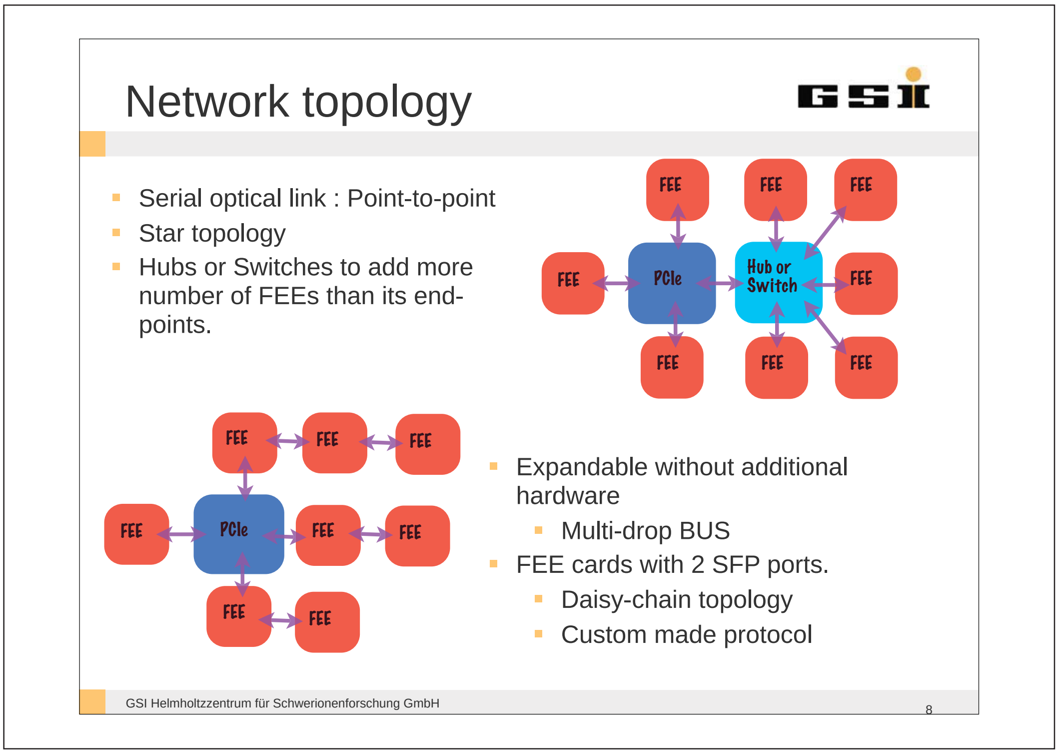
FEE card with ADC - FEBEX



Data transfer Protocol

Data transfer between FEEs to PCIe

- Requirement
  - Gigabit data rate to be as fast as PCIe 2.5 Gbps/lane
  - Something very simple to fit in FPGA chips on FEEs.
  - Scalable system to support various experiments
- Our solution
  - PCIe card as a master and FEEs as slaves in daisy-chain configuration
    - Request packets are always sent from master to slaves.
    - Expandable without additional hardware
    - FEE cards must have 2 SFP ports.



Network topology

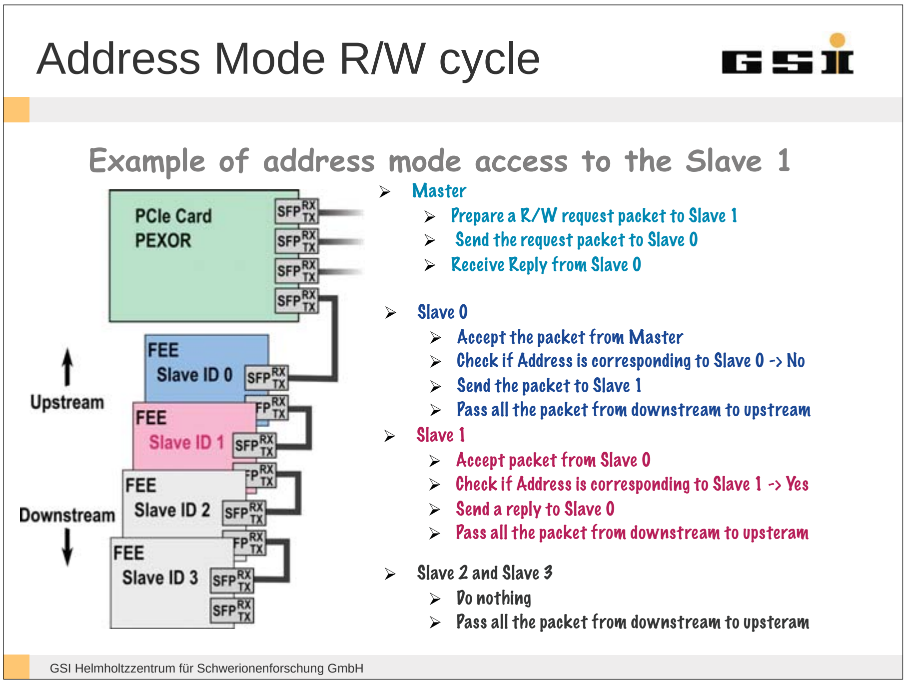
- Serial optical link : Point-to-point
- Star topology
- Hubs or Switches to add more number of FEEs than its end-points.

- Expandable without additional hardware
  - Multi-drop BUS
- FEE cards with 2 SFP ports.
  - Daisy-chain topology
  - Custom made protocol

Design of protocol

- Gigabit Optical Serial Interface Protocol (GOSIP)
  - 8bit base - SERDES configured as 8b10b
  - 2Gbps (PCIe 2.5 Gbps, low-cost FPGA)
  - Optical link but like memory mapped multi-drop BUS
  - Initialization
    - gives FEEs 8-bit module IDs
    - The slave module closest to the master assigned to ID 0, then next module is assigned to ID 1, and so on.
  - Two modes of data transfer
    - Address mode
      - read/write access to registers and memories on FEEs
      - Each register/memory has own address
      - Address space 24bits, data width 32bits per FEE
      - A32D32 memory space per SFP port
    - Block mode (token passing) - fast data transfer to PCIe interface

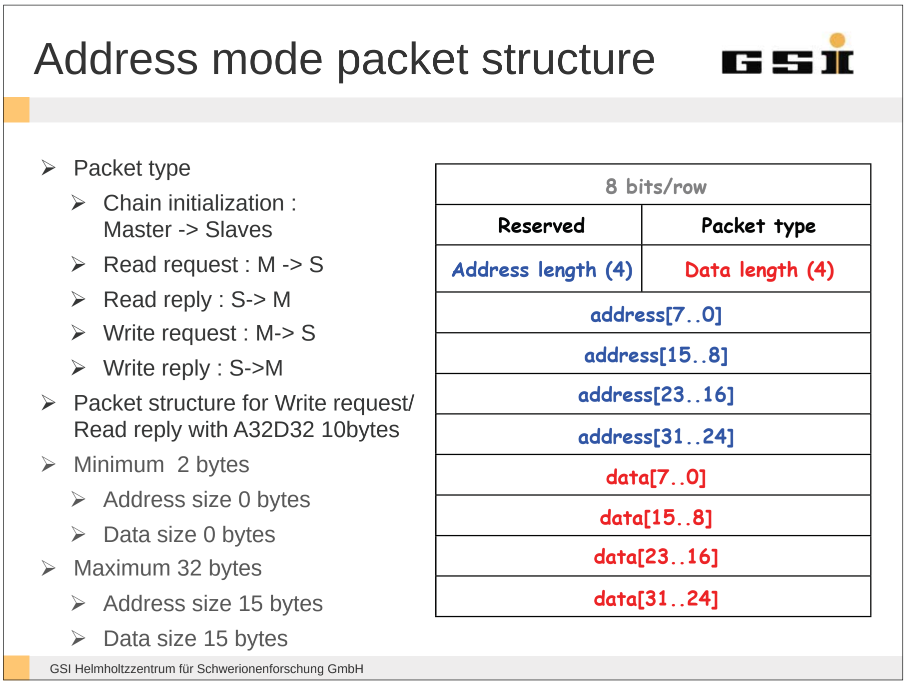
---



Address Mode R/W cycle

Example of address mode access to the Slave 1

- Master
  - Prepare a R/W request packet to Slave 1
  - Send the request packet to Slave 0
  - Receive Reply from Slave 0
- Slave 0
  - Accept the packet from Master
  - Check if Address is corresponding to Slave 0 -> No
  - Send the packet to Slave 1
  - Pass all the packet from downstream to upstream
- Slave 1
  - Accept packet from Slave 0
  - Check if Address is corresponding to Slave 1 -> Yes
  - Send a reply to Slave 0
  - Pass all the packet from downstream to upsteram
- Slave 2 and Slave 3
  - Do nothing
  - Pass all the packet from downstream to upsteram



Address mode packet structure

- Packet type
  - Chain initialization : Master -> Slaves
  - Read request : M -> S
  - Read reply : S-> M
  - Write request : M-> S
  - Write reply : S->M
- Packet structure for Write request/ Read reply with A32D32 10bytes
- Minimum 2 bytes
  - Address size 0 bytes
  - Data size 0 bytes
- Maximum 32 bytes
  - Address size 15 bytes
  - Data size 15 bytes

8 bits/row	
Reserved	**Packet type**
Address length (4)	Data length (4)
address[7..0]	
address[15..8]	
address[23..16]	
address[31..24]	
data[7..0]	
data[15..8]	
data[23..16]	
data[31..24]	

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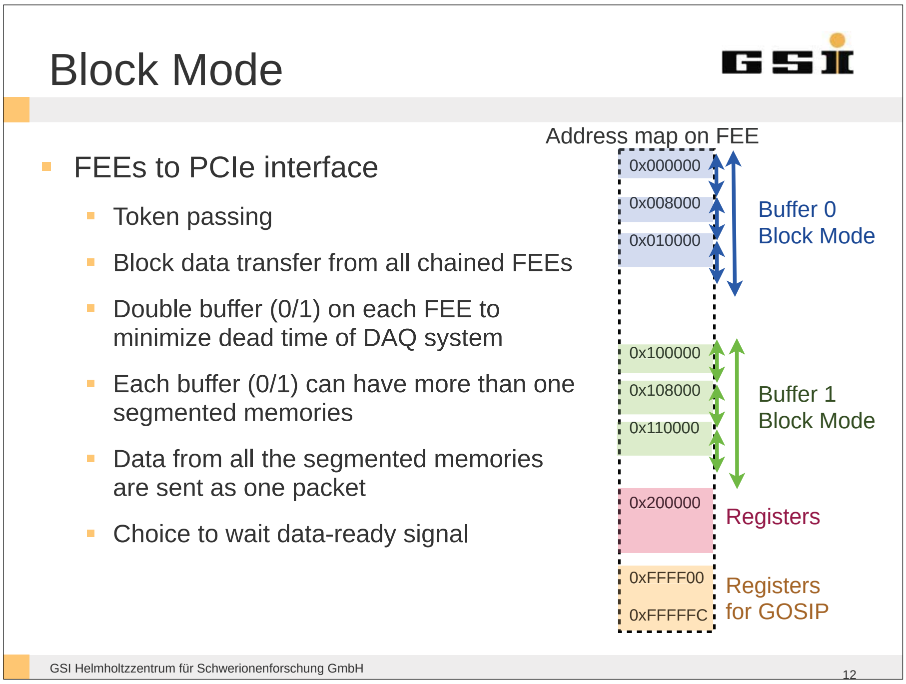

Block Mode

- FEEs to PCIe interface
  - Token passing
  - Block data transfer from all chained FEEs
  - Double buffer (0/1) on each FEE to minimize dead time of DAQ system
  - Each buffer (0/1) can have more than one segmented memories
  - Data from all the segmented memories are sent as one packet
  - Choice to wait data-ready signal

Address map on FEE

0x000000
0x008000
0x010000
Buffer 0 Block Mode

0x100000
0x108000
0x110000
Buffer 1 Block Mode

0x200000
Registers

0xFFFF00
0xFFFFFC
Registers for GOSIP

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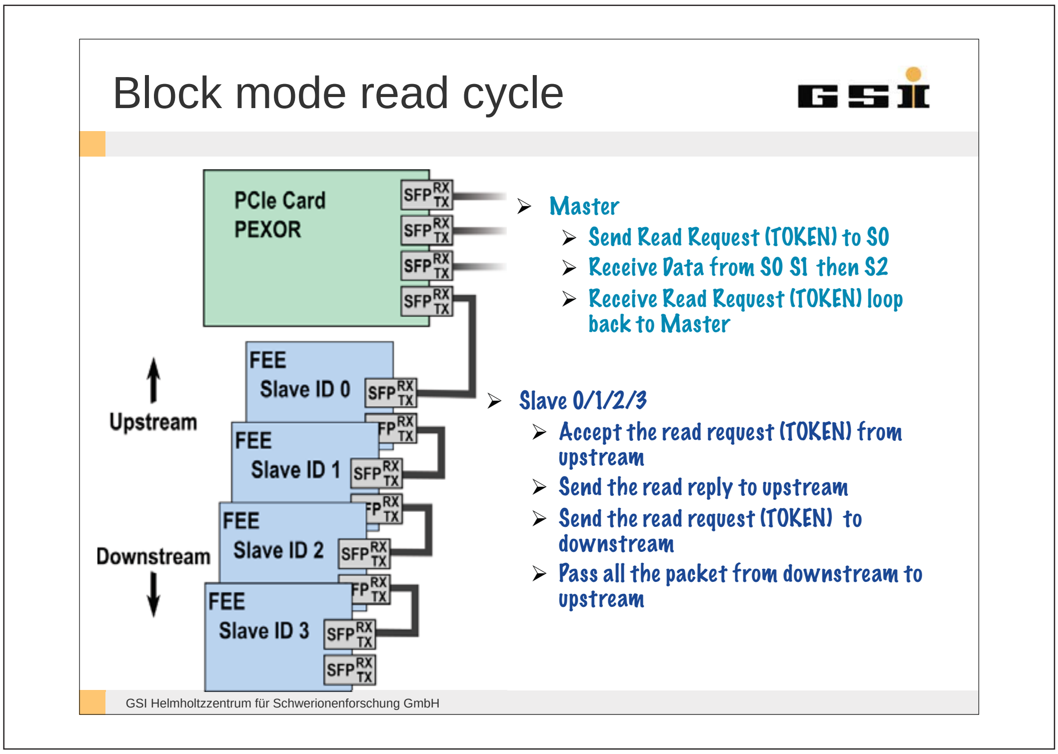
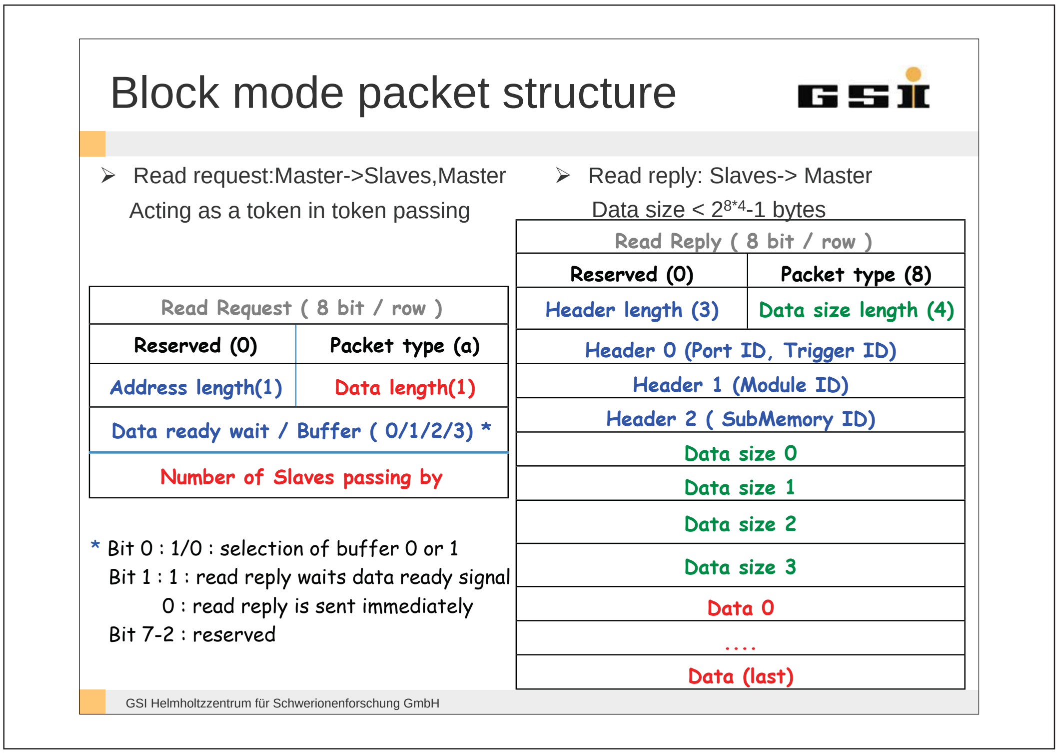


Block mode read cycle

- Master
  - Send Read Request (TOKEN) to S0
  - Receive Data from S0 S1 then S2
  - Receive Read Request (TOKEN) loop back to Master
- Slave 0/1/2/3
  - Accept the read request (TOKEN) from upstream
  - Send the read reply to upstream
  - Send the read request (TOKEN) to downstream
  - Pass all the packet from downstream to upstream



Block mode packet structure

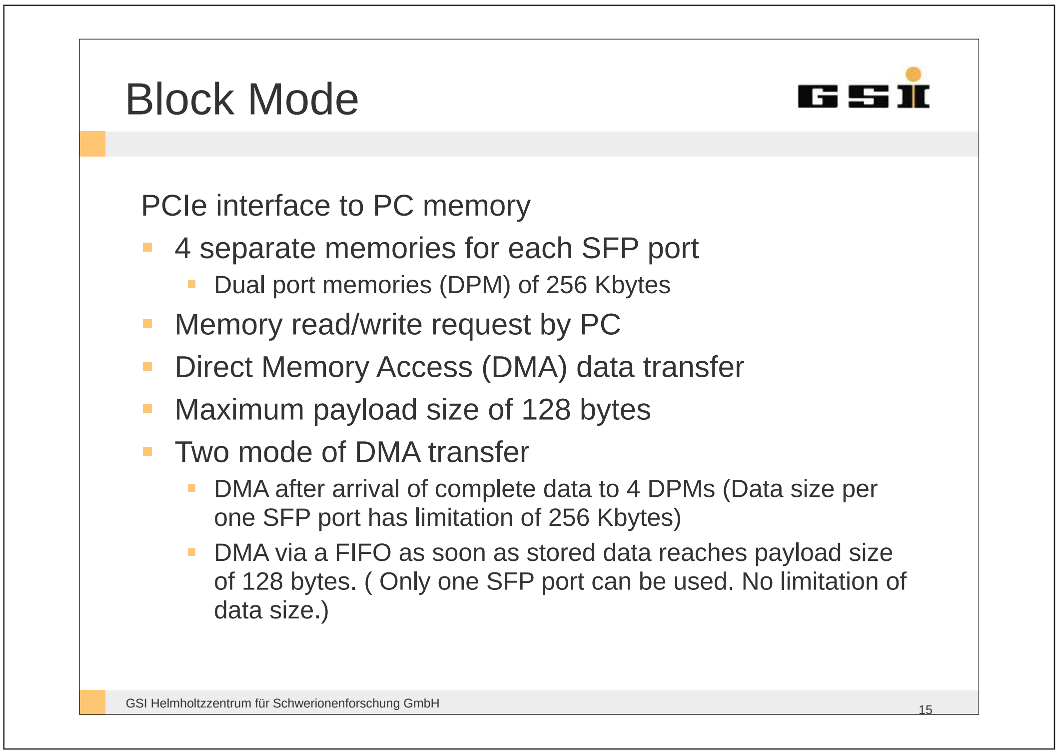
- Read request:Master->Slaves,Master Acting as a token in token passing

Read Request (8 bit / row)	
Reserved (0)	Packet type (a)
Address length(1)	Data length(1)
Data ready wait / Buffer (0/1/2/3) *	
Number of Slaves passing by	

* Bit 0 : 1/0 : selection of buffer 0 or 1
Bit 1 : 1 : read reply waits data ready signal
0 : read reply is sent immediately
Bit 7-2 : reserved

- Read reply: Slaves-> Master Data size < 2^{8*4}-1 bytes

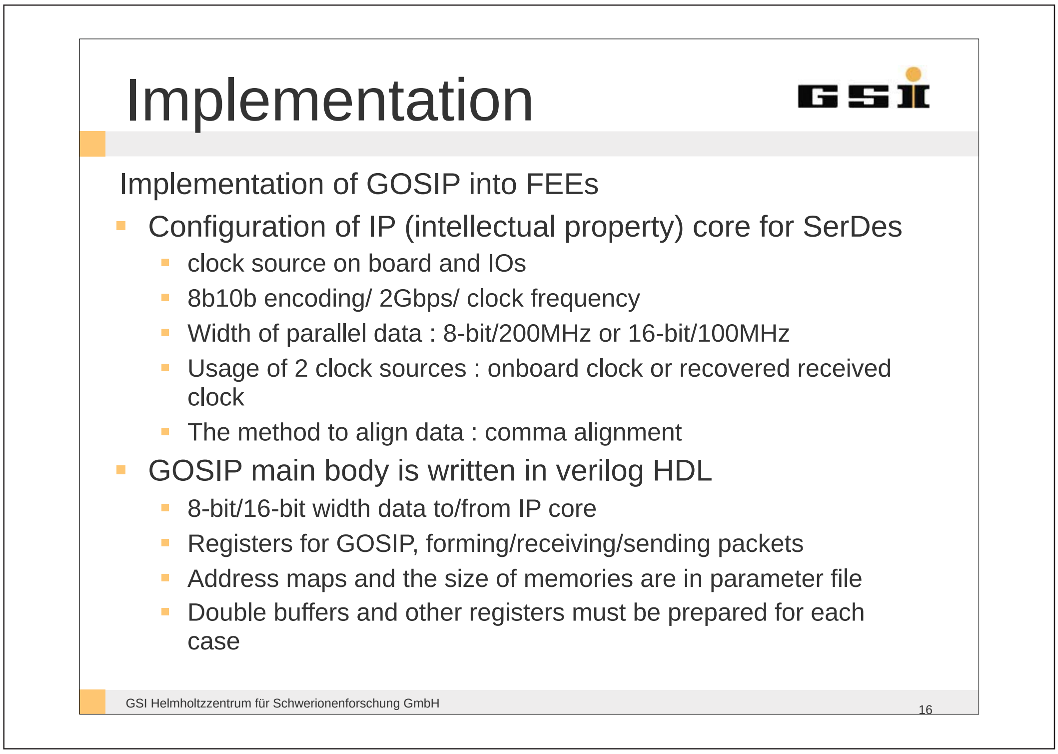
Read Reply (8 bit / row)	
Reserved (0)	Packet type (8)
Header length (3)	Data size length (4)
Header 0 (Port ID, Trigger ID)	
Header 1 (Module ID)	
Header 2 (SubMemory ID)	
Data size 0	
Data size 1	
Data size 2	
Data size 3	
Data 0	
....	
Data (last)	



Block Mode

PCIe interface to PC memory

- 4 separate memories for each SFP port
  - Dual port memories (DPM) of 256 Kbytes
- Memory read/write request by PC
- Direct Memory Access (DMA) data transfer
- Maximum payload size of 128 bytes
- Two mode of DMA transfer
  - DMA after arrival of complete data to 4 DPMs (Data size per one SFP port has limitation of 256 Kbytes)
  - DMA via a FIFO as soon as stored data reaches payload size of 128 bytes. (Only one SFP port can be used. No limitation of data size.)



Implementation

Implementation of GOSIP into FEEs

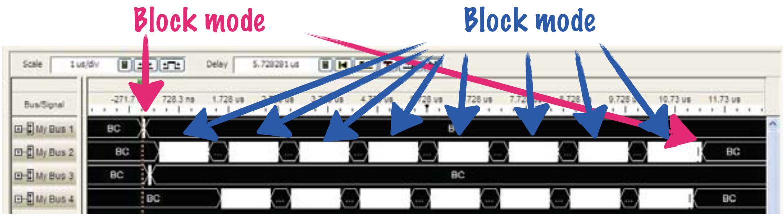
- Configuration of IP (intellectual property) core for SerDes
  - clock source on board and IOs
  - 8b10b encoding/ 2Gbps/ clock frequency
  - Width of parallel data : 8-bit/200MHz or 16-bit/100MHz
  - Usage of 2 clock sources : onboard clock or recovered received clock
  - The method to align data : comma alignment
- GOSIP main body is written in verilog HDL
  - 8-bit/16-bit width data to/from IP core
  - Registers for GOSIP, forming/receiving/sending packets
  - Address maps and the size of memories are in parameter file
  - Double buffers and other registers must be prepared for each case

Implementation of GPSIP

Implementation of GOSIP into FEEs

- 5 % for protocol - 1k Slices of Lattice ECP2M50

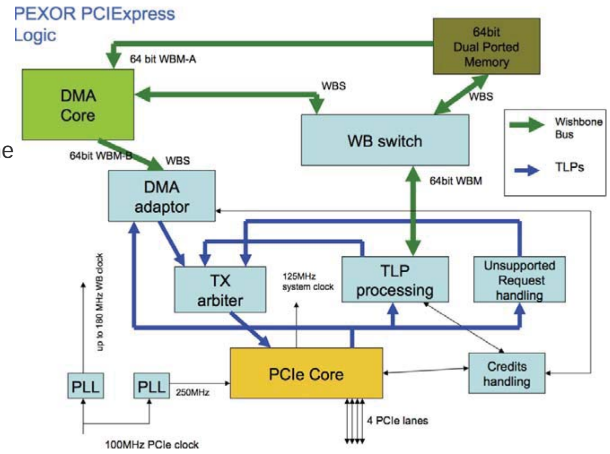
Block Mode with 8 slaves with data size of 200 bytes per



410 nsec + cable delay

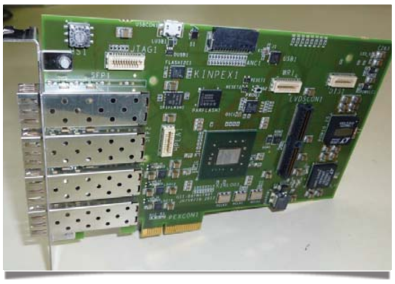
PCIe implementation - PEXOR(Lattice SCM40)

- PCIe has 3 layers: Transaction Layer, Data Link Layer, Physical Layer
- IP core covers all PCIe layers up to the basic transaction layer.
- Transaction layer packet (TLPs) <- a demo PCI express board
- Interconnect with Wishbone interface
- DMA engine
- Interrupt handling



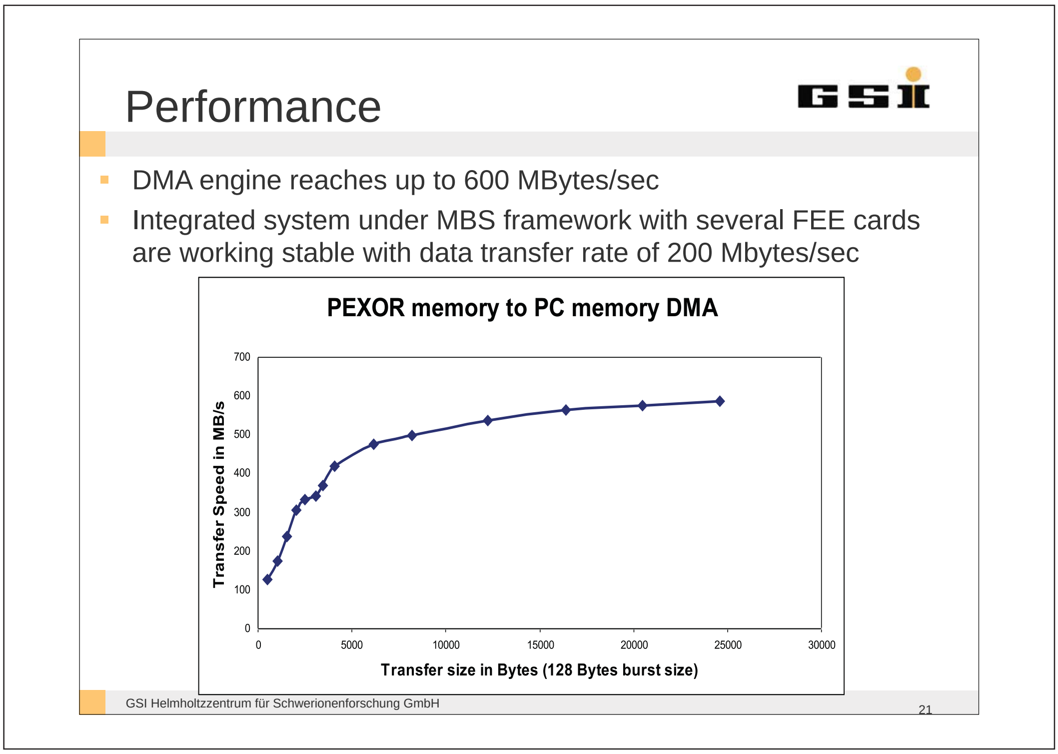
PCIe implementation - KINPEX

- Kintex-7 XC7K160T by Xilinx corp.
  - supports PCIe 5.0 Gbps (Gen 2)
  - supports serdes with the data rate up to 12.5 Gbps
- Compatibility with PEXOR - PCIe 2.5 Gbps, Serdes 2.0 Gbps
- IP core
  - provides all 3 layers of PCIe protocol
  - Link speed 2.5 GT/s/
  - Lane width 4
  - PCIe Endpoint device
  - Reference clock frequency100MHz
  - Enable Bar0, memory size 4 Mbytes
  - Max payload 1024 bytes
  - Enable Interrupt



PCIe implementation - KINPEX

- IP provides an example HDL codes to process transaction layer packets (TLPs)
- 32-bit memory read/write access to control registers and 4 256 KByte dual-port-memories by modifying the example
- DMA engine developed for PEXOR is used
  - Maximum payload size of 128 bytes
  - Two mode of DMA transfer
    - DMA after arrival of complete data to 4 DPMs (DMA initiated by PC)
    - DMA via a FIFO as soon as stored data reaches payload size of 128 bytes. (DMA initiated by PCIe)
- Interrupt handling
- Arbitration



Performance

- DMA engine reaches up to 600 MBytes/sec
- Integrated system under MBS framework with several FEE cards are working stable with data transfer rate of 200 Mbytes/sec

PEXOR memory to PC memory DMA

GSI Helmholtzzentrum für Schwerionenforschung GmbH

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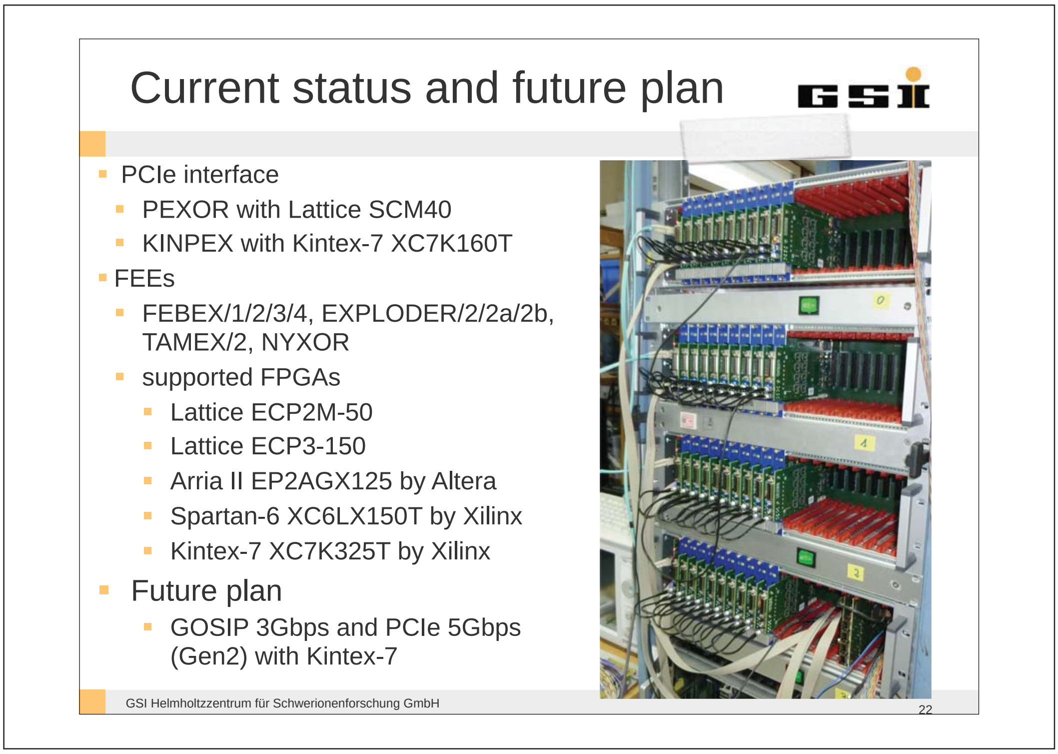
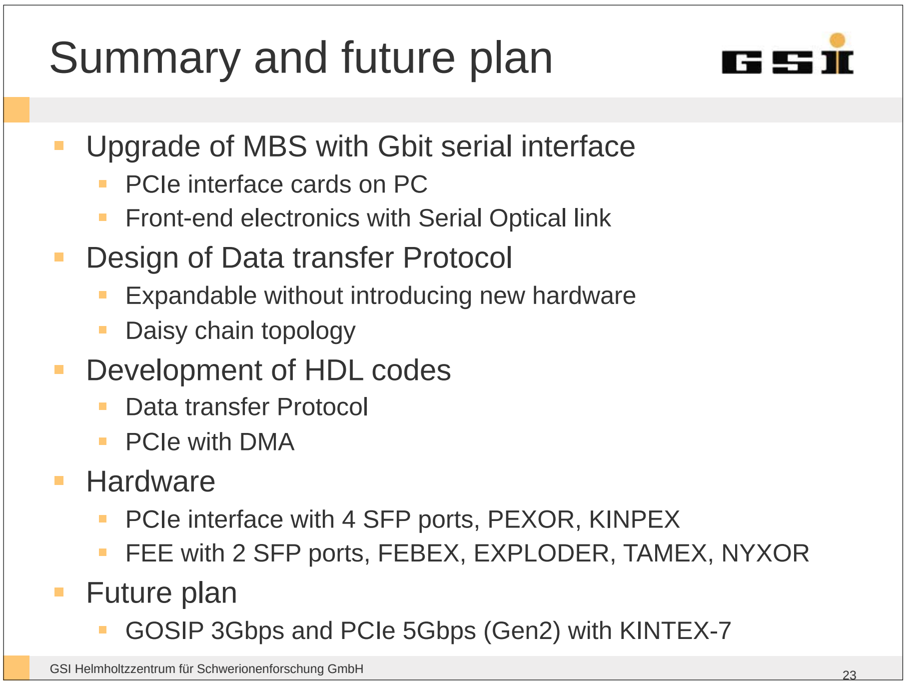


Current status and future plan

- PCIe interface
  - PEXOR with Lattice SCM40
  - KINPEX with Kintex-7 XC7K160T
- FEEs
  - FEBEX/1/2/3/4, EXPLODER/2/2a/2b, TAMEX/2, NYXOR
  - supported FPGAs
    - Lattice ECP2M-50
    - Lattice ECP3-150
    - Arria II EP2AGX125 by Altera
    - Spartan-6 XC6LX150T by Xilinx
    - Kintex-7 XC7K325T by Xilinx
- Future plan
    - GOSIP 3Gbps and PCIe 5Gbps (Gen2) with Kintex-7

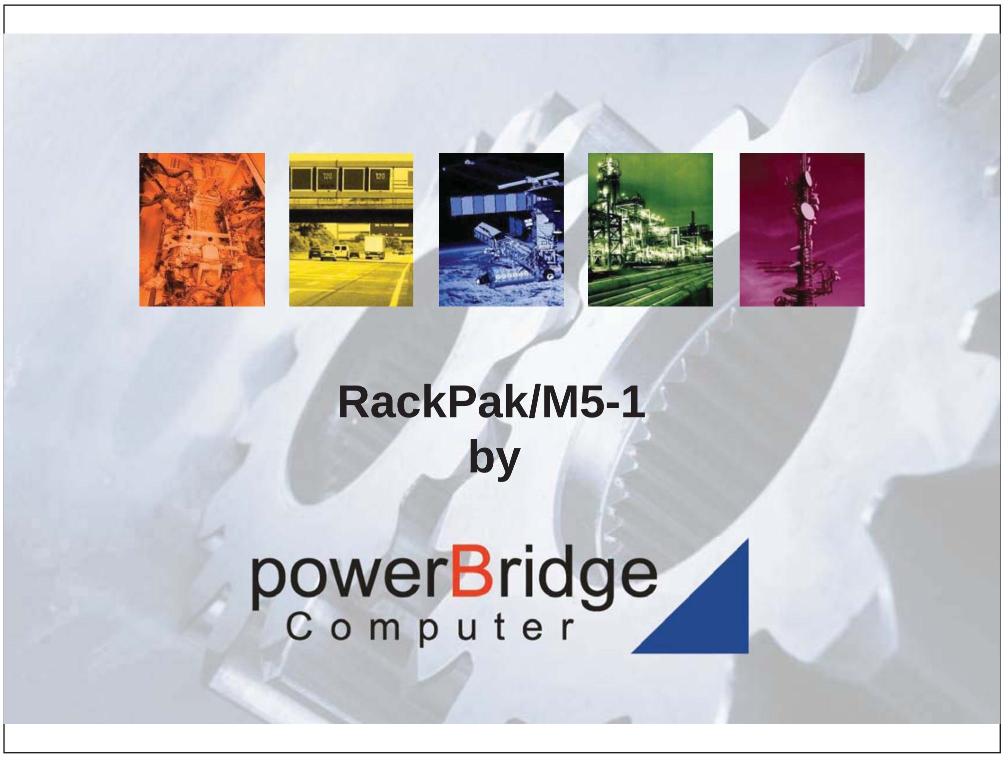
GSI Helmholtzzentrum für Schwerionenforschung GmbH

22



Summary and future plan

- Upgrade of MBS with Gbit serial interface
  - PCIe interface cards on PC
  - Front-end electronics with Serial Optical link
- Design of Data transfer Protocol
  - Expandable without introducing new hardware
  - Daisy chain topology
- Development of HDL codes
  - Data transfer Protocol
  - PCIe with DMA
- Hardware
  - PCIe interface with 4 SFP ports, PEXOR, KINPEX
  - FEE with 2 SFP ports, FEBEX, EXPLODER, TAMEX, NYXOR
- Future plan
  - GOSIP 3Gbps and PCIe 5Gbps (Gen2) with KINTEX-7



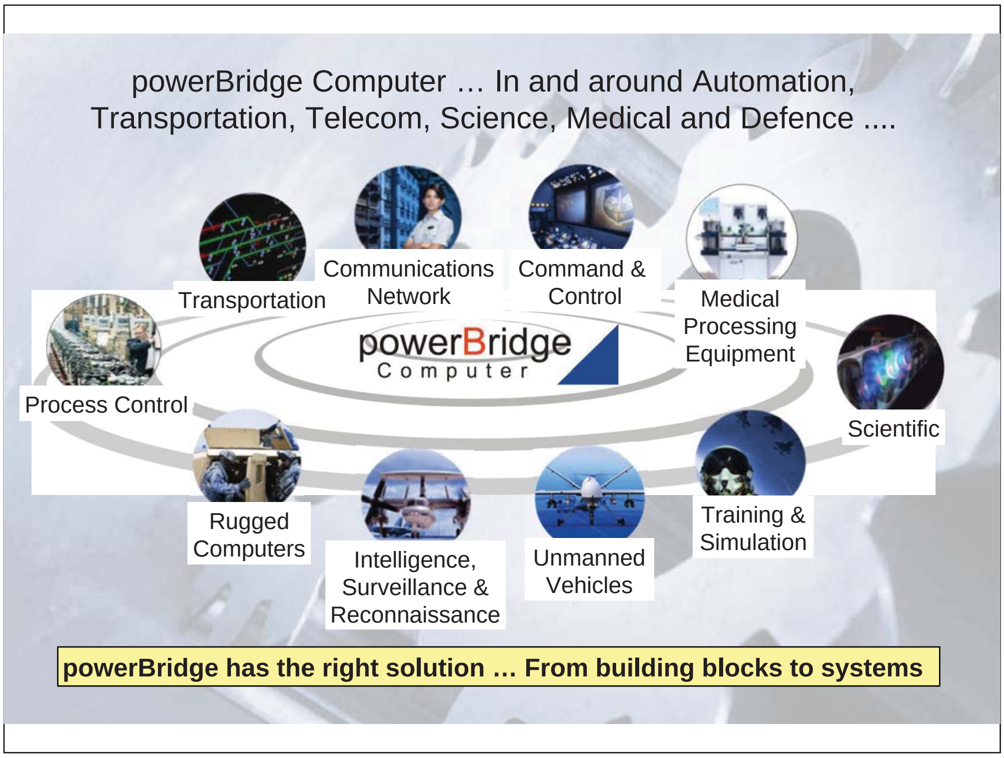
RackPak/M5-1
by

powerBridge Computer

powerBridge Computer - At A Glance

- ✦Over 20 years in the market
- ✦Privately owned
- ✦Over 25 years VME experience
- ✦Own Lab and integration facilities
- ✦powerBridge has delivered over 27.000 VME boards and 5.500 systems
- ✦PICMG member, actively working on MTCA.4 specification
- ✦ISO 9001:2008 and 14001:2009 approved

powerBridge and their partners are the backbone of VITA & PICMG Technology. We are experts of technologies.



powerBridge Computer … In and around Automation, Transportation, Telecom, Science, Medical and Defence ....

powerBridge Computer

Transportation

Communications Network

Command & Control

Medical Processing Equipment

Process Control

Scientific

Rugged Computers

Intelligence, Surveillance & Reconnaissance

Unmanned Vehicles

Training & Simulation

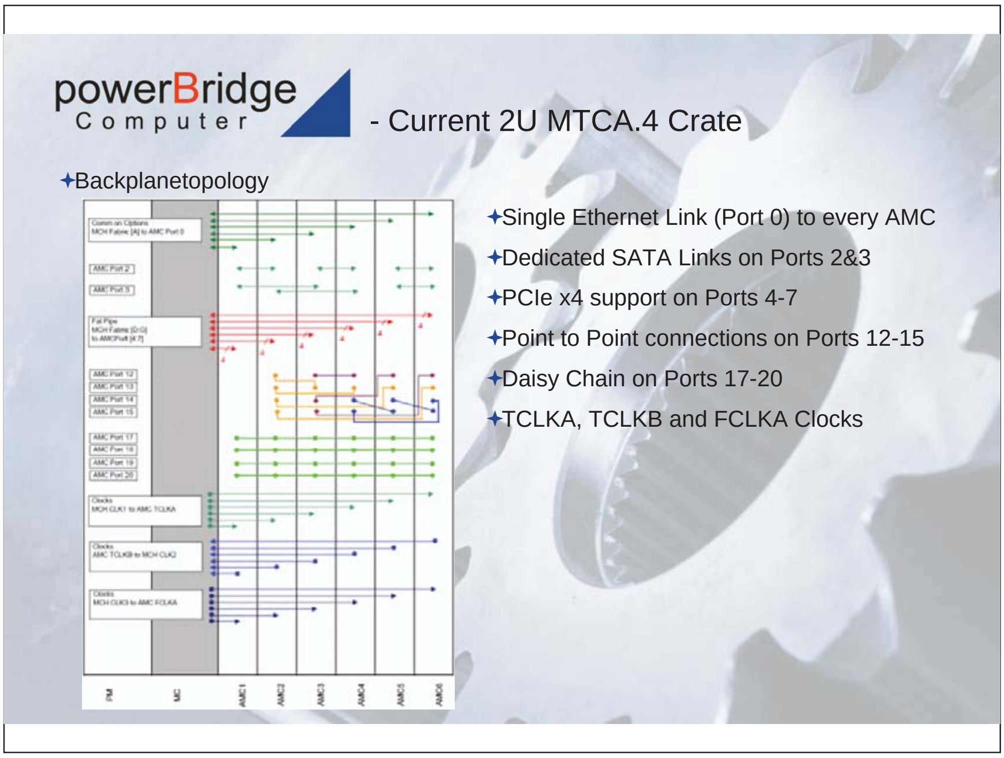
powerBridge has the right solution … From building blocks to systems

powerBridge Computer - MTCA.4 Toolbox

- MTCA.4 Starter Kits, including MCH, CPU & PM
- Carrier + Mezzanines (IP, PMC, XMC, FMC)
- AMC Modules
- SW & FW Support including BSP, source code drivers, sample applications, FPGA framework
- Spare parts, like filler modules, adapter cables, program and debug tools, test adapter

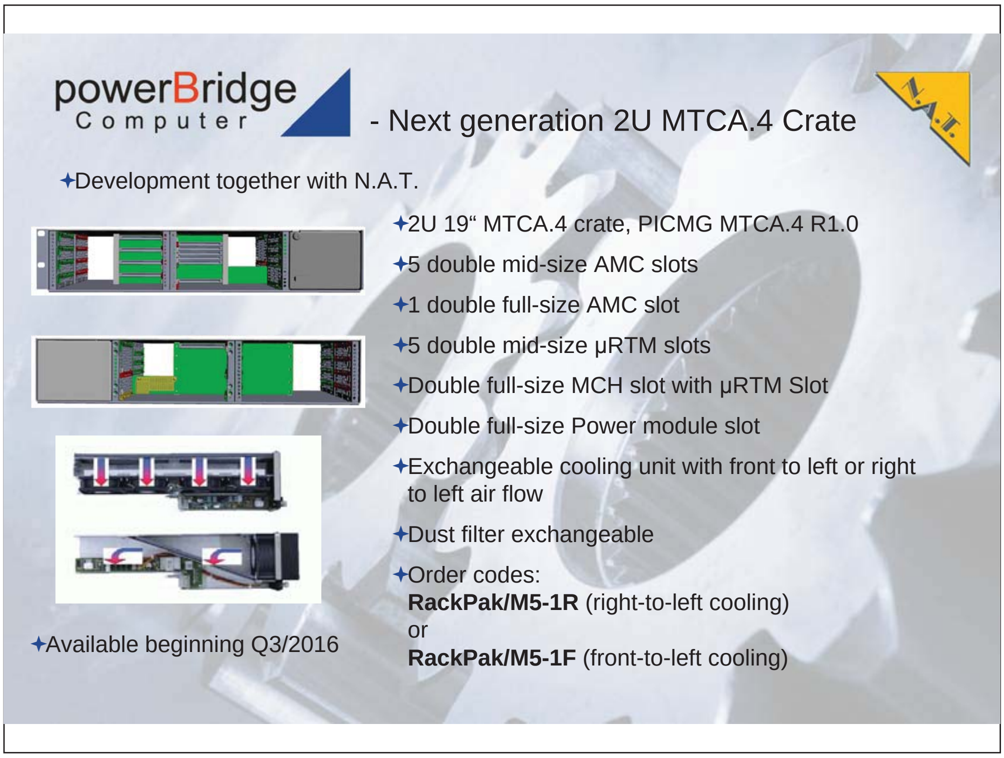
powerBridge Computer - Current 2U MTCA.4 Crate

- Current 2U MTCA.4 Crate
  - 2U 19“ MTCA.4 crate, PICMG MTCA.4 R1.0
  - 6 double mid-size AMC slots
  - 4 double mid-size μRTM slots
  - Double full-size MCH slot
  - Double full-size Power module slot
  - Exchangeable cooling unit with front to left or right to left air flow
  - Dust filter exchangeable



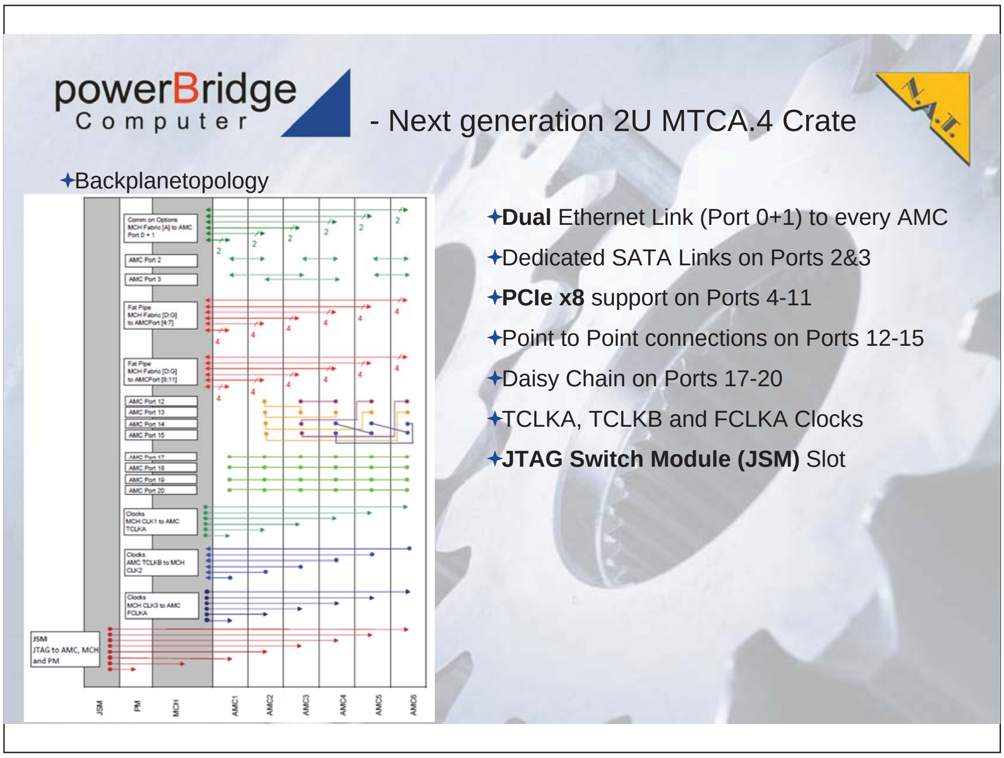
powerBridge Computer - Current 2U MTCA.4 Crate

- Backplanetopology
  - Single Ethernet Link (Port 0) to every AMC
  - Dedicated SATA Links on Ports 2&3
  - PCIe x4 support on Ports 4-7
  - Point to Point connections on Ports 12-15
  - Daisy Chain on Ports 17-20
  - TCLKA, TCLKB and FCLKA Clocks



powerBridge Computer - Next generation 2U MTCA.4 Crate

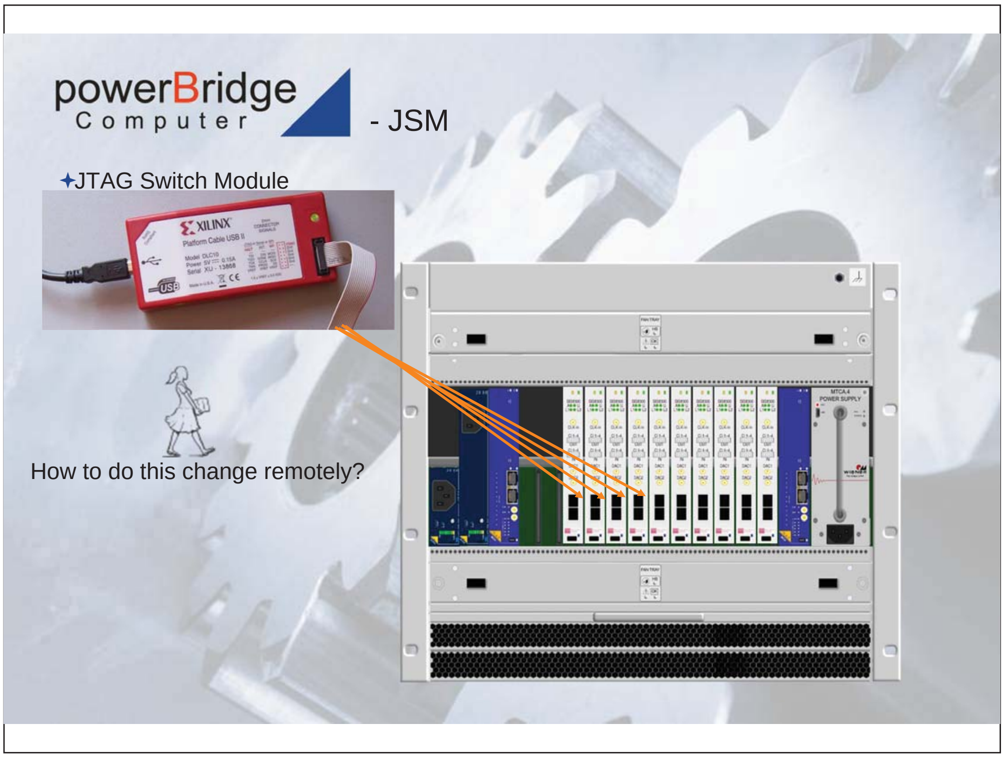
- Development together with N.A.T.
- 2U 19“ MTCA.4 crate, PICMG MTCA.4 R1.0
- 5 double mid-size AMC slots
- 1 double full-size AMC slot
- 5 double mid-size µRTM slots
- Double full-size MCH slot with µRTM Slot
- Double full-size Power module slot
- Exchangeable cooling unit with front to left or right to left air flow
- Dust filter exchangeable
- Order codes:
  RackPak/M5-1R (right-to-left cooling)
  or
  RackPak/M5-1F (front-to-left cooling)
- Available beginning Q3/2016



powerBridge Computer - Next generation 2U MTCA.4 Crate

- Backplanetopology

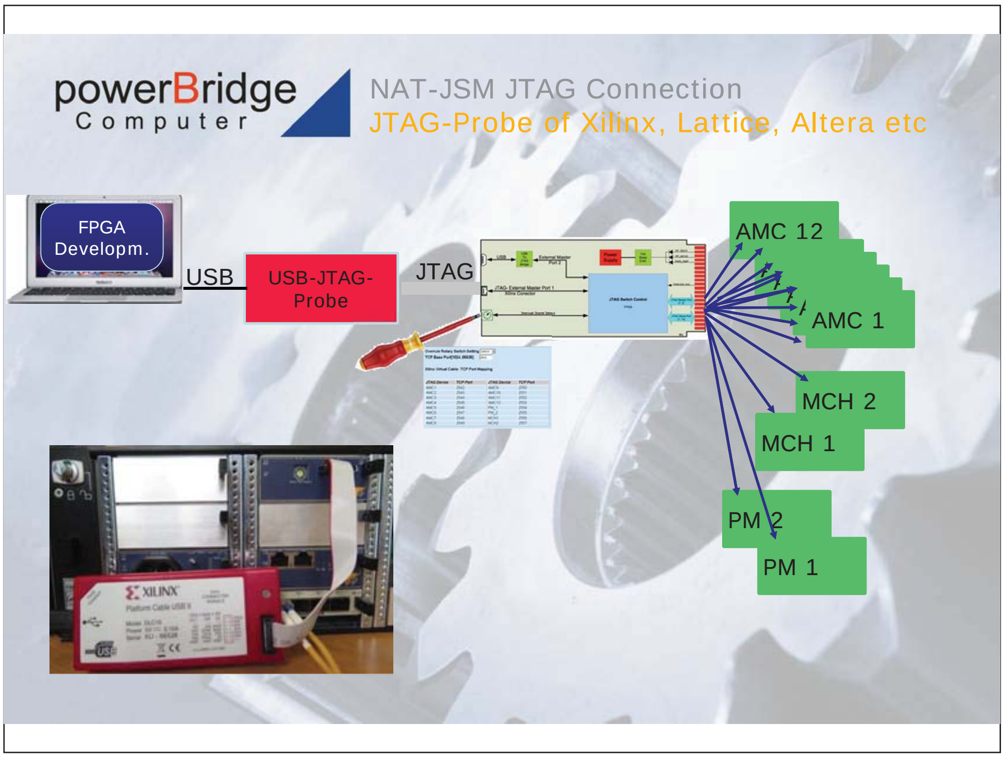
- **Dual** Ethernet Link (Port 0+1) to every AMC
- Dedicated SATA Links on Ports 2&3
- **PCIe x8** support on Ports 4-11
- Point to Point connections on Ports 12-15
- Daisy Chain on Ports 17-20
- TCLKA, TCLKB and FCLKA Clocks
- **JTAG Switch Module (JSM)** Slot



powerBridge Computer - JSM

✦JTAG Switch Module

How to do this change remotely?

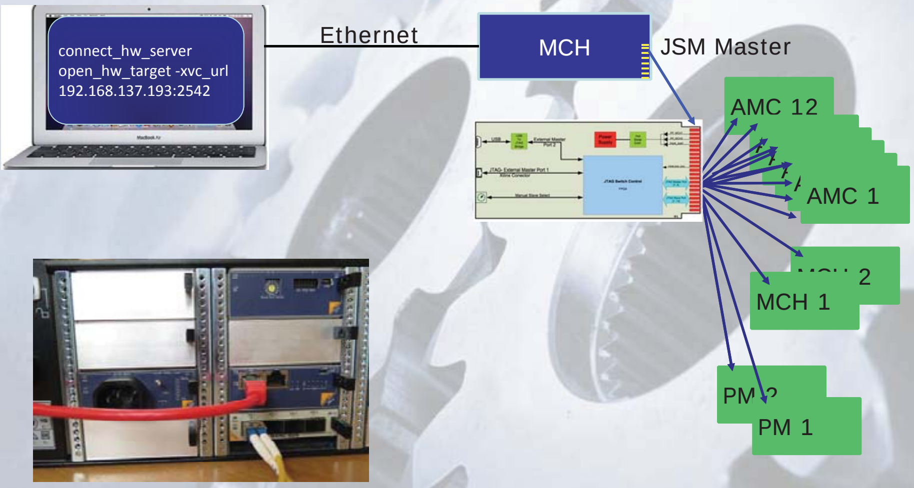


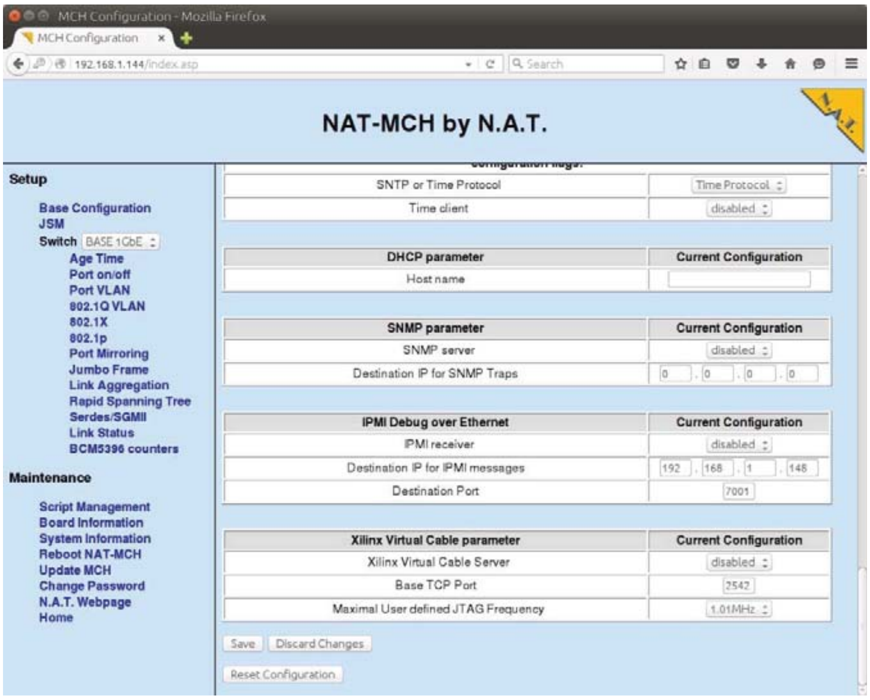
powerBridge Computer NAT-JSM JTAG Connection

JTAG-Probe of Xilinx, Lattice, Altera etc powerBridge Computer

NAT-JSM Ethernet to Xilinx HW Manager

connect_hw_server
open_hw_target -xvc_url 192.168.137.193:2542





SNTP or Time Protocol	Time Protocol
Time client	disabled

DHCP parameter	Current Configuration
Host name	

SNMP parameter	Current Configuration
SNMP server	disabled
Destination IP for SNMP Traps	0 . 0 . 0 . 0

IPMI Debug over Ethernet	Current Configuration
IPMI receiver	disabled
Destination IP for IPMI messages	192 . 168 . 1 . 148
Destination Port	7001

Xilinx Virtual Cable parameter	Current Configuration
Xilinx Virtual Cable Server	disabled
Base TCP Port	2542
Maximal User defined JTAG Frequency	1.01MHz

powerBridge Computer - Contact Information

Let´s discuss your requirements and test our performance!

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✦Email: thomas.holzapfel@powerbridge.de
✦Tel: +49-5139-9980-21

✦Kay Klockmann
✦Email: kay.klockmann@powerbridge.de
✦Tel: +49-5139-9980-15

powerBridge Computer Vertriebs GmbH,
Ehlbeek 15a, 30938 Burgwedel, Germany
http://www.powerbridge.de

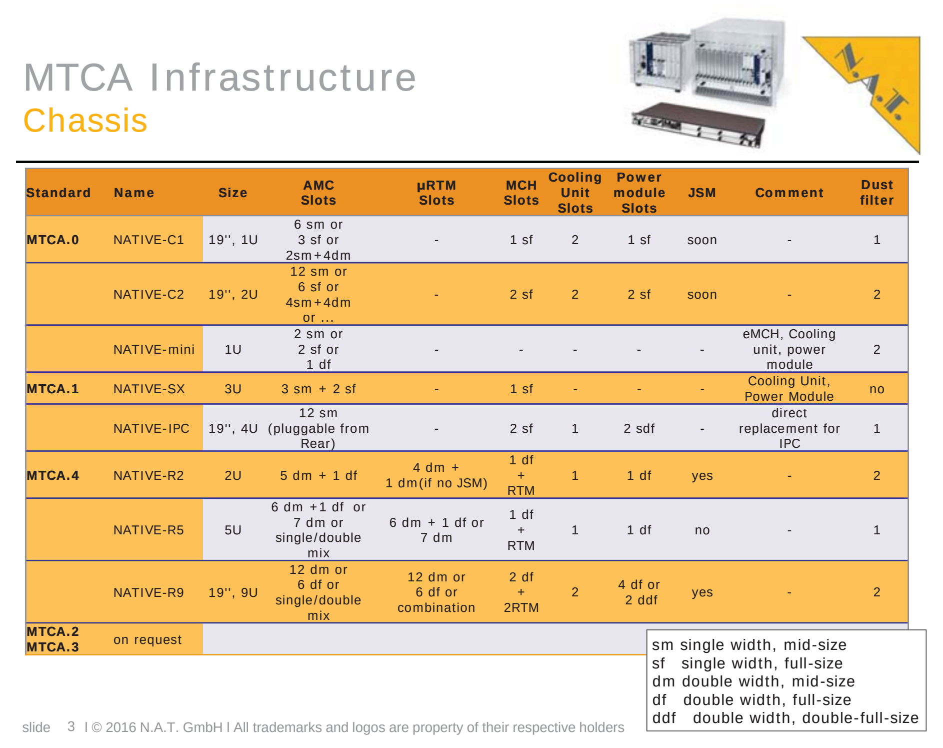
About N.A.T.

Network and Automation Technology

- Founded in 1990, privately owned
- Hard- and Software design and manufacturing
- Focus on innovation in communication
- international and worldwide operations
- Headquarters

Konrad-Zuse-Platz 9
53227 Bonn
Germany

- Instructors:
  - Dipl. Ing. Vollrath Dirksen, vollrath@nateurope.com
  - Dipl. Phys. Heiko Körte, heiko@nateurope.com

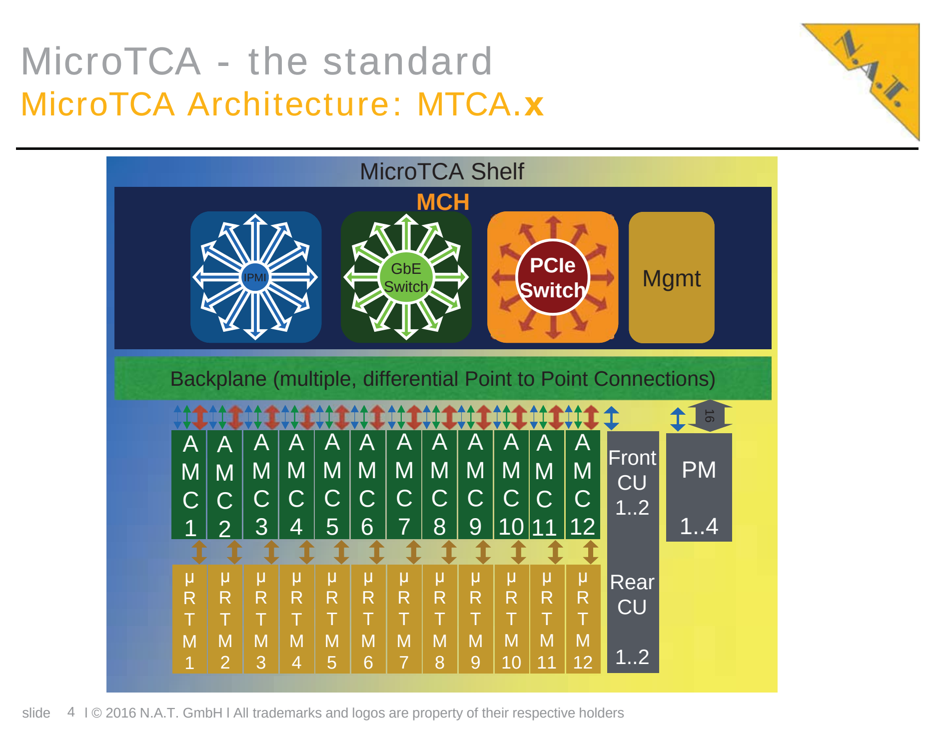


MTCA Infrastructure

Chassis

Standard	Name	Size	AMC Slots	µRTM Slots	MCH Slots	Cooling Unit Slots	Power module Slots	JSM	Comment	Dust filter
MTCA.0	NATIVE-C1	19'', 1U	6 sm or 3 sf or 2sm+4dm	-	1 sf	2	1 sf	soon	-	1
	NATIVE-C2	19'', 2U	12 sm or 6 sf or 4sm+4dm or ...	-	2 sf	2	2 sf	soon	-	2
	NATIVE-mini	1U	2 sm or 2 sf or 1 df	-	-	-	-	-	eMCH, Cooling unit, power module	2
MTCA.1	NATIVE-SX	3U	3 sm + 2 sf	-	1 sf	-	-	-	Cooling Unit, Power Module	no
	NATIVE-IPC	19'', 4U	12 sm (pluggable from Rear)	-	2 sf	1	2 sdf	-	direct replacement for IPC	1
MTCA.4	NATIVE-R2	2U	5 dm + 1 df	4 dm + 1 dm(if no JSM)	1 df + RTM	1	1 df	yes	-	2
	NATIVE-R5	5U	6 dm +1 df or 7 dm or single/double mix	6 dm + 1 df or 7 dm	1 df + RTM	1	1 df	no	-	1
	NATIVE-R9	19'', 9U	12 dm or 6 df or single/double mix	12 dm or 6 df or combination	2 df + 2RTM	2	4 df or 2 ddf	yes	-	2
MTCA.2 **MTCA.3**	on request									

sm	single width, mid-size
sf	single width, full-size
dm	double width, mid-size
df	double width, full-size
ddf	double width, double-full-size



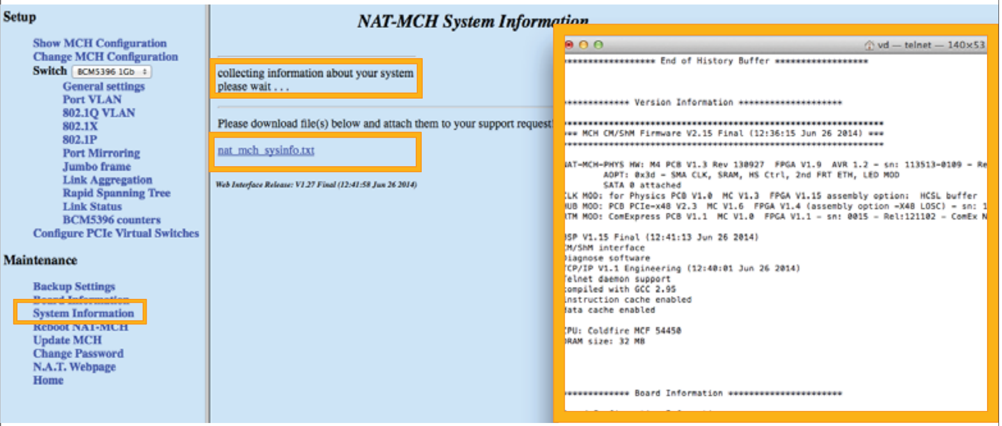
MicroTCA - the standard

MicroTCA Architecture: MTCA.**x**

NAT-MCH Maintenance Functions

System Information

- output of the following commands collected in text file:
  - history, version, bi, mch, show_pm, show_sensor_info for all FRU-IDs
  - show_fruinfo 253 (backplane)
  - show_ekey, show_link_state



Setup

Show MCH Configuration
Change MCH Configuration
Switch BCM5396 1Gb
General settings
Port VLAN
802.1Q VLAN
802.1X
802.1P
Port Mirroring
Jumbo frame
Link Aggregation
Rapid Spanning Tree
Link Status
BCM5396 counters
Configure PCIe Virtual Switches

Maintenance

Backup Settings
Board Information
System Information
Reboot NAT-MCH
Update MCH
Change Password
N.A.T. Webpage
Home

NAT-MCH System Information

collecting information about your system
please wait . . .

Please download file(s) below and attach them to your support request!

nat_mch_sysinfo.txt

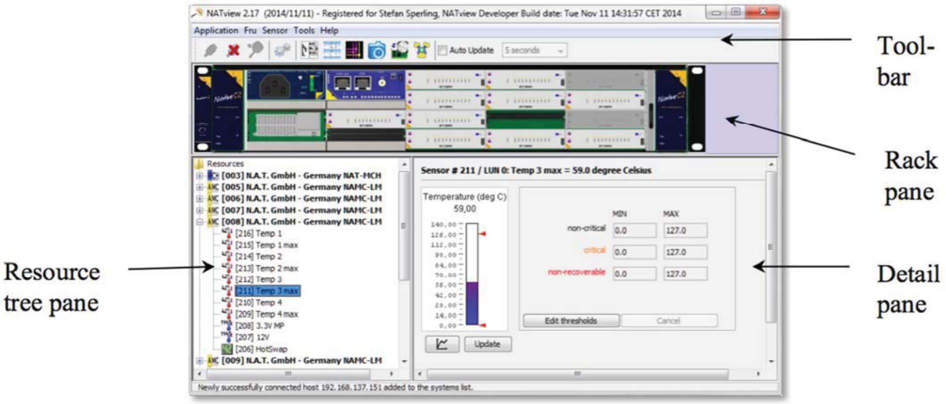
Web Interface Release: V1.27 Final (12:41:58 Jun 26 2014)

vd — telnet — 140×53

```
***************** End of History Buffer *****************



************ Version Information *******************

************************************************************
*** MCH CM/ShM Firmware V2.15 Final (12:36:15 Jun 26 2014) ***
************************************************************

NAT-MCH-PHYS HW: M4 PCB V1.3 Rev 130927  FPGA V1.9  AVR 1.2 - sn: 113513-0109 - Re
       AOPT: 0x3d - SMA CLK, SRAM, HS Ctrl, 2nd FRT ETH, LED MOD
       SATA 0 attached
CLK MOD: for Physics PCB V1.0  MC V1.3  FPGA V1.15 assembly option:  HCSL buffer
HUB MOD: PCB PCIe-x48 V2.3  MC V1.6  FPGA V1.4 (assembly option -X48 LOSC) - sn: 1
RTM MOD: ComExpress PCB V1.1  MC V1.0  FPGA V1.1 - sn: 0015 - Rel:121102 - ComEx N

BSP V1.15 Final (12:41:13 Jun 26 2014)
CM/ShM interface
Diagnose software
TCP/IP V1.1 Engineering (12:40:01 Jun 26 2014)
Telnet daemon support
compiled with GCC 2.95
instruction cache enabled
data cache enabled

CPU: Coldfire MCF 54450
DRAM size: 32 MB




************ Board Information *********************
```

Visualization Tool

NATview



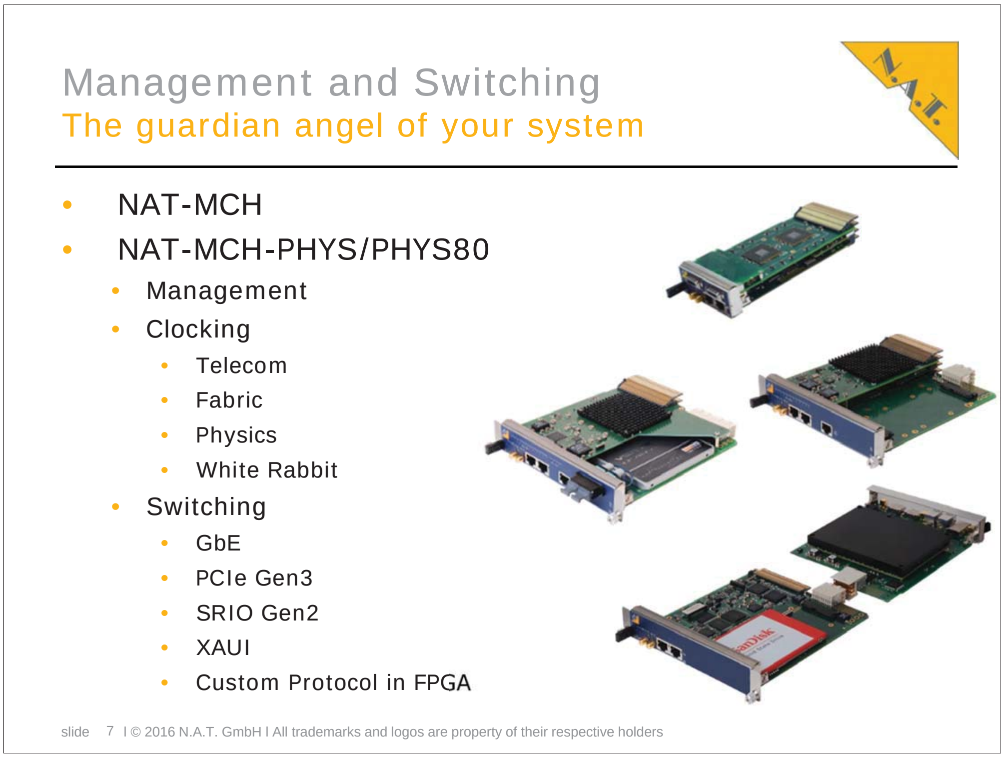
NATview 2.17 (2014/11/11) - Registered for Stefan Sperling, NATview Developer Build date: Tue Nov 11 14:31:57 CET 2014

[003] N.A.T. GmbH - Germany NAT-MCH
[005] N.A.T. GmbH - Germany NAMC-LM
[006] N.A.T. GmbH - Germany NAMC-LM
[007] N.A.T. GmbH - Germany NAMC-LM
[008] N.A.T. GmbH - Germany NAMC-LM
  [216] Temp 1
  [215] Temp 1 max
  [214] Temp 2
  [213] Temp 2 max
  [212] Temp 3
  [211] Temp 3 max
  [210] Temp 4
  [209] Temp 4 max
  [208] 3.3V MP
  [207] 12V
  [206] HotSwap
[009] N.A.T. GmbH - Germany NAMC-LM

Sensor # 211 / LUN 0: Temp 3 max = 59.0 degree Celsius

	MIN	MAX
non-critical	0.0	127.0
critical	0.0	127.0
non-recoverable	0.0	127.0

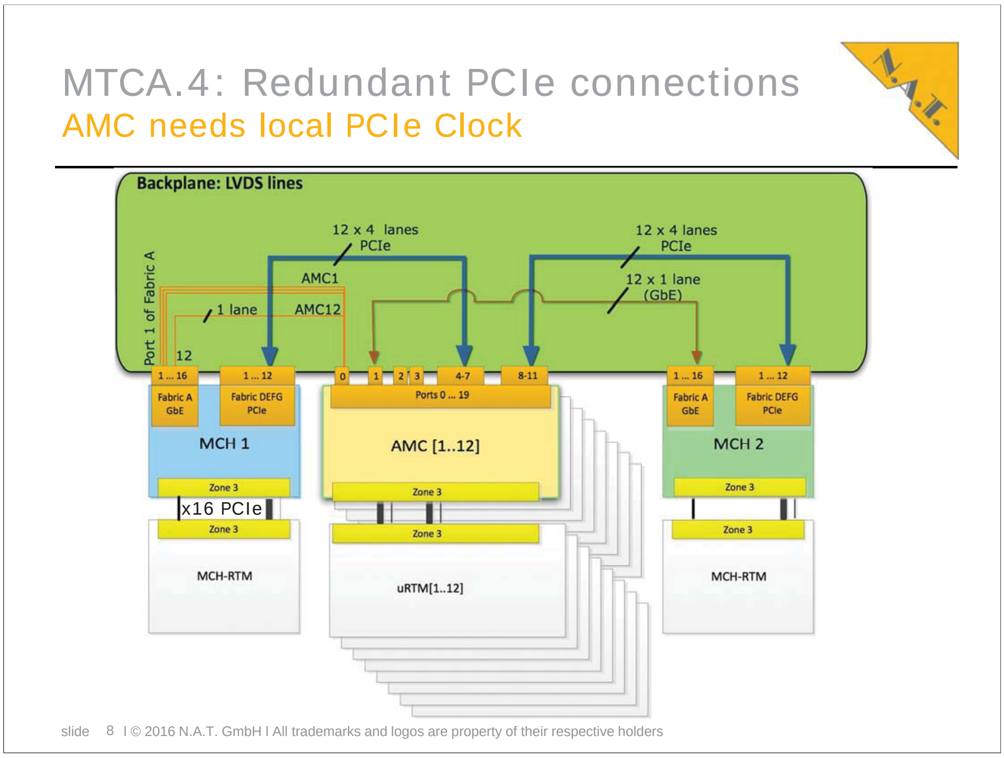
Newly successfully connected host 192.168.137.151 added to the systems list.



Management and Switching

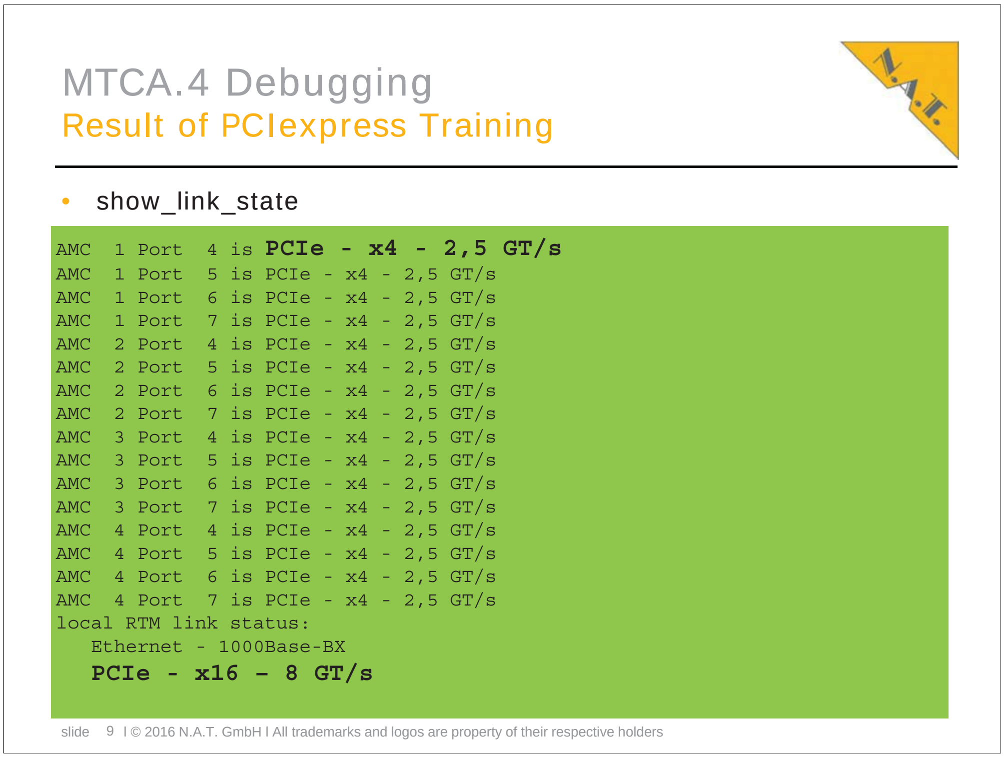
The guardian angel of your system

- NAT-MCH
- NAT-MCH-PHYS/PHYS80
  - Management
  - Clocking
    - Telecom
    - Fabric
    - Physics
    - White Rabbit
  - Switching
    - GbE
    - PCIe Gen3
    - SRIO Gen2
    - XAUI
    - Custom Protocol in FPGA



MTCA.4: Redundant PCIe connections

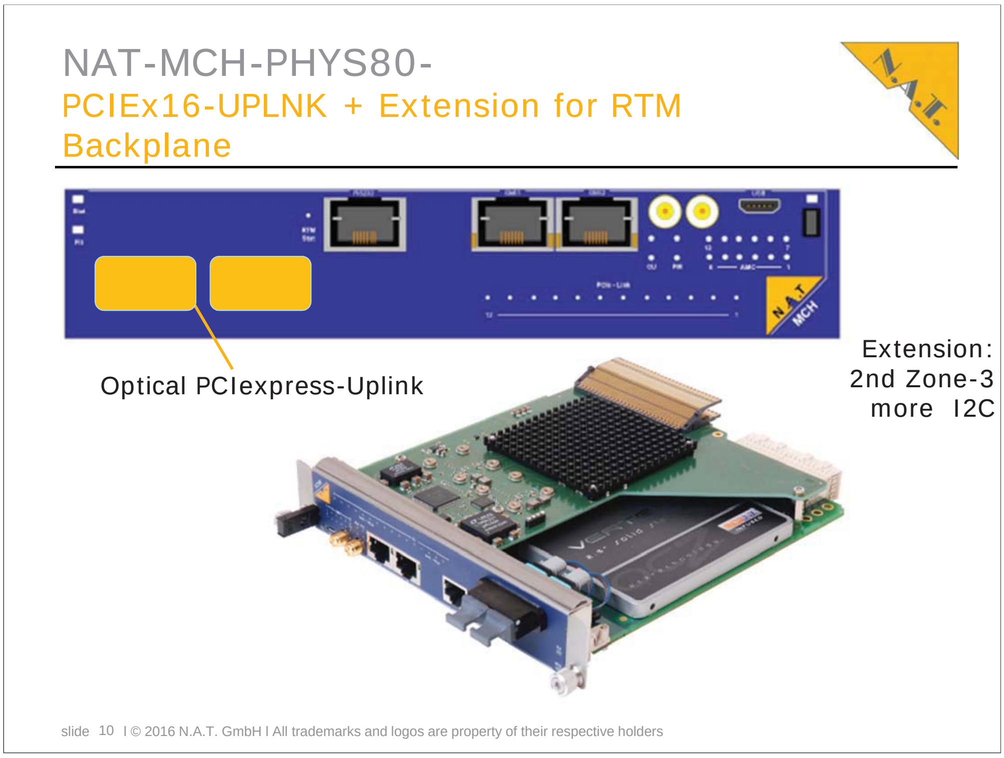
AMC needs local PCIe Clock



MTCA.4 Debugging
Result of PCIexpress Training

- show_link_state

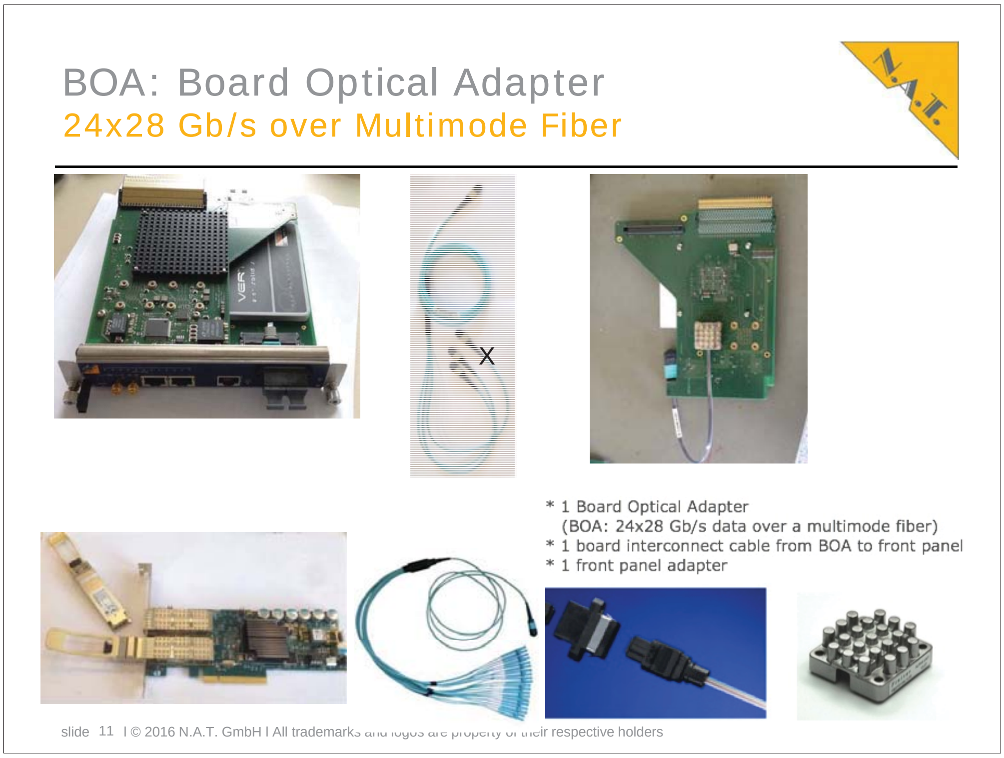
```
AMC  1 Port  4 is PCIe - x4 - 2,5 GT/s
AMC  1 Port  5 is PCIe - x4 - 2,5 GT/s
AMC  1 Port  6 is PCIe - x4 - 2,5 GT/s
AMC  1 Port  7 is PCIe - x4 - 2,5 GT/s
AMC  2 Port  4 is PCIe - x4 - 2,5 GT/s
AMC  2 Port  5 is PCIe - x4 - 2,5 GT/s
AMC  2 Port  6 is PCIe - x4 - 2,5 GT/s
AMC  2 Port  7 is PCIe - x4 - 2,5 GT/s
AMC  3 Port  4 is PCIe - x4 - 2,5 GT/s
AMC  3 Port  5 is PCIe - x4 - 2,5 GT/s
AMC  3 Port  6 is PCIe - x4 - 2,5 GT/s
AMC  3 Port  7 is PCIe - x4 - 2,5 GT/s
AMC  4 Port  4 is PCIe - x4 - 2,5 GT/s
AMC  4 Port  5 is PCIe - x4 - 2,5 GT/s
AMC  4 Port  6 is PCIe - x4 - 2,5 GT/s
AMC  4 Port  7 is PCIe - x4 - 2,5 GT/s
local RTM link status:
   Ethernet - 1000Base-BX
   PCIe - x16 – 8 GT/s
```



NAT-MCH-PHYS80-
PCIEx16-UPLNK + Extension for RTM Backplane

Optical PCIexpress-Uplink

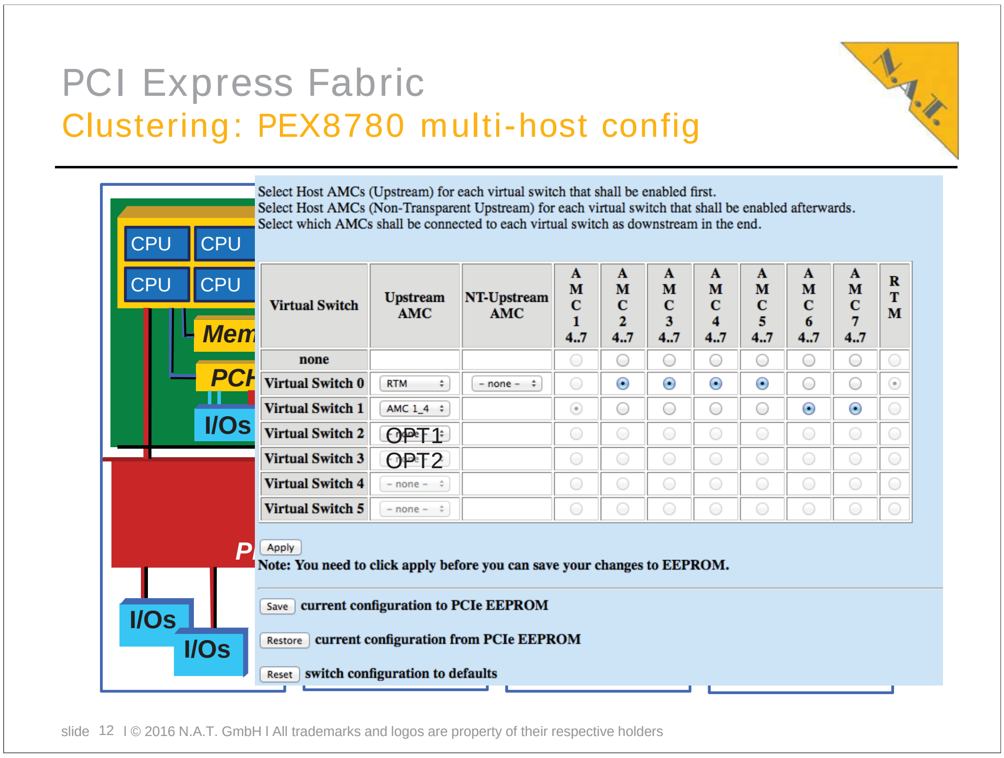
Extension:
2nd Zone-3
more I2C



BOA: Board Optical Adapter

24x28 Gb/s over Multimode Fiber

* 1 Board Optical Adapter
(BOA: 24x28 Gb/s data over a multimode fiber)
* 1 board interconnect cable from BOA to front panel
* 1 front panel adapter



PCI Express Fabric

Clustering: PEX8780 multi-host config

Select Host AMCs (Upstream) for each virtual switch that shall be enabled first.
Select Host AMCs (Non-Transparent Upstream) for each virtual switch that shall be enabled afterwards.
Select which AMCs shall be connected to each virtual switch as downstream in the end.

Virtual Switch	Upstream AMC	NT-Upstream AMC	AMC 1 4..7	AMC 2 4..7	AMC 3 4..7	AMC 4 4..7	AMC 5 4..7	AMC 6 4..7	AMC 7 4..7	RTM
none			○	○	○	○	○	○	○	○
Virtual Switch 0	RTM	– none –	○	●	●	●	●	○	○	⊙
Virtual Switch 1	AMC 1_4		⊙	○	○	○	○	●	●	○
Virtual Switch 2	OPT1		○	○	○	○	○	○	○	○
Virtual Switch 3	OPT2		○	○	○	○	○	○	○	○
Virtual Switch 4	– none –		○	○	○	○	○	○	○	○
Virtual Switch 5	– none –		○	○	○	○	○	○	○	○

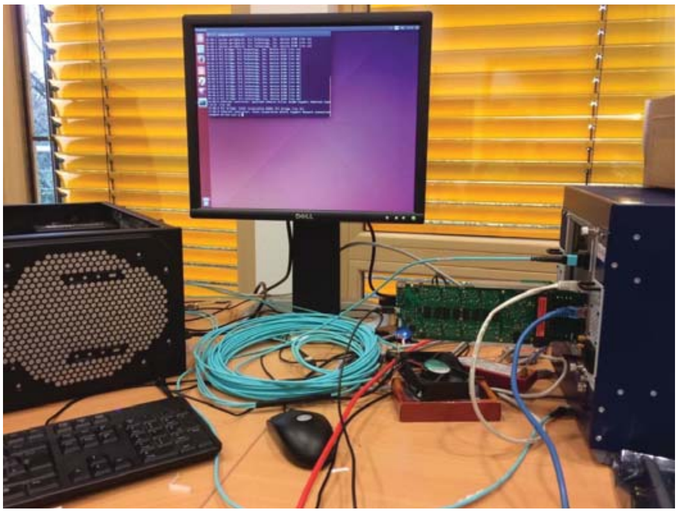
Note: You need to click apply before you can save your changes to EEPROM.

Save **current configuration to PCIe EEPROM**

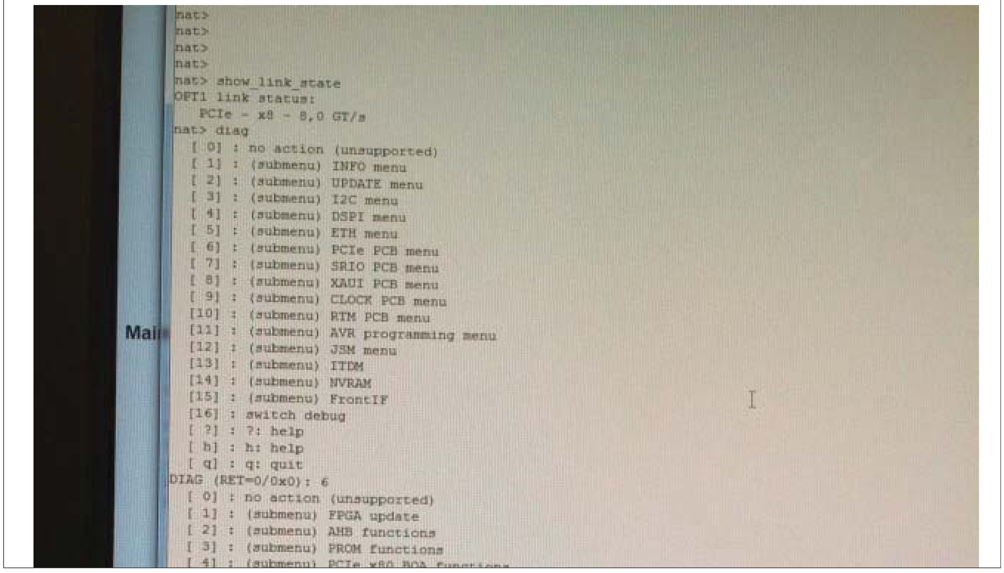
Restore **current configuration from PCIe EEPROM**

Reset **switch configuration to defaults**

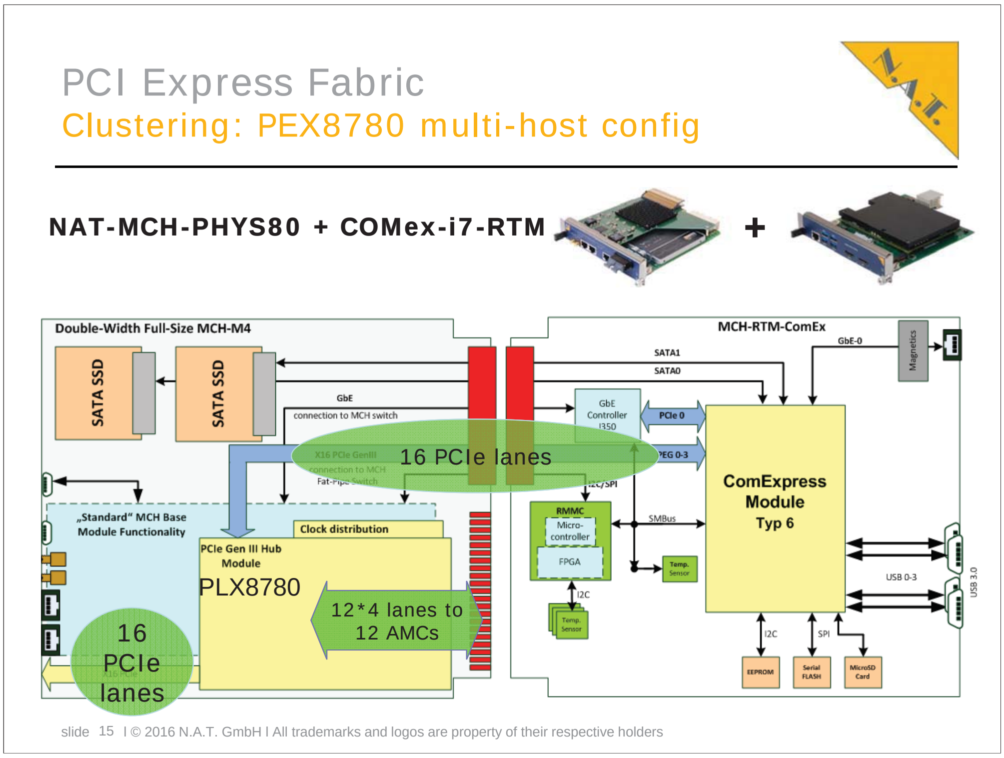
Example
8 optical PCIe lanes to external PC



Example Error Counter
8 optical PCIe Uplinks

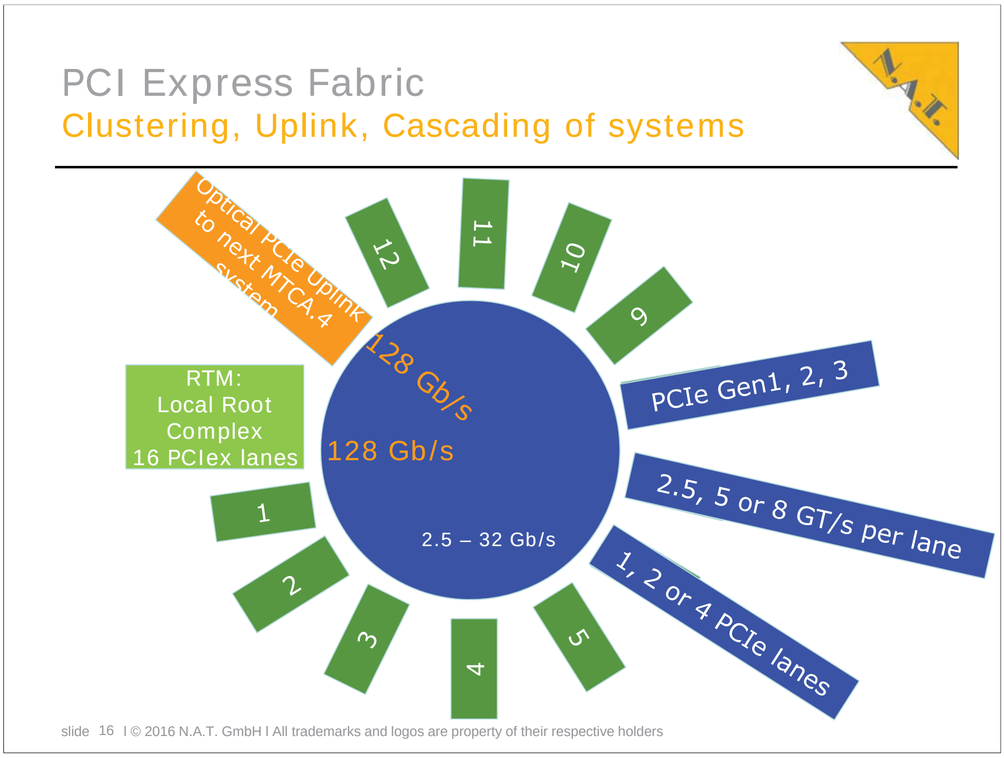


```
nat>
nat>
nat>
nat>
nat> show_link_state
OPT1 link status:
   PCIe - x8 - 8,0 GT/s
nat> diag
  [ 0] : no action (unsupported)
  [ 1] : (submenu) INFO menu
  [ 2] : (submenu) UPDATE menu
  [ 3] : (submenu) I2C menu
  [ 4] : (submenu) DSPI menu
  [ 5] : (submenu) ETH menu
  [ 6] : (submenu) PCIe PCB menu
  [ 7] : (submenu) SRIO PCB menu
  [ 8] : (submenu) XAUI PCB menu
  [ 9] : (submenu) CLOCK PCB menu
  [10] : (submenu) RTM PCB menu
  [11] : (submenu) AVR programming menu
  [12] : (submenu) JSM menu
  [13] : (submenu) ITDM
  [14] : (submenu) NVRAM
  [15] : (submenu) FrontIF
  [16] : switch debug
  [ ?] : ?: help
  [ h] : h: help
  [ q] : q: quit
DIAG (RET=0/0x0): 6
  [ 0] : no action (unsupported)
  [ 1] : (submenu) FPGA update
  [ 2] : (submenu) AHB functions
  [ 3] : (submenu) PROM functions
  [ 4] : (submenu) PCIe x80 BOA functions
```



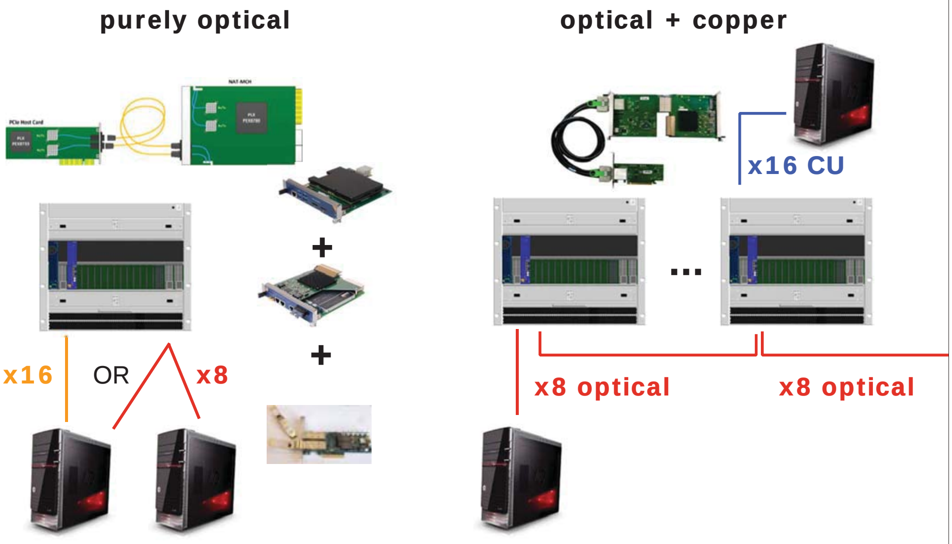
PCI Express Fabric
Clustering: PEX8780 multi-host config

NAT-MCH-PHYS80 + COMex-i7-RTM +



PCI Express Fabric
Clustering, Uplink, Cascading of systems

PCI Express Fabric
Uplink/Cascading: PCIe Gen3 examples



purely optical

optical + copper

x16 CU

x16 OR **x8**

+

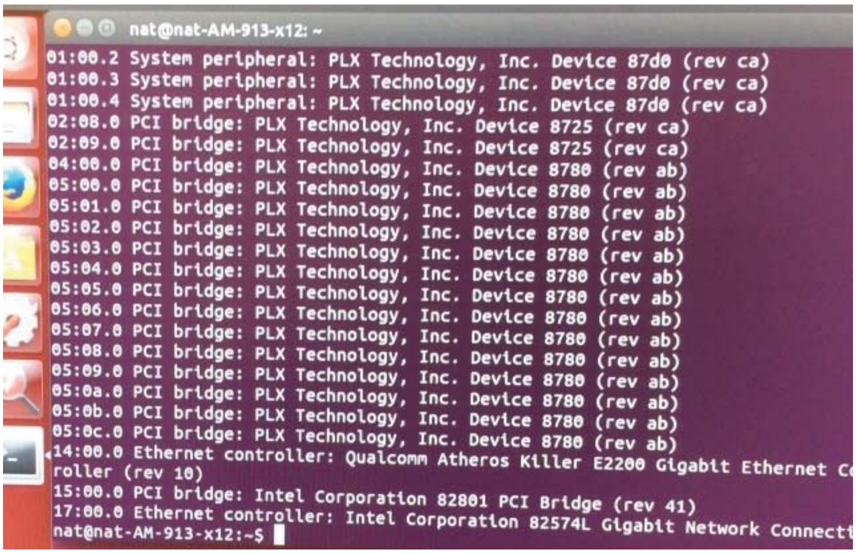
+

...

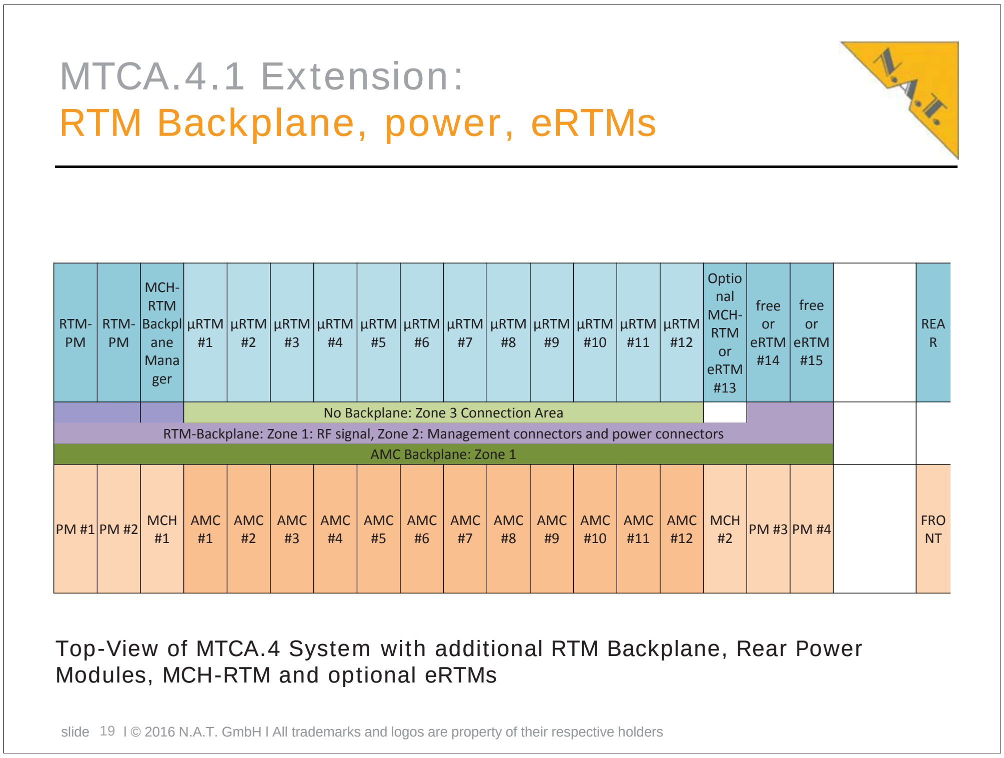
x8 optical

x8 optical

Example: 14 PCIe slots
Cascading of two MTCA.4 chassis



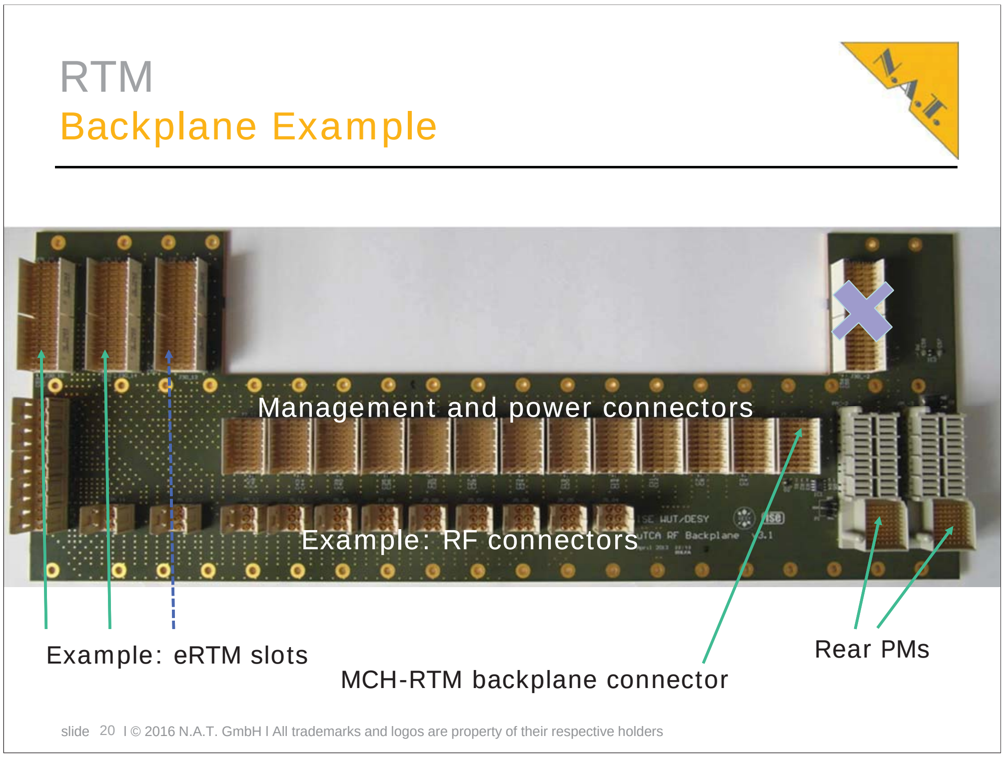
```
nat@nat-AM-913-x12: ~
01:00.2 System peripheral: PLX Technology, Inc. Device 87d0 (rev ca)
01:00.3 System peripheral: PLX Technology, Inc. Device 87d0 (rev ca)
01:00.4 System peripheral: PLX Technology, Inc. Device 87d0 (rev ca)
02:08.0 PCI bridge: PLX Technology, Inc. Device 8725 (rev ca)
02:09.0 PCI bridge: PLX Technology, Inc. Device 8725 (rev ca)
04:00.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:00.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:01.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:02.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:03.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:04.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:05.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:06.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:07.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:08.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:09.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:0a.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:0b.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
05:0c.0 PCI bridge: PLX Technology, Inc. Device 8780 (rev ab)
14:00.0 Ethernet controller: Qualcomm Atheros Killer E2200 Gigabit Ethernet C
roller (rev 10)
15:00.0 PCI bridge: Intel Corporation 82801 PCI Bridge (rev 41)
17:00.0 Ethernet controller: Intel Corporation 82574L Gigabit Network Connect
nat@nat-AM-913-x12:~$
```



MTCA.4.1 Extension:
RTM Backplane, power, eRTMs

RTM-PM	RTM-PM	MCH-RTM Backplane Manager	µRTM #1	µRTM #2	µRTM #3	µRTM #4	µRTM #5	µRTM #6	µRTM #7	µRTM #8	µRTM #9	µRTM #10	µRTM #11	µRTM #12	Optional MCH-RTM or eRTM #13	free or eRTM #14	free or eRTM #15		REAR
			No Backplane: Zone 3 Connection Area																
RTM-Backplane: Zone 1: RF signal, Zone 2: Management connectors and power connectors																			
AMC Backplane: Zone 1																			
PM #1	PM #2	MCH #1	AMC #1	AMC #2	AMC #3	AMC #4	AMC #5	AMC #6	AMC #7	AMC #8	AMC #9	AMC #10	AMC #11	AMC #12	MCH #2	PM #3	PM #4		FRONT

Top-View of MTCA.4 System with additional RTM Backplane, Rear Power Modules, MCH-RTM and optional eRTMs



RTM
Backplane Example

Management and power connectors

Example: RF connectors

Example: eRTM slots

MCH-RTM backplane connector

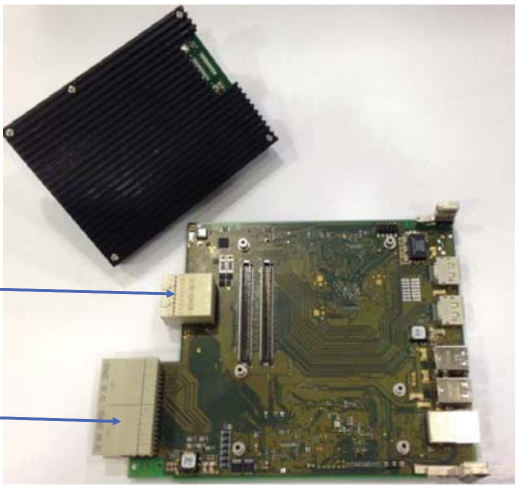
Rear PMs

Low Level RF Backplane
NAT-MCH-RTM-RF: new RTM

Optional:
COMexpress-CPU-Module

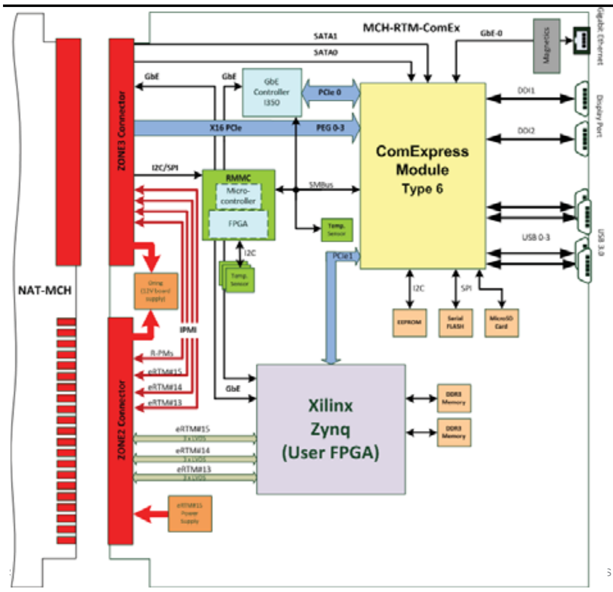
RTM Power connector
RTM Control&Data connector

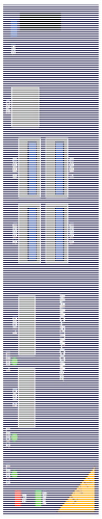
Second Zone3 connector



MTCA.4 Enhancement (coming soon)
μRTMs (Zone 1,2,3), eRTM15 and MCH-RTM-BM

Low Level RF Backplane
NAT-MCH-RTM-RF: new RTM



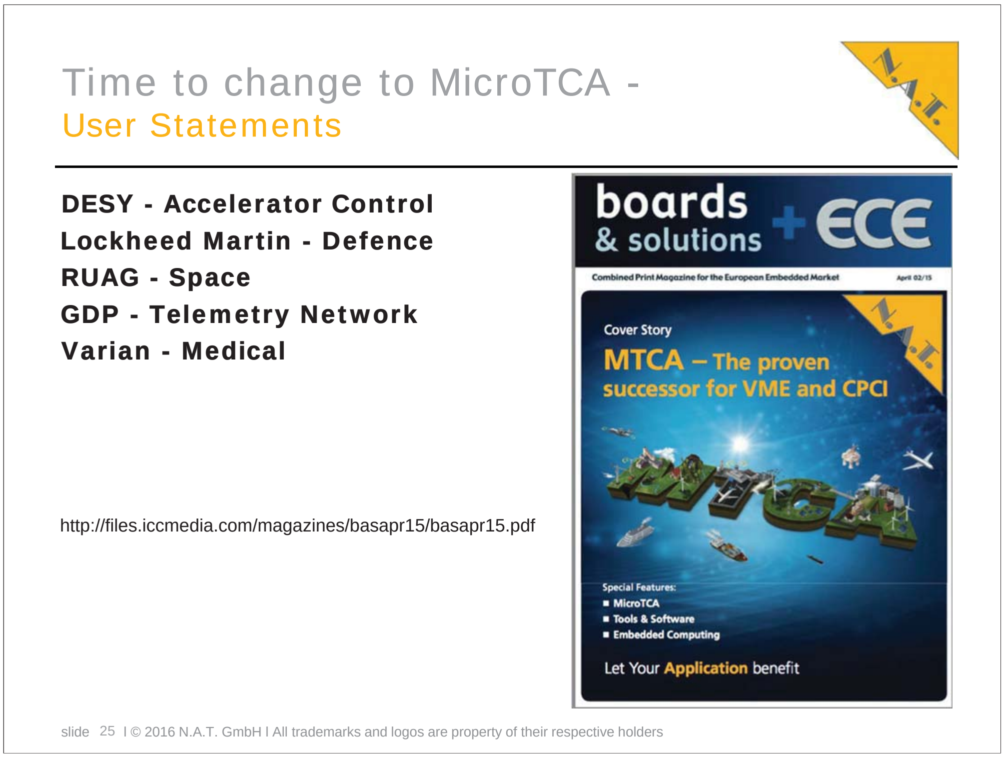


MicroTCA
Markets

- 1 or 2 “big“ standards in our work life
  - VME, PCI, cPCI ....
- MicroTCA and AMCs will be the next dominating standards for industrial systems
  - nothing real new but better and different
  - one standard meeting requirements of many different vertical markets

❾ MicroTCA is important already !

❾ MicroTCA will become even more important in the future !



Time to change to MicroTCA -
User Statements

DESY - Accelerator Control
Lockheed Martin - Defence
RUAG - Space
GDP - Telemetry Network
Varian - Medical

http://files.iccmedia.com/magazines/basapr15/basapr15.pdf

Thank you very much!
Questions?

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53227 Bonn, Germany

www.nateurope.com

Let Your Application

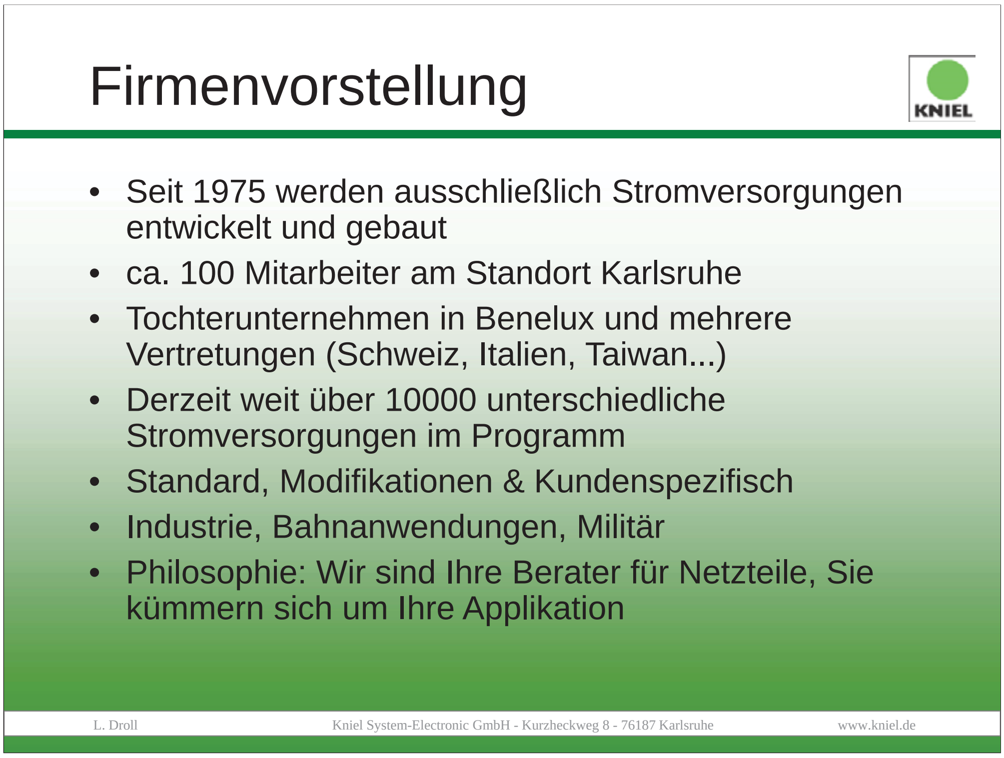
Dates Training:
visit
mtca.eu
support-> training

ope.com

Kniel macht den Unterschied

Stromversorgungen

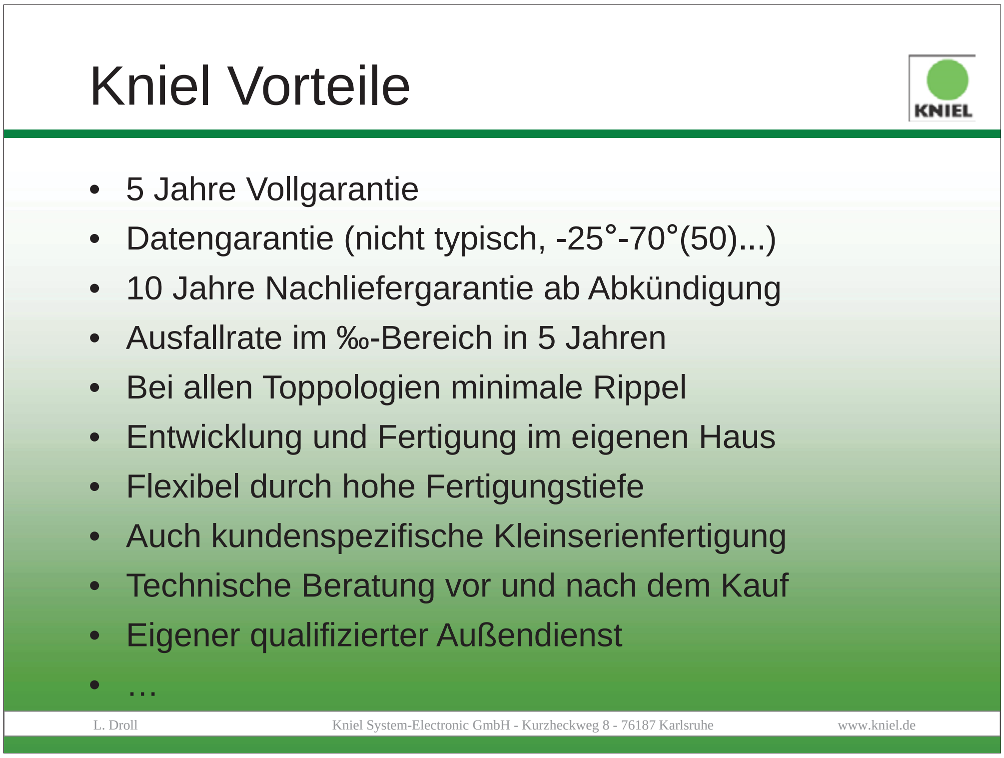
für die empfindliche Messtechnik
und die komplexe Automatisierung



Firmenvorstellung

- Seit 1975 werden ausschließlich Stromversorgungen entwickelt und gebaut
- ca. 100 Mitarbeiter am Standort Karlsruhe
- Tochterunternehmen in Benelux und mehrere Vertretungen (Schweiz, Italien, Taiwan...)
- Derzeit weit über 10000 unterschiedliche Stromversorgungen im Programm
- Standard, Modifikationen & Kundenspezifisch
- Industrie, Bahnanwendungen, Militär
- Philosophie: Wir sind Ihre Berater für Netzteile, Sie kümmern sich um Ihre Applikation

L. Droll Kniel System-Electronic GmbH - Kurzheckweg 8 - 76187 Karlsruhe www.kniel.de



Kniel Vorteile

- 5 Jahre Vollgarantie
- Datengarantie (nicht typisch, -25°-70°(50)...)
- 10 Jahre Nachliefergarantie ab Abkündigung
- Ausfallrate im ‰-Bereich in 5 Jahren
- Bei allen Toppologien minimale Rippel
- Entwicklung und Fertigung im eigenen Haus
- Flexibel durch hohe Fertigungstiefe
- Auch kundenspezifische Kleinserienfertigung
- Technische Beratung vor und nach dem Kauf
- Eigener qualifizierter Außendienst
- …

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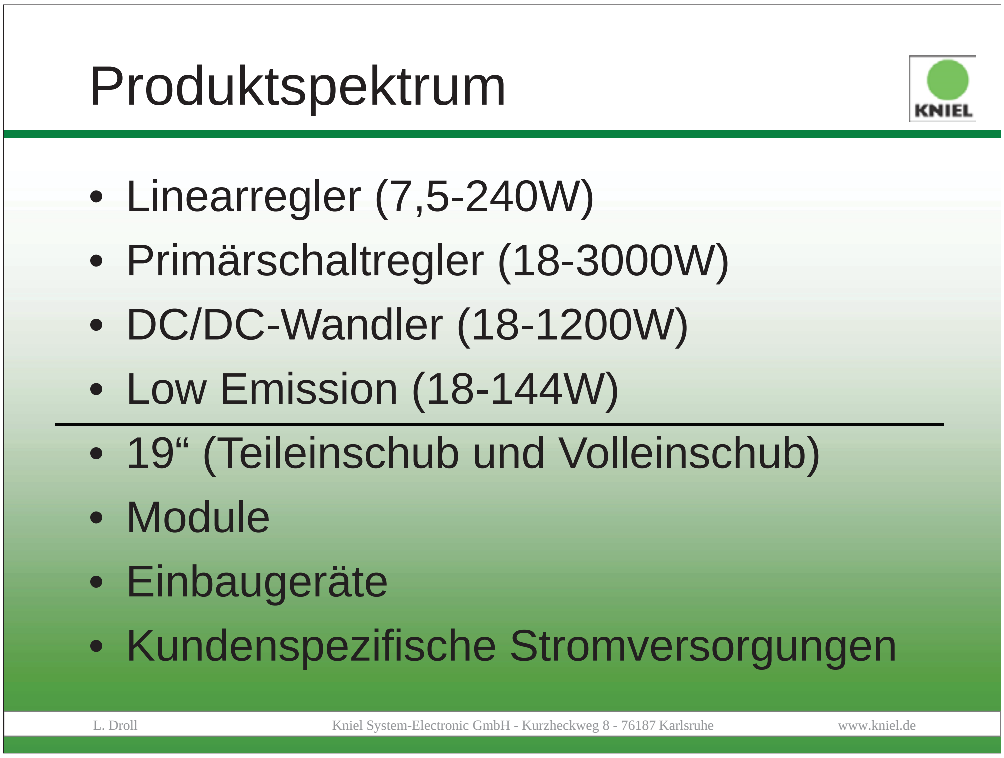

Produktspektrum

- Linearregler (7,5-240W)
- Primärschaltregler (18-3000W)
- DC/DC-Wandler (18-1200W)
- Low Emission (18-144W)
- 19“ (Teileinschub und Volleinschub)
- Module
- Einbaugeräte
- Kundenspezifische Stromversorgungen

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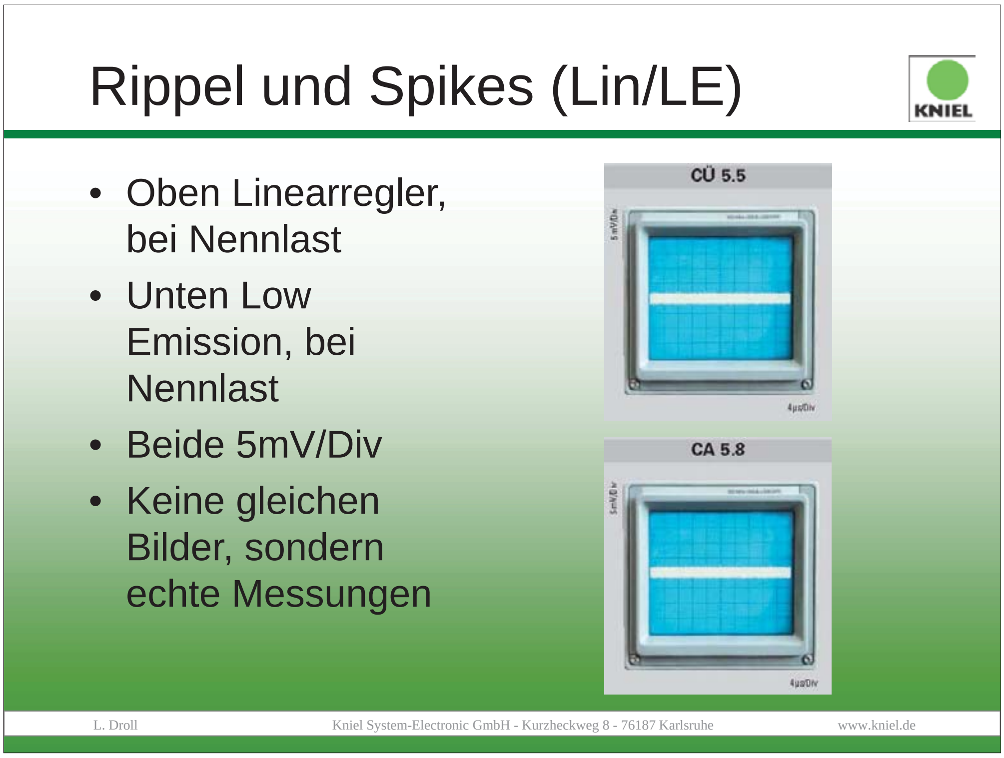
Low Emission (incl. NRTL-Abnahme)

- ✓ Vereint die **Vorteile** von Linear- und Schaltregler
- ✓ Geringe Spikes und Rippel von Linearregler

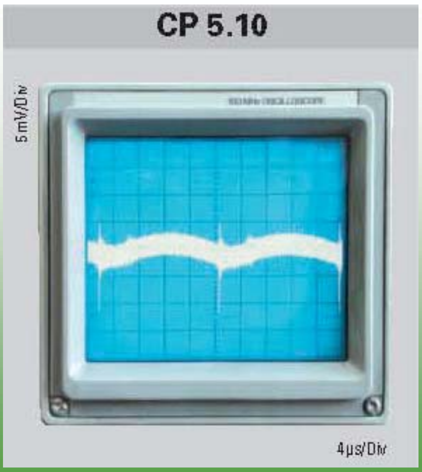


Rippel und Spikes (Lin/LE)

- Oben Linearregler, bei Nennlast
- Unten Low Emission, bei Nennlast
- Beide 5mV/Div
- Keine gleichen Bilder, sondern echte Messungen

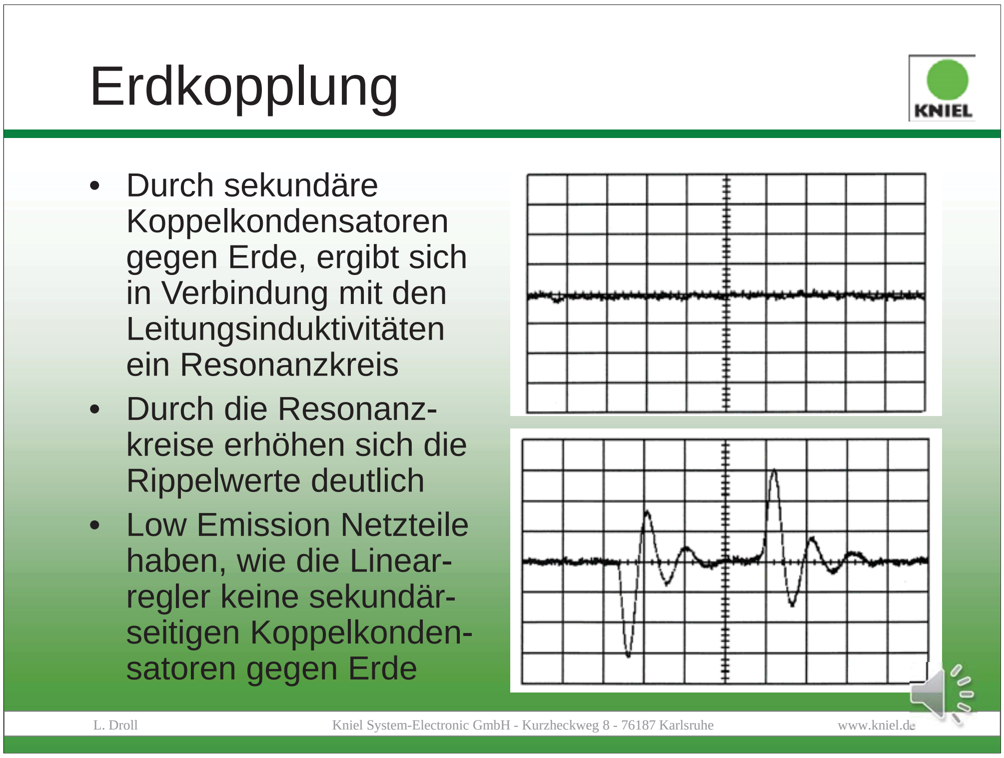
Rippel & Spikes (Schaltregler)

- Deutlicher Schaltfrequenzrippel
- Überlagerte Spikes
- 5mV/Div
- Durch Kondensatoren gegen Erde werden die Rippel in der Anwendung noch erhöht



Low Emission (incl. NRTL-Abnahme)

- ✓ Vereint die **Vorteile** von Linear- und Schaltregler
- ✓ Geringe Spikes und Rippel von Linearregler
- ✓ Geringe Größe, Gewicht und hoher Wirkungsgrad vom Schaltregler
- ✓ Keine rückschaltende Kennlinie
- ✓ Keine sekundäre Kopplung zu Erde, auch nicht über Kondensatoren



Erdkopplung

- Durch sekundäre Koppelkondensatoren gegen Erde, ergibt sich in Verbindung mit den Leitungsinduktivitäten ein Resonanzkreis
- Durch die Resonanzkreise erhöhen sich die Rippelwerte deutlich
- Low Emission Netzteile haben, wie die Linearregler keine sekundärseitigen Koppelkondensatoren gegen Erde

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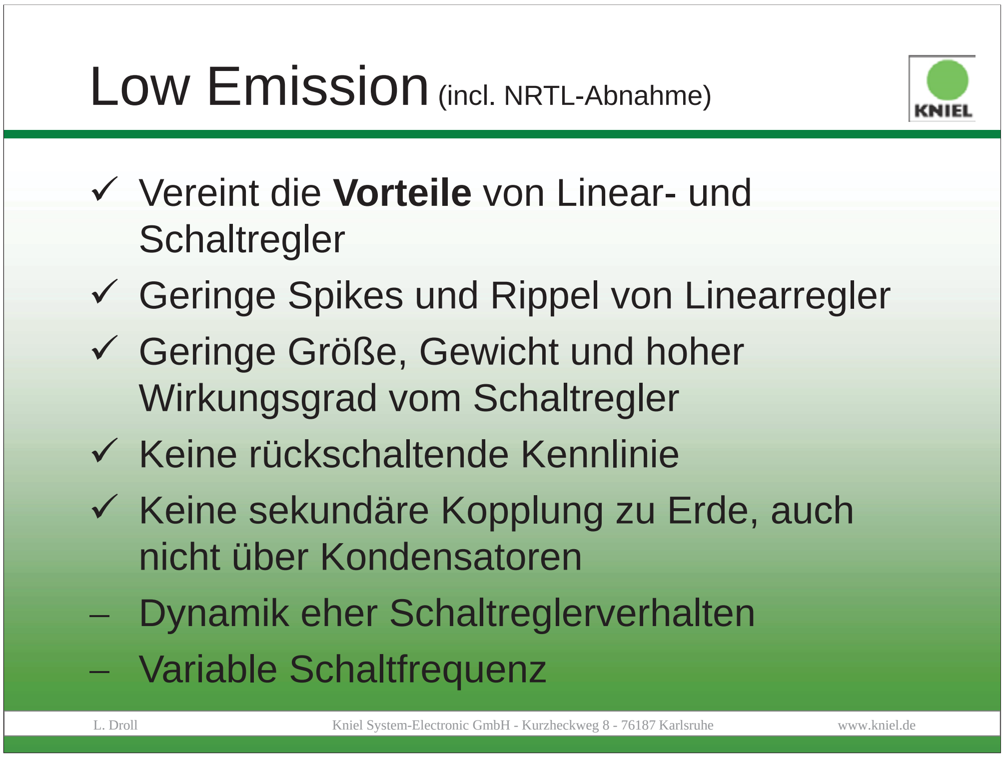

Low Emission (incl. NRTL-Abnahme)

- ✓ Vereint die **Vorteile** von Linear- und Schaltregler
- ✓ Geringe Spikes und Rippel von Linearregler
- ✓ Geringe Größe, Gewicht und hoher Wirkungsgrad vom Schaltregler
- ✓ Keine rückschaltende Kennlinie
- ✓ Keine sekundäre Kopplung zu Erde, auch nicht über Kondensatoren
- – Dynamik eher Schaltreglerverhalten
- – Variable Schaltfrequenz

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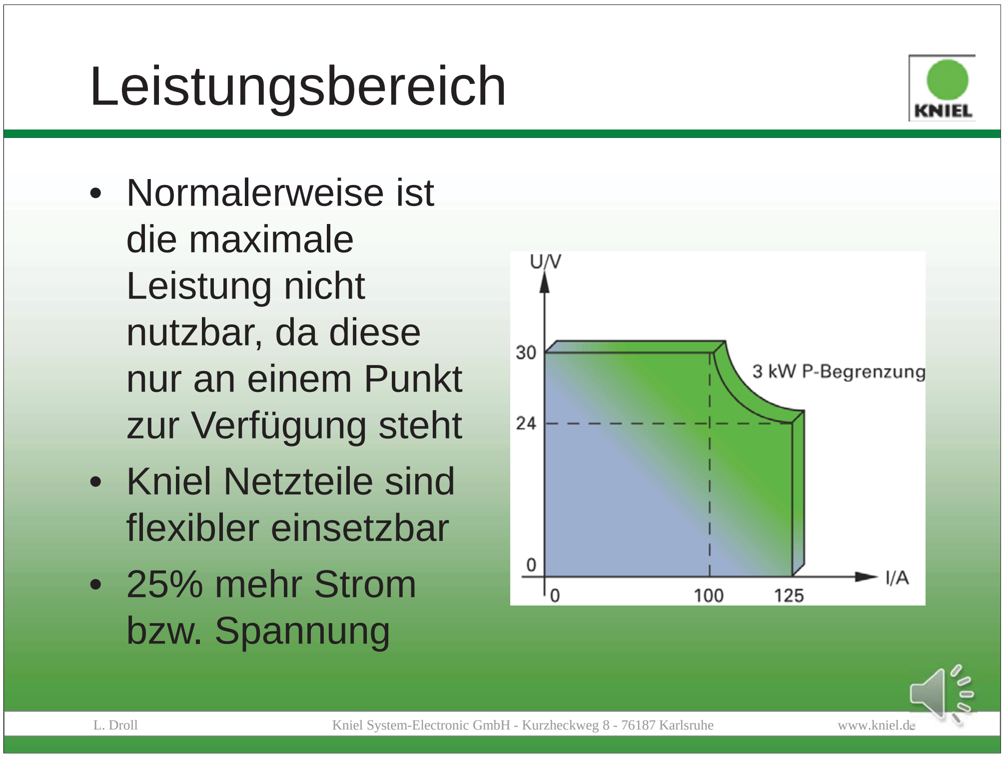
Netzüberwachung und mehr

- Netzmonitor für U & I …
- Modular aufgebaut
- Frei konfigurierbar
- Emailversand bei Ereignissen
- Web- & FTP-Server für direkten Zugriff
- Integrierte USV
- Integrierter Datenspeicher zur Aufzeichnung von Jahren
- Selectiver Passwortschutz
- …

ENERGY Serien

- Digitale Netzteile (fest, einstellbar, analog, digital)
- 400/(800)/1200/1500/3000W über einen Bereich.



Leistungsbereich

- Normalerweise ist die maximale Leistung nicht nutzbar, da diese nur an einem Punkt zur Verfügung steht
- Kniel Netzteile sind flexibler einsetzbar
- 25% mehr Strom bzw. Spannung

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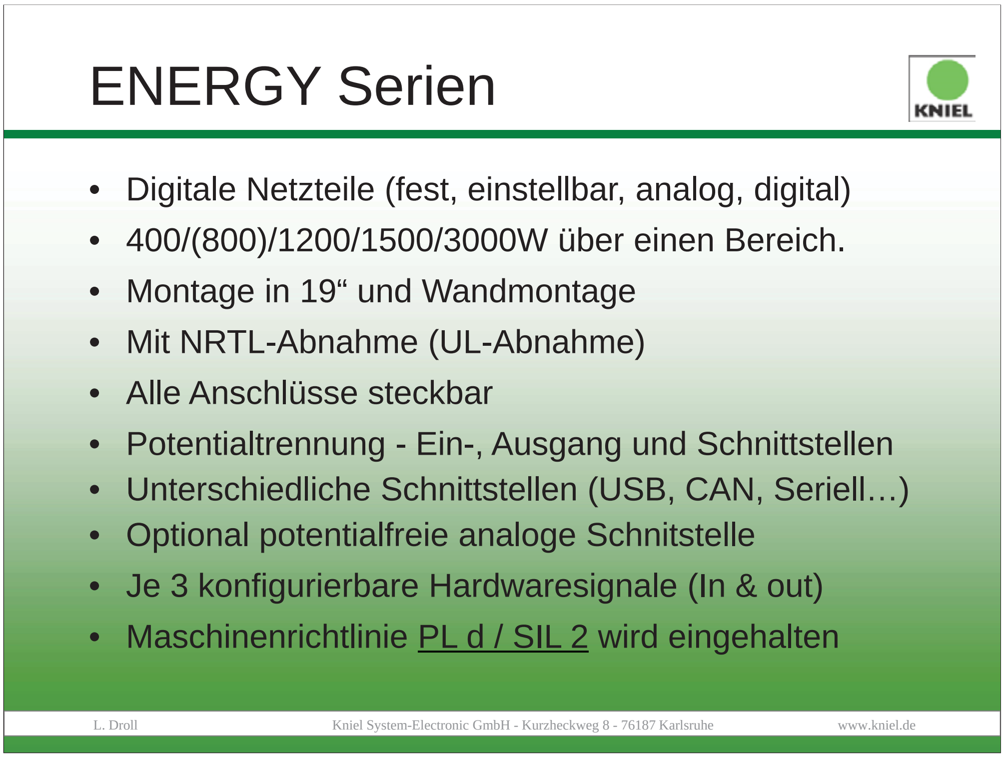

ENERGY Serien

- Digitale Netzteile (fest, einstellbar, analog, digital)
- 400/(800)/1200/1500/3000W über einen Bereich.
- Montage in 19“ und Wandmontage
- Mit NRTL-Abnahme (UL-Abnahme)
- Alle Anschlüsse steckbar
- Potentialtrennung - Ein-, Ausgang und Schnittstellen
- Unterschiedliche Schnittstellen (USB, CAN, Seriell…)
- Optional potentialfreie analoge Schnitstelle
- Je 3 konfigurierbare Hardwaresignale (In & out)
- Maschinenrichtlinie PL d / SIL 2 wird eingehalten

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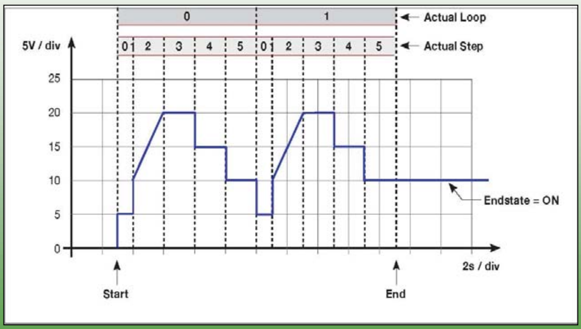
ENERGY Software

- Alle Baureihen mit absolut identischer Firmware
- Integrierte „Intelligenz“
- Alle Soll- und Istwerte als Echtwerte
- Gerätekontrolle bei Netzteilaustausch
- Spannungs-, Strom- und Leistungsregelung
- Einstellbare Rampen, Limits und Thresholds
- Einstellbare positive und negative Innenwiderstände
- Einstellbare E-Last
- CAN-Bus in normierter Form (CiA 453)
- 50 Parametersätze speicherbar
- Eigenständige Sequenzabarbeitung (2 Stück)

Sequenzen

- Step & Rampen
- Digtale I/O
- Entlastung des Datenbusses
- Bis zu 100 Steps je Loop
- Ab 1 msec
- 1 bis 254 Loops, oder unendlich
- Konfigurierbarer Endstatus
- Zugriff auf alle gespeicherten Parametersätze
- Testmodus



Kniel macht den Unterschied

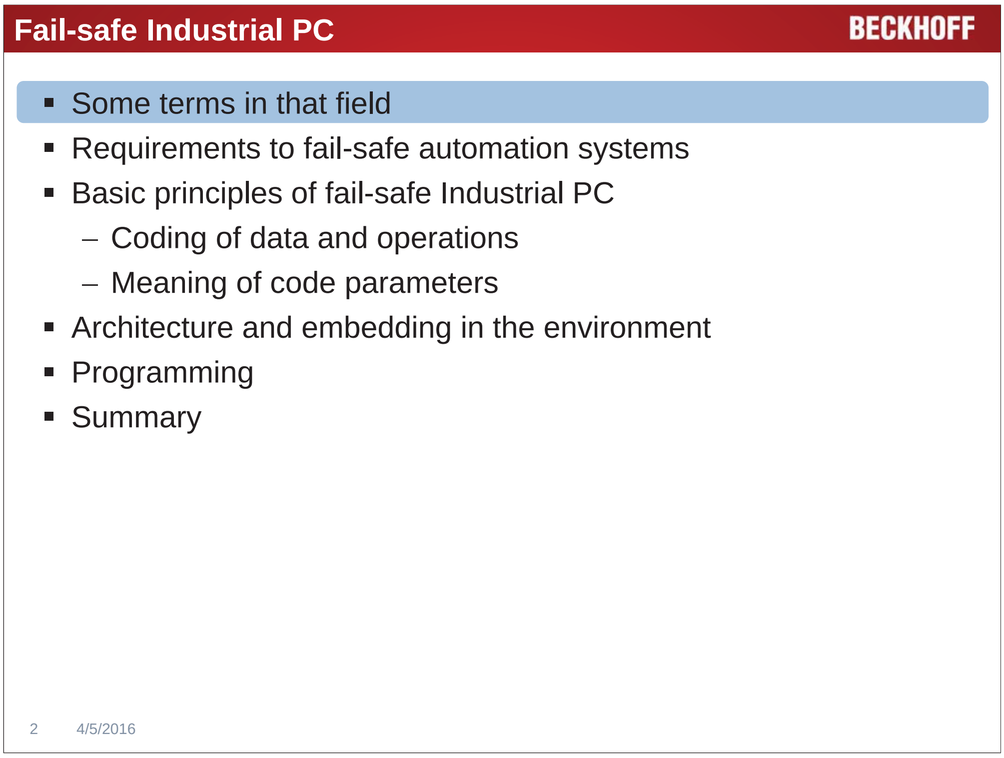
Stromversorgungen

für die empfindliche Messtechnik
und die komplexe Automatisierung

BECKHOFF

Fail-safe Industrial PC

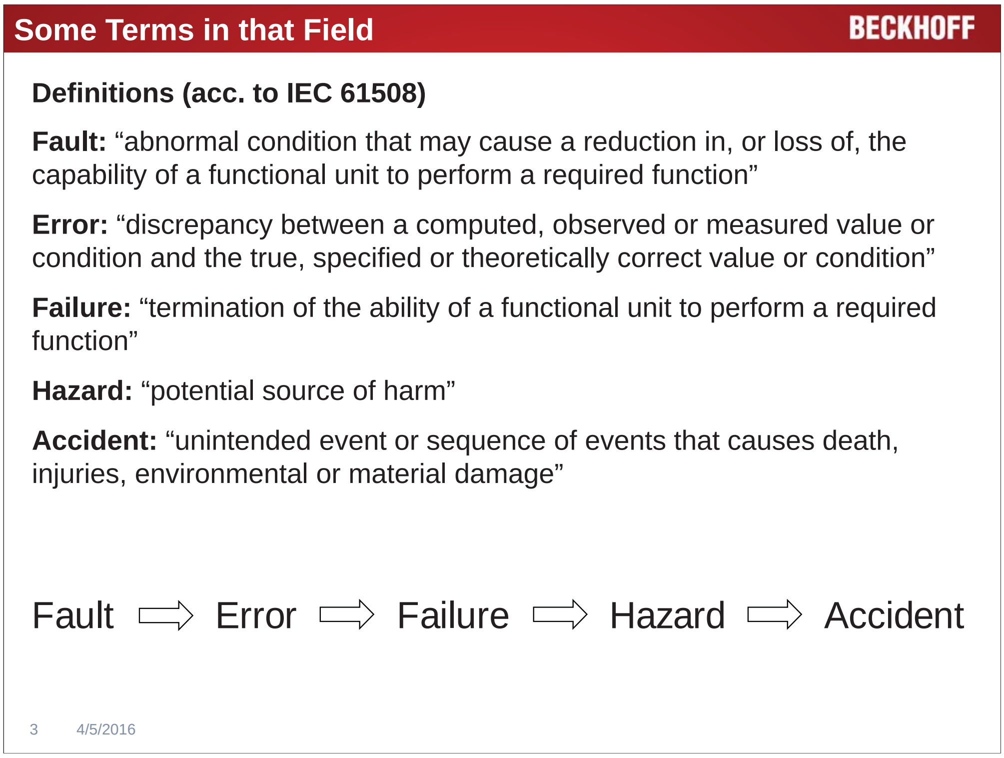
Prof. Frank Schiller, Dr. Martin Früchtl
Scientific Safety & Security
Beckhoff Automation GmbH & Co. KG
F.Schiller@beckhoff.com



Fail-safe Industrial PC

BECKHOFF

- Some terms in that field
- Requirements to fail-safe automation systems
- Basic principles of fail-safe Industrial PC
  - Coding of data and operations
  - Meaning of code parameters
- Architecture and embedding in the environment
- Programming
- Summary



Some Terms in that Field

BECKHOFF

Definitions (acc. to IEC 61508)

Fault: “abnormal condition that may cause a reduction in, or loss of, the capability of a functional unit to perform a required function”

Error: “discrepancy between a computed, observed or measured value or condition and the true, specified or theoretically correct value or condition”

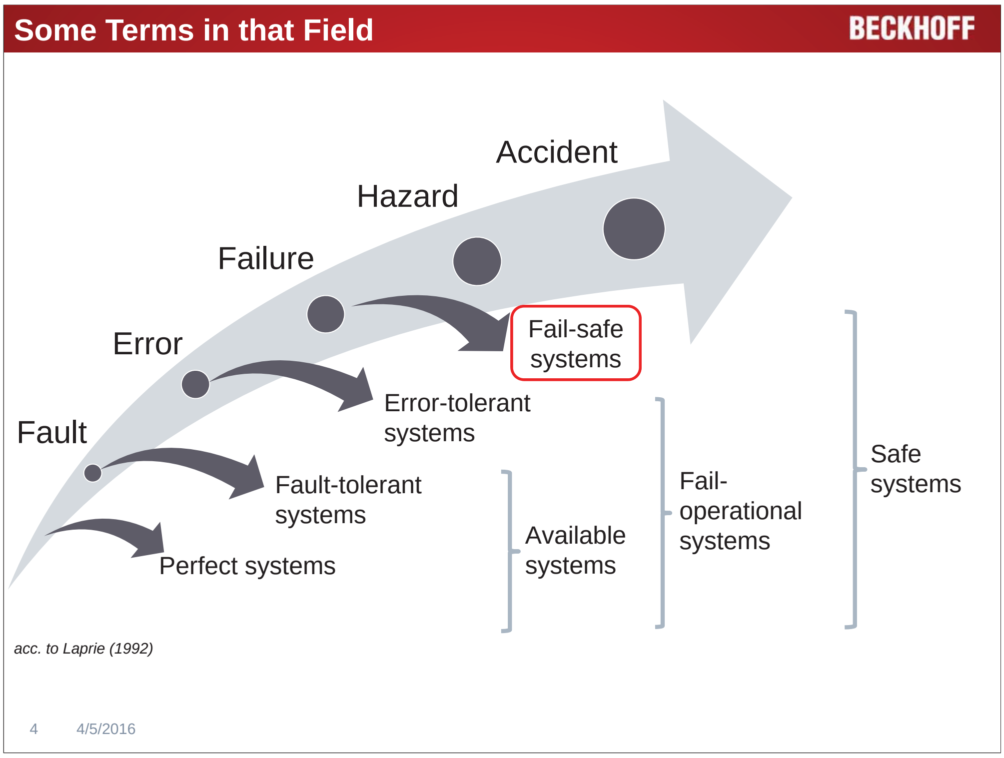
Failure: “termination of the ability of a functional unit to perform a required function”

Hazard: “potential source of harm”

Accident: “unintended event or sequence of events that causes death, injuries, environmental or material damage”

Fault ⇨ Error ⇨ Failure ⇨ Hazard ⇨ Accident

3 4/5/2016



Some Terms in that Field

BECKHOFF

Accident

Hazard

Failure

Error

Fault

Fail-safe systems

Error-tolerant systems

Fault-tolerant systems

Perfect systems

Available systems

Fail-operational systems

Safe systems

acc. to Laprie (1992)

4 4/5/2016

Some Terms in that Field

Safety: „Freedom from unacceptable risk of harm.”
(EN 292, IEC ISO guide)

Safety means

- to detect (dangerous) failures and to react safely.

Safety does not necessarily mean

- to avoid failures or
- to compensate failures.

Safety has to be proved.

Some Terms in that Field

Safety Integrity Level (IEC 61508)	Probability of dangerous failure per hour	Probability of dangerous failure per year
SIL 1	$<10^{-5}$	$<10^{-1}$
SIL 2	$<10^{-6}$	$<10^{-2}$
SIL 3	$<10^{-7}$	$<10^{-3}$
SIL 4	$<10^{-8}$	$<10^{-4}$

Automation

Public
Transport

Fail-safe Industrial PC

- Some terms in that field
- Requirements to fail-safe automation systems
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Requirements to Fail-safe Automation Systems

- **Current State**
  - Specific safety controllers
  - Performance of IPC could not be used in safety applications
  - Programming of safety controllers mainly by means of function blocks
- **Goals**
  - Hardware independent safety realized in software
  - Increase of flexibility of applications by enabling safety applications based on a subset of C

Requirements to Fail-safe Automation Systems

BECKHOFF

- Error detection with high probability
- Fast initiation of the safe reaction of the plant
- Provability
- Usability, operability
- Profitability (use of Commercial-off-the-Shelf (COTS), e.g. Industrial PC)

Fail-safe Industrial PC

BECKHOFF

- Some terms in that field
- Requirements to fail-safe automation systems
- Basic principles of fail-safe Industrial PC
  - Coding of data and operations
  - Meaning of code parameters
- Architecture and embedding in the environment
- Programming
- Summary

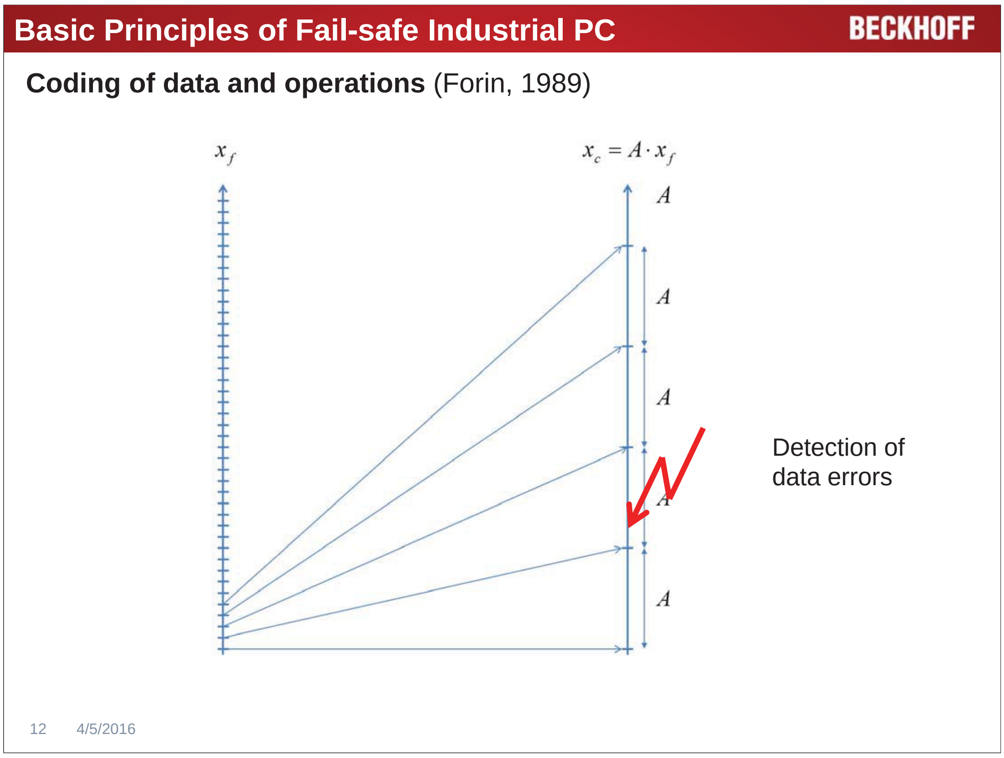
Basic Principles of Fail-safe Industrial PC

BECKHOFF

Coding of data and operations (Forin, 1989)

Original date: x_f

Coded date: $x_c = A \cdot x_f$

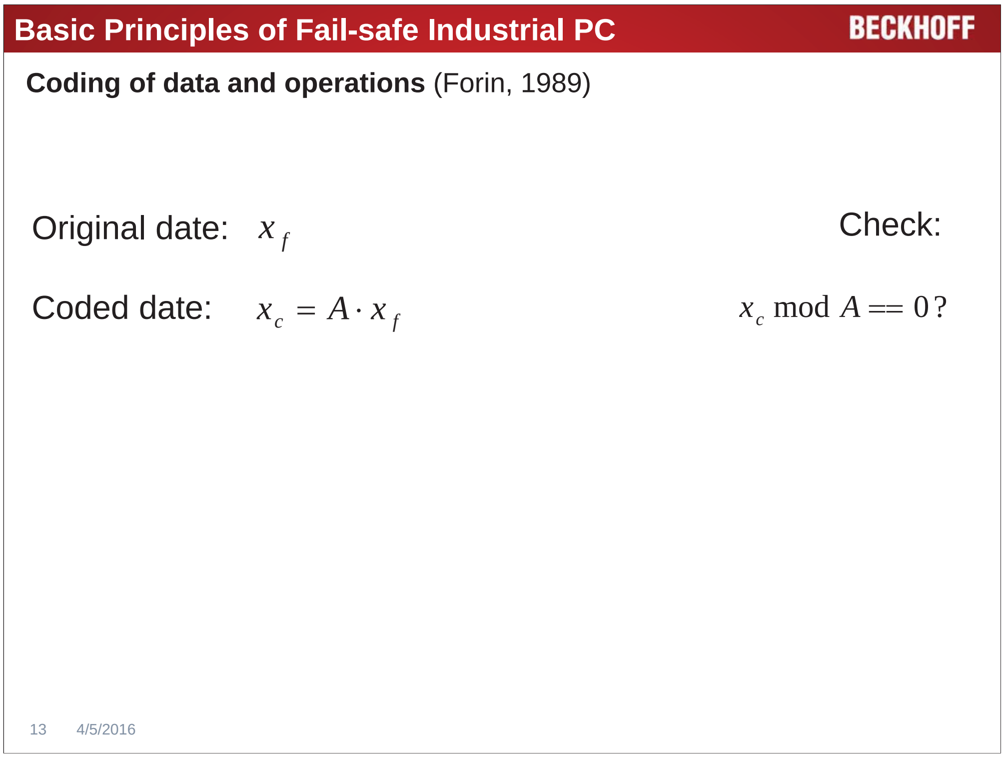


Basic Principles of Fail-safe Industrial PC

BECKHOFF

Coding of data and operations (Forin, 1989)

Detection of data errors



Basic Principles of Fail-safe Industrial PC

BECKHOFF

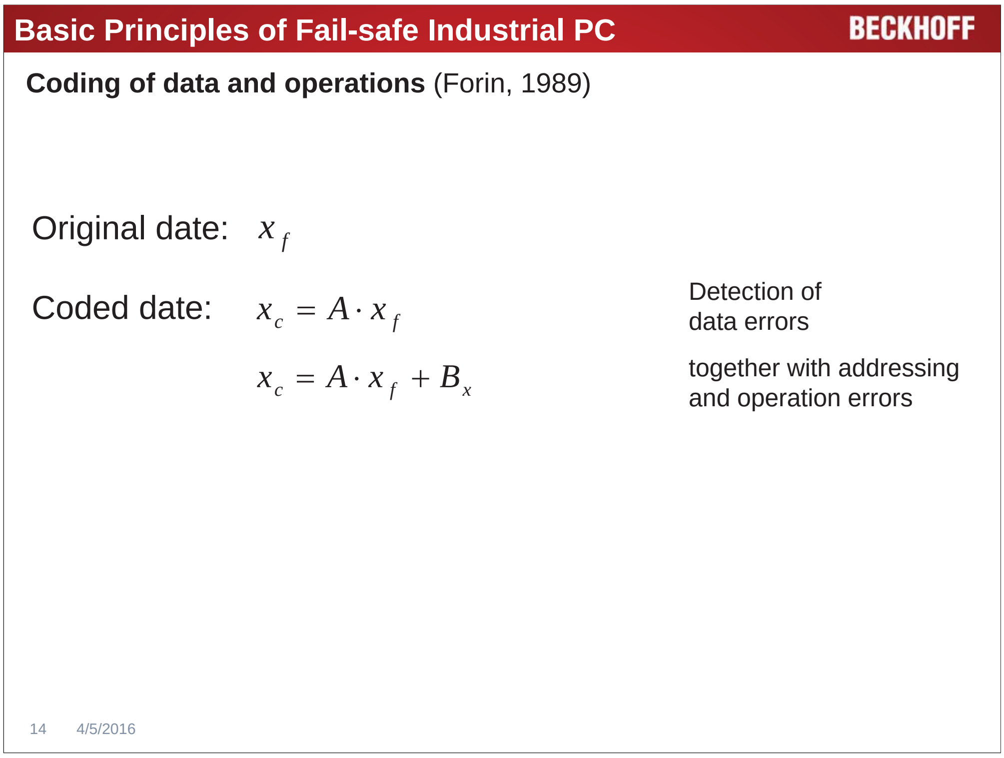
Coding of data and operations (Forin, 1989)

Original date: x_f

Coded date: $x_c = A \cdot x_f$

Check:

$x_c \bmod A == 0\,?$



Basic Principles of Fail-safe Industrial PC

BECKHOFF

Coding of data and operations (Forin, 1989)

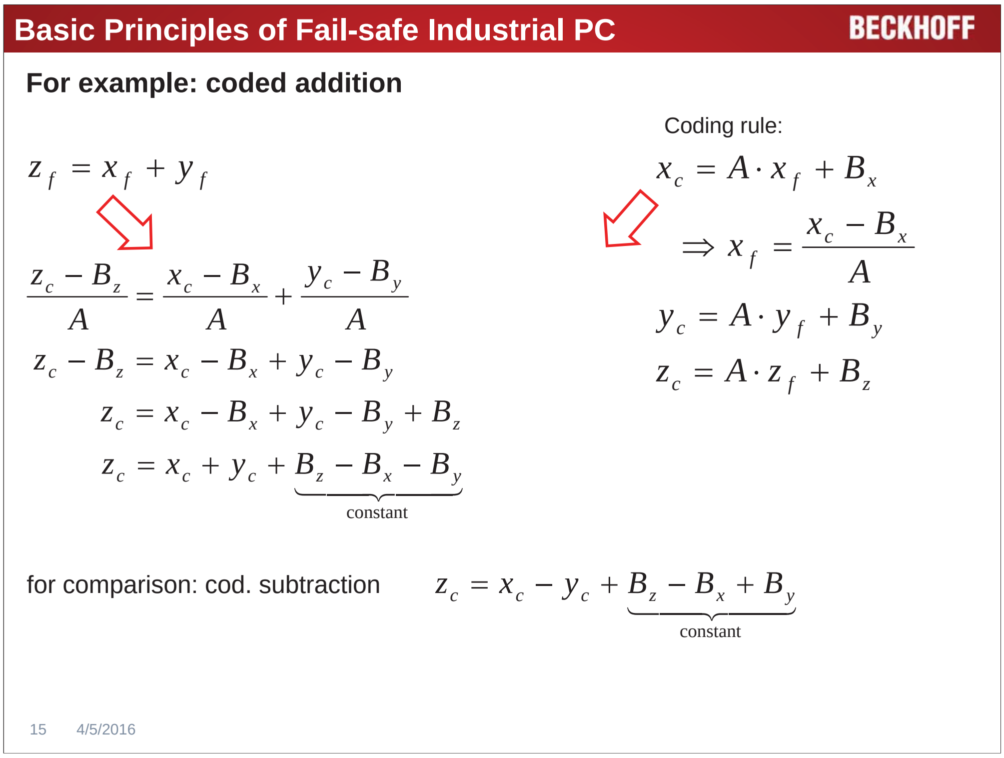
Original date: x_f

Coded date: $x_c = A \cdot x_f$

Detection of data errors

$x_c = A \cdot x_f + B_x$

together with addressing and operation errors



Basic Principles of Fail-safe Industrial PC

BECKHOFF

For example: coded addition

$$z_f = x_f + y_f$$

Coding rule:

$$x_c = A \cdot x_f + B_x$$

$$\Rightarrow x_f = \frac{x_c - B_x}{A}$$

$$y_c = A \cdot y_f + B_y$$

$$z_c = A \cdot z_f + B_z$$

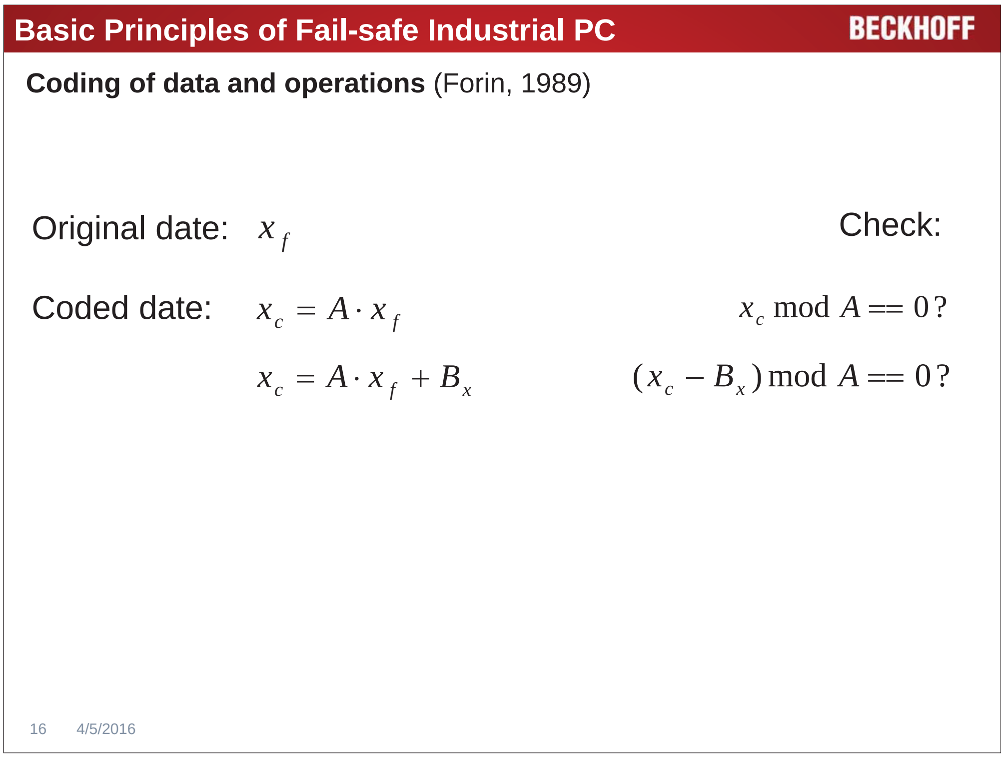
$$\frac{z_c - B_z}{A} = \frac{x_c - B_x}{A} + \frac{y_c - B_y}{A}$$

$$z_c - B_z = x_c - B_x + y_c - B_y$$

$$z_c = x_c - B_x + y_c - B_y + B_z$$

$$z_c = x_c + y_c + \underbrace{B_z - B_x - B_y}_{\text{constant}}$$

for comparison: cod. subtraction $z_c = x_c - y_c + \underbrace{B_z - B_x + B_y}_{\text{constant}}$



Basic Principles of Fail-safe Industrial PC

BECKHOFF

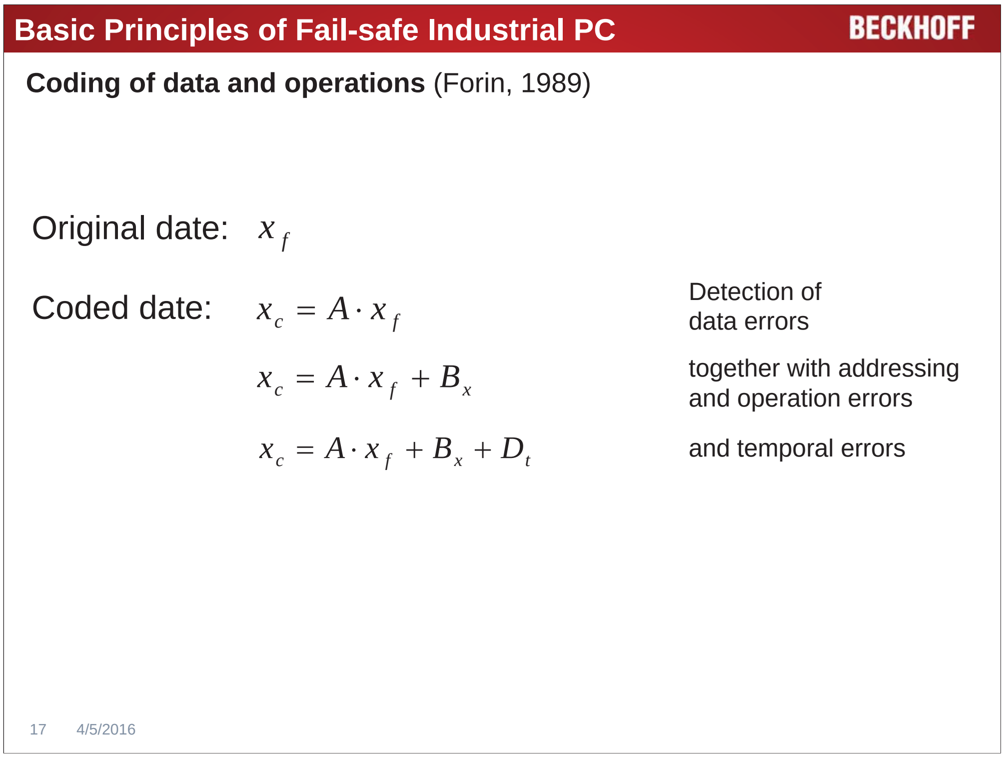
Coding of data and operations (Forin, 1989)

Original date: x_f

Check:

Coded date: $x_c = A \cdot x_f$ — $x_c \bmod A == 0\,?$

$x_c = A \cdot x_f + B_x$ — $(x_c - B_x) \bmod A == 0\,?$



Basic Principles of Fail-safe Industrial PC

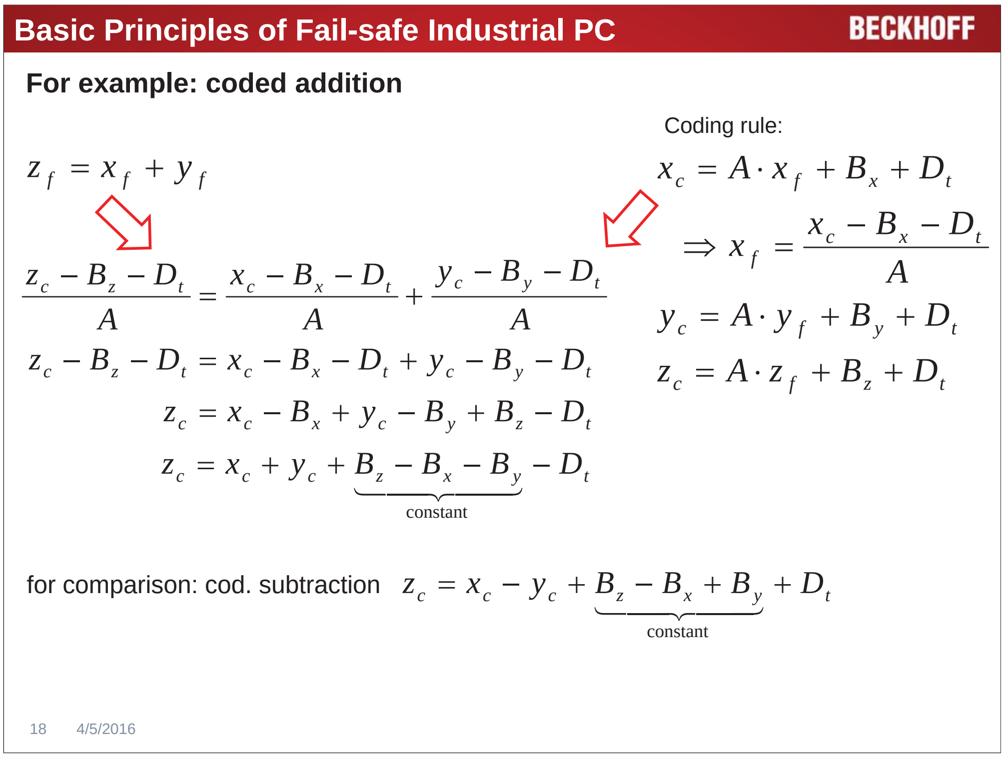
BECKHOFF

Coding of data and operations (Forin, 1989)

Original date: x_f

Coded date:

$x_c = A \cdot x_f$	Detection of data errors
$x_c = A \cdot x_f + B_x$	together with addressing and operation errors
$x_c = A \cdot x_f + B_x + D_t$	and temporal errors



Basic Principles of Fail-safe Industrial PC

BECKHOFF

For example: coded addition

$$z_f = x_f + y_f$$

$$\frac{z_c - B_z - D_t}{A} = \frac{x_c - B_x - D_t}{A} + \frac{y_c - B_y - D_t}{A}$$

$$z_c - B_z - D_t = x_c - B_x - D_t + y_c - B_y - D_t$$

$$z_c = x_c - B_x + y_c - B_y + B_z - D_t$$

$$z_c = x_c + y_c + \underbrace{B_z - B_x - B_y}_{\text{constant}} - D_t$$

Coding rule:

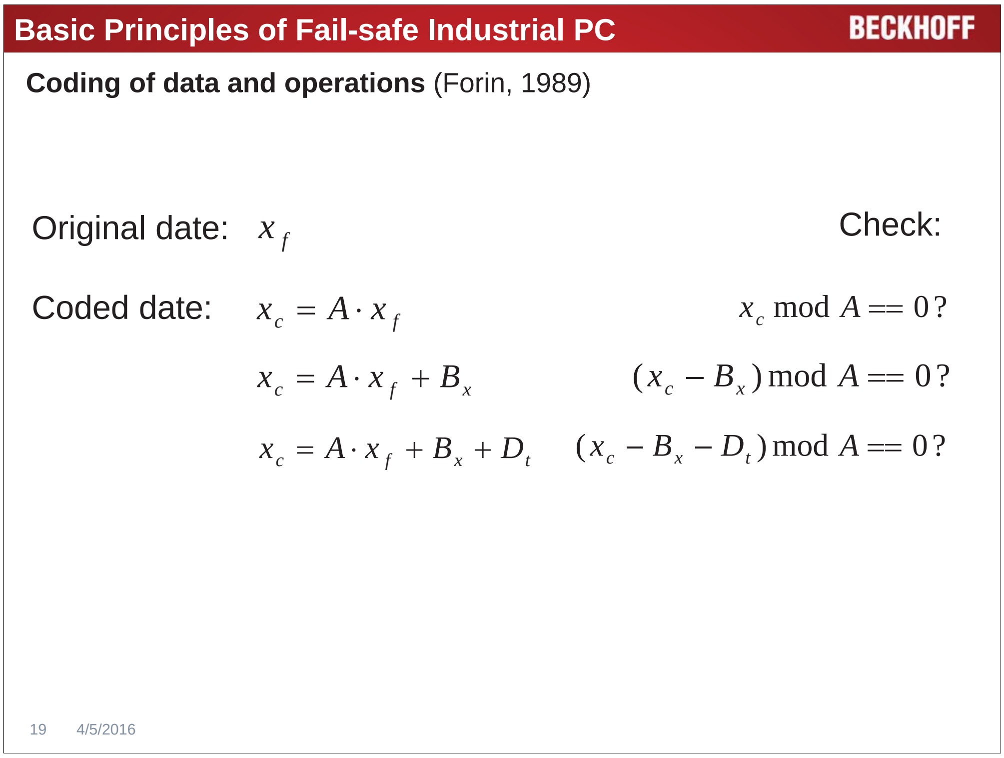
$$x_c = A \cdot x_f + B_x + D_t$$

$$\Rightarrow x_f = \frac{x_c - B_x - D_t}{A}$$

$$y_c = A \cdot y_f + B_y + D_t$$

$$z_c = A \cdot z_f + B_z + D_t$$

for comparison: cod. subtraction $z_c = x_c - y_c + \underbrace{B_z - B_x + B_y}_{\text{constant}} + D_t$



Basic Principles of Fail-safe Industrial PC

BECKHOFF

Coding of data and operations (Forin, 1989)

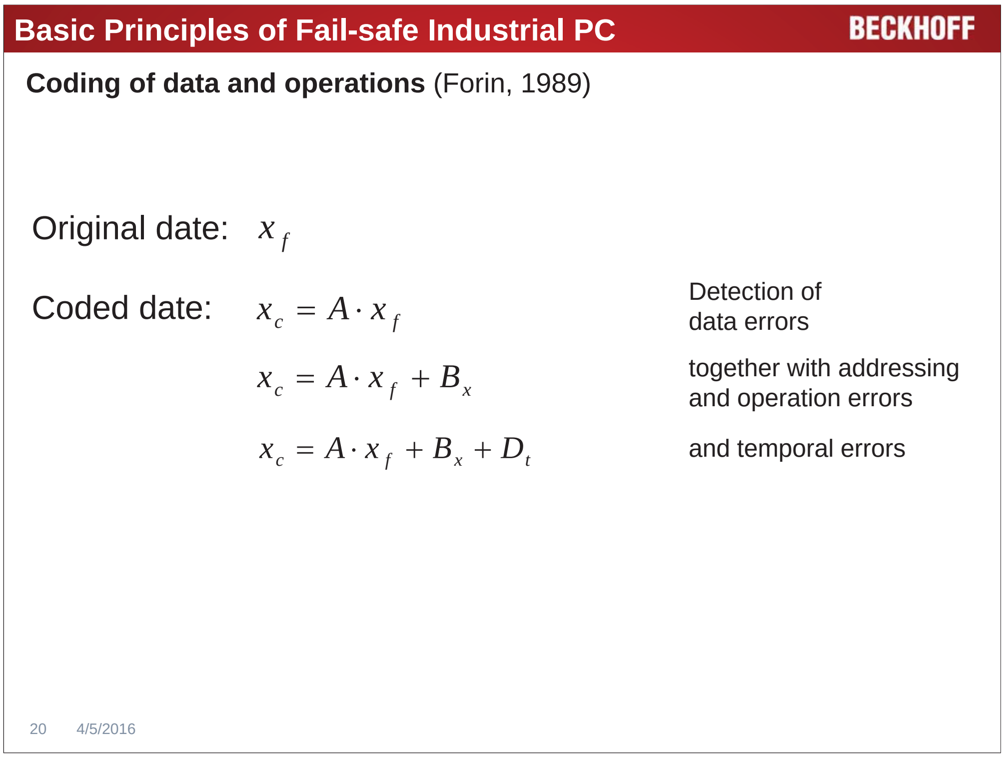
Original date: x_f

Check:

Coded date: $x_c = A \cdot x_f$ — $x_c \bmod A == 0\,?$

$x_c = A \cdot x_f + B_x$ — $(x_c - B_x) \bmod A == 0\,?$

$x_c = A \cdot x_f + B_x + D_t$ — $(x_c - B_x - D_t) \bmod A == 0\,?$



Basic Principles of Fail-safe Industrial PC

BECKHOFF

Coding of data and operations (Forin, 1989)

Original date: x_f

Coded date: $x_c = A \cdot x_f$ — Detection of data errors

$x_c = A \cdot x_f + B_x$ — together with addressing and operation errors

$x_c = A \cdot x_f + B_x + D_t$ — and temporal errors

Basic Principles of Fail-safe Industrial PC

BECKHOFF

Meaning of code parameters w.r.t. data and operations

$$x_c = A \cdot x_f + B_x + D_t \qquad (x_c - B_x - D_t) \bmod A == 0\,?$$

$A:$ Prime number: A sequence of i erroneous operations with constant Offset f causes the final Offset $i{\cdot}f$. This Offset is only divisible by A, if i or f are divisible by A. If A is not a prime number, factors of i and f could also cause multiples of A. The same holds for multiplication.

Furthermore, A provides deterministic criteria like the *Hamming distance* and the *arithmetic distance*.

$B_x: \quad B_x < A$

$D_t: \quad D_t < A$

reason: since $(x_c - B_x - D_t) \bmod A == 0\,?$

$$(x_c - \underbrace{B_x \bmod A}_{<A} - \underbrace{D_t \bmod A}_{<A}) \bmod A == 0\,?$$

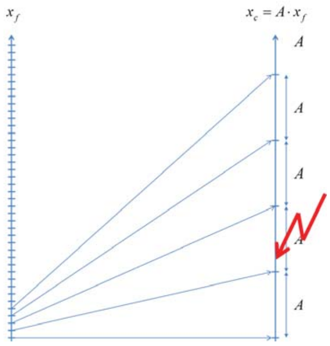
holds, the effective signatures are: $(B_x \bmod A), (D_t \bmod A)$

Basic Principles of Fail-safe Industrial PC

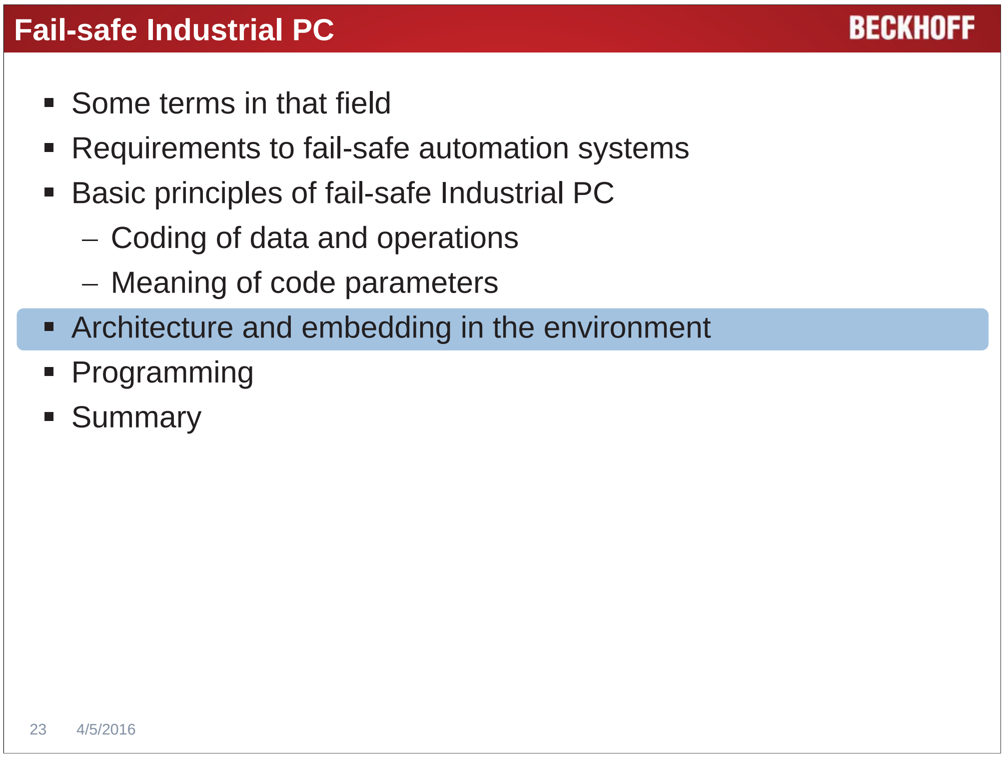
BECKHOFF

Meaning of code parameters w.r.t. data and operations

Residual error probability:



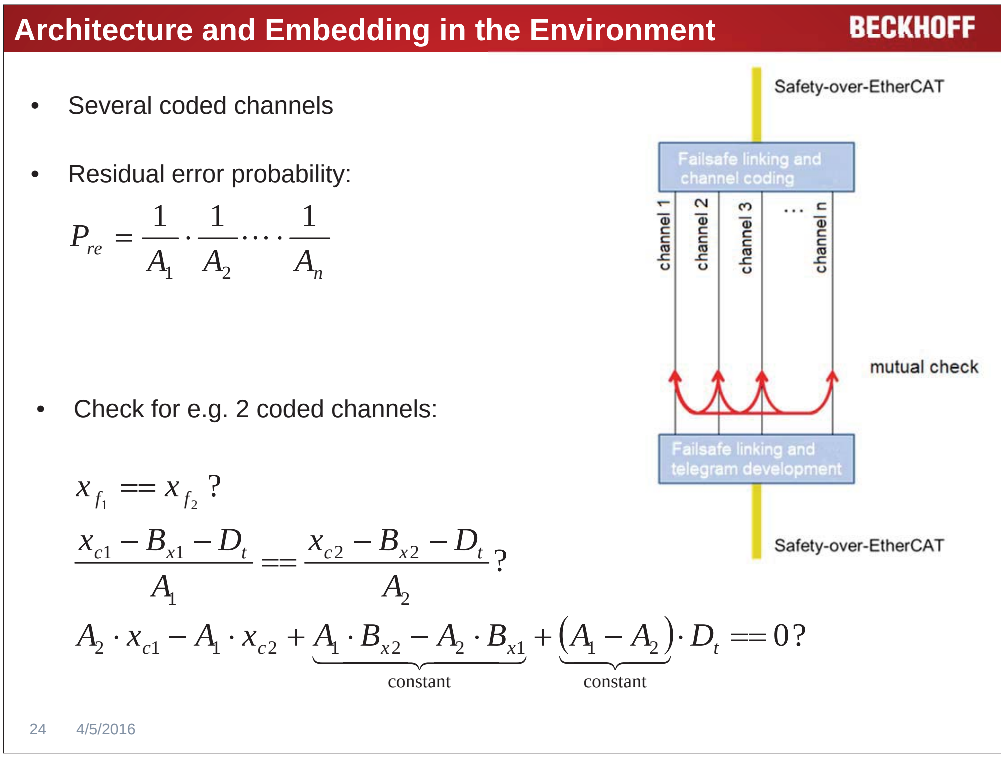
$$P_{re} = \frac{\text{Number of all erroneous values divisible by } A}{\text{Number of all possible values}} = \frac{\frac{\| x_c \|}{A} - 1}{\| x_c \|} < \frac{1}{A}$$



Fail-safe Industrial PC

BECKHOFF

- Some terms in that field
- Requirements to fail-safe automation systems
- Basic principles of fail-safe Industrial PC
  - Coding of data and operations
  - Meaning of code parameters
- Architecture and embedding in the environment
- Programming
- Summary



Architecture and Embedding in the Environment

BECKHOFF

- Several coded channels
- Residual error probability:

$$P_{re} = \frac{1}{A_1} \cdot \frac{1}{A_2} \cdot \ldots \cdot \frac{1}{A_n}$$

- Check for e.g. 2 coded channels:

$$x_{f_1} == x_{f_2} \; ?$$

$$\frac{x_{c1} - B_{x1} - D_t}{A_1} == \frac{x_{c2} - B_{x2} - D_t}{A_2} \; ?$$

$$A_2 \cdot x_{c1} - A_1 \cdot x_{c2} + \underbrace{A_1 \cdot B_{x2} - A_2 \cdot B_{x1}}_{\text{constant}} + \underbrace{(A_1 - A_2)}_{\text{constant}} \cdot D_t == 0?$$

Fail-safe Industrial PC

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- Some terms in that field
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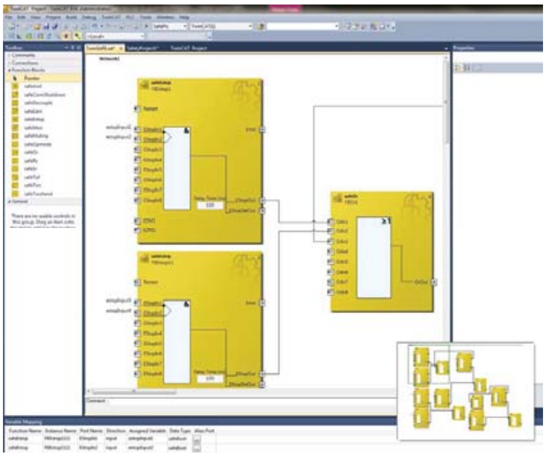
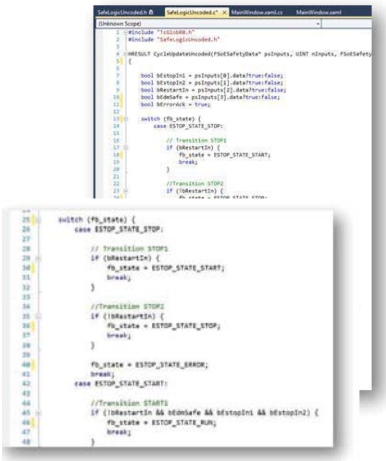
Programming

BECKHOFF

1. Graphical Editor (in TwinCAT, as in existing safety solutions)
2. Safety C (limited C instruction set)





```
#include "TcGlobRB.h"
#include "SafeLogicUncoded.h"

HRESULT CycleUpdateUncoded(FSoESafetyData* psInputs, UINT nInputs, FSoESafety
{

    bool bEstopIn1 = psInputs[0].data?true:false;
    bool bEstopIn2 = psInputs[1].data?true:false;
    bool bRestartIn = psInputs[2].data?true:false;
    bool bEdmSafe = psInputs[3].data?true:false;
    bool bErrorAck = true;

    switch (fb_state) {
        case ESTOP_STATE_STOP:

            // Transition STOP1
            if (bRestartIn) {
                fb_state = ESTOP_STATE_START;
                break;
            }

            //Transition STOP2
            if (!bRestartIn) {
```

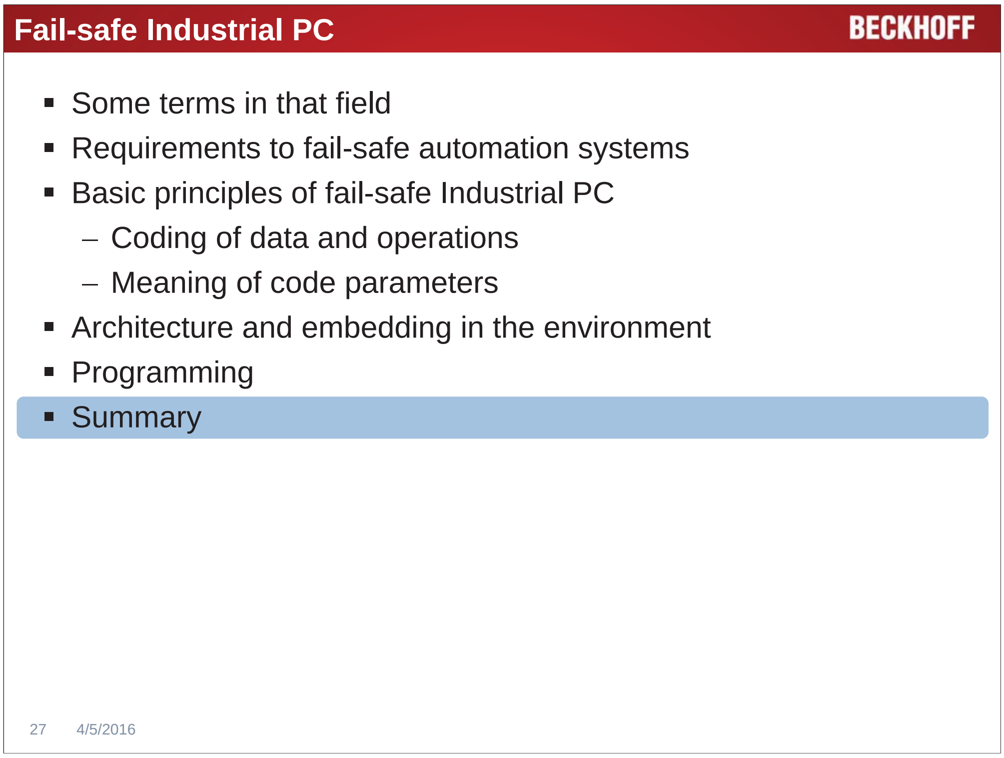
```
    switch (fb_state) {
        case ESTOP_STATE_STOP:

            // Transition STOP1
            if (bRestartIn) {
                fb_state = ESTOP_STATE_START;
                break;
            }

            //Transition STOP2
            if (!bRestartIn) {
                fb_state = ESTOP_STATE_STOP;
                break;
            }

            fb_state = ESTOP_STATE_ERROR;
            break;
        case ESTOP_STATE_START:

            //Transition START1
            if (!bRestartIn && bEdmSafe && bEstopIn1 && bEstopIn2) {
                fb_state = ESTOP_STATE_RUN;
                break;
            }
```



Fail-safe Industrial PC

BECKHOFF

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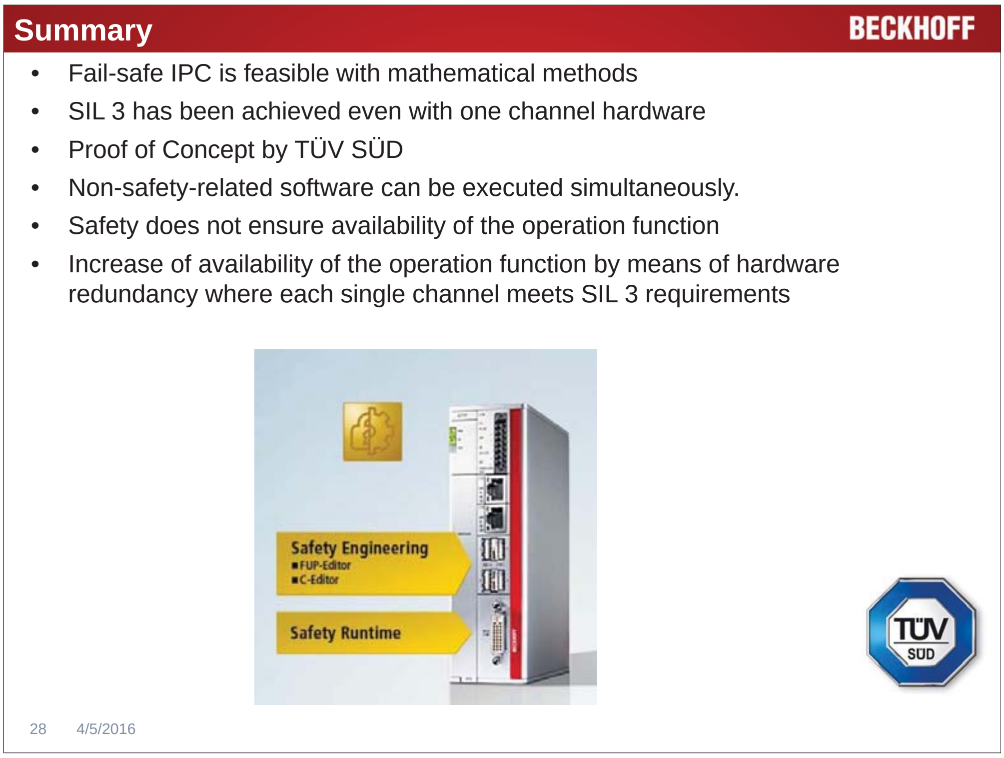

Summary

BECKHOFF

- Fail-safe IPC is feasible with mathematical methods
- SIL 3 has been achieved even with one channel hardware
- Proof of Concept by TÜV SÜD
- Non-safety-related software can be executed simultaneously.
- Safety does not ensure availability of the operation function
- Increase of availability of the operation function by means of hardware redundancy where each single channel meets SIL 3 requirements

Contact

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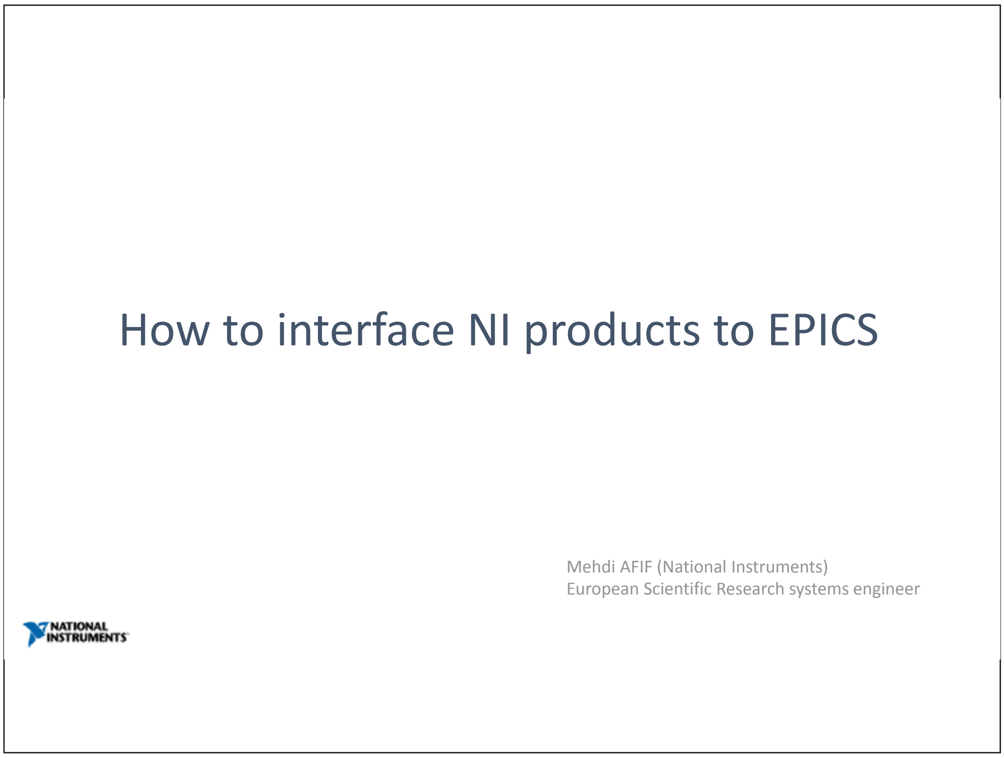
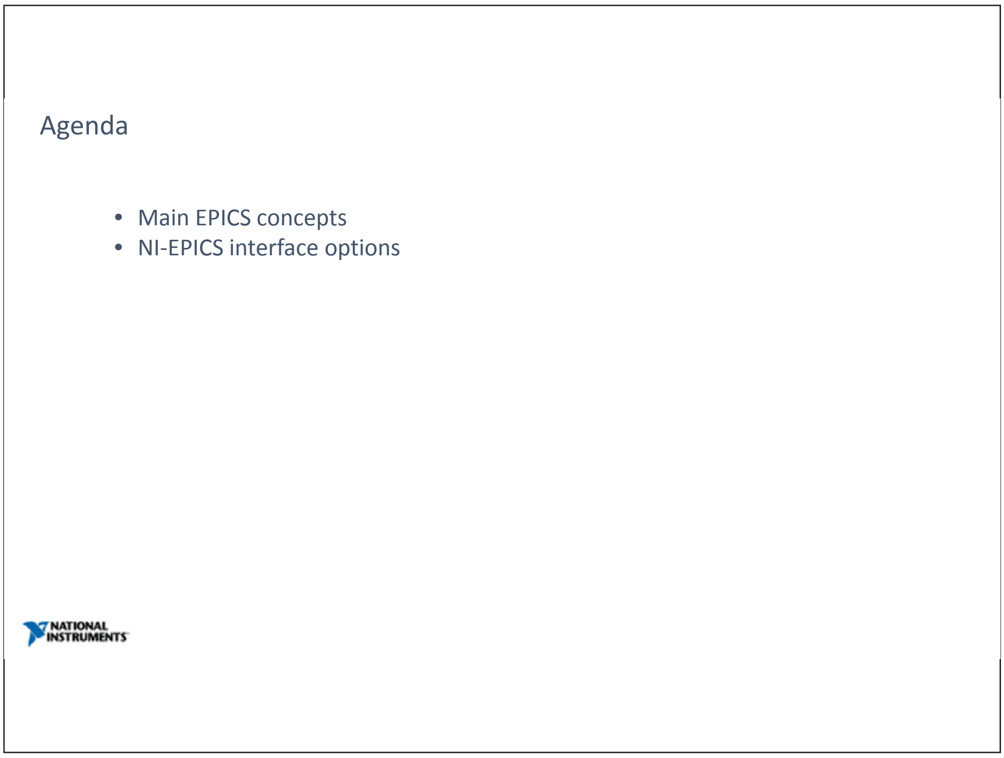


How to interface NI products to EPICS

Mehdi AFIF (National Instruments)
European Scientific Research systems engineer

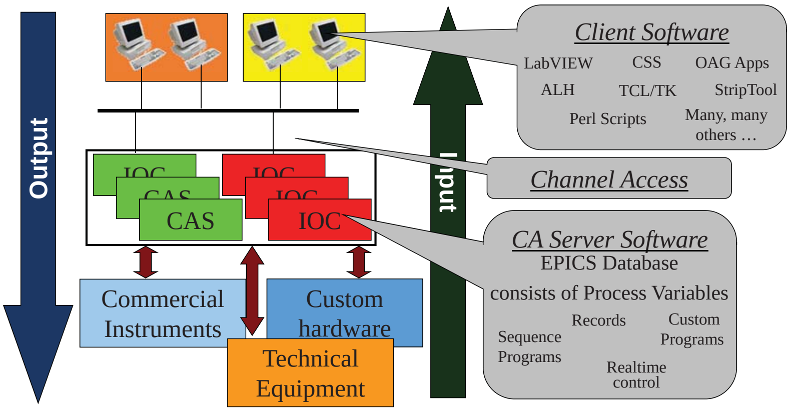


Agenda

- Main EPICS concepts
- NI-EPICS interface options

EPICS architecture

Network based Client/Server control system architecture
Servers provide information and service/ Clients request information or use services



Output

IOC
CAS
CAS

IOC
IOC
IOC

Commercial Instruments

Custom hardware

Technical Equipment

Input

Client Software

LabVIEW CSS OAG Apps
ALH TCL/TK StripTool
Perl Scripts Many, many others …

Channel Access

CA Server Software

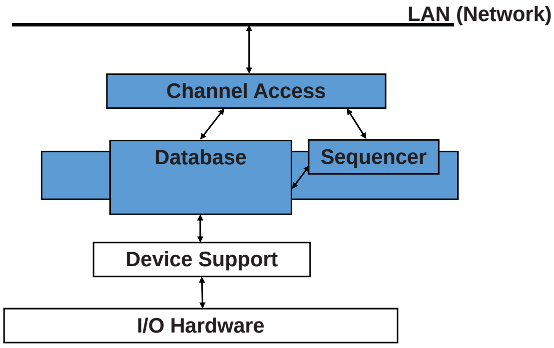
EPICS Database consists of Process Variables

Records
Custom Programs
Sequence Programs
Realtime control

From PSI Epics Course

Inside an IOC

The major software components of an IOC



LAN (Network)

Channel Access

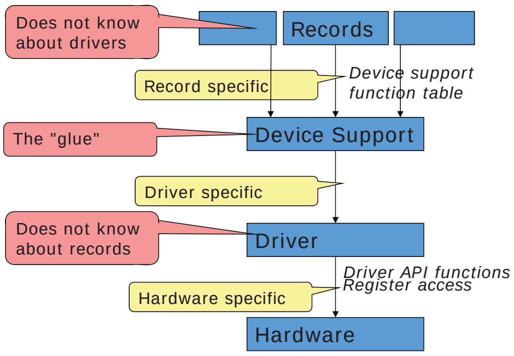
Database

Sequencer

Device Support

I/O Hardware

Device support and records



Does not know about drivers

Records

Record specific

Device support function table

The "glue"

Device Support

Driver specific

Does not know about records

Driver

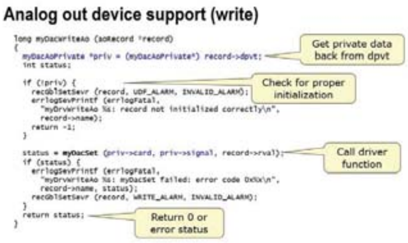
Driver API functions

Register access

Hardware specific

Hardware

```
record (ai, “TEST:CURRENT”) {
        field (EGU, "mV")
        field (LOW, “10”)
        field (HIGH, “300”)
        field (HOPR, "370")
        field (LOPR, "0")
        field (DESC, “Feedback voltage”)
        field (SCAN, “1 Second”)
        field (DTYP, “NI 6268 ")
        field (INP, "#C0 S0)
}
```

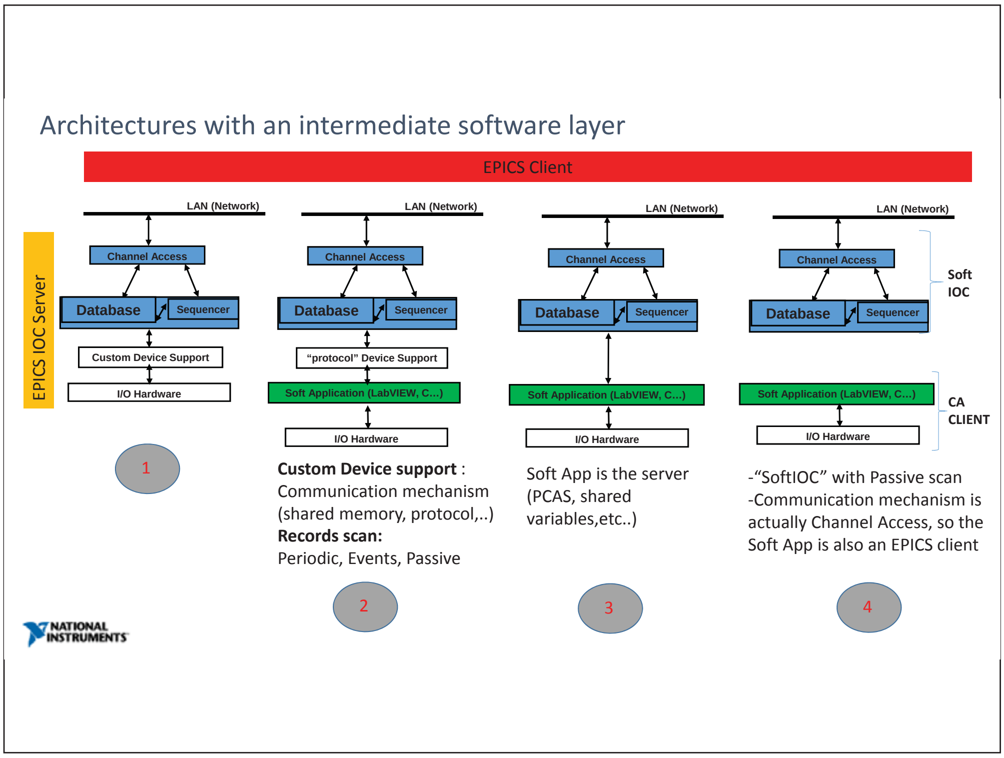


Analog out device support (write)

```
long myDacWriteAo (aoRecord *record)
{
  myDacAoPrivate *priv = (myDacAoPrivate*) record->dpvt;
  int status;

  if (!priv) {
    recGblSetSevr (record, UDF_ALARM, INVALID_ALARM);
    errlogSevPrintf (errlogFatal,
      "myDrvWriteAo %s: record not initialized correctly\n",
      record->name);
    return -1;
  }

  status = myDacSet (priv->card, priv->signal, record->rval);
  if (status) {
    errlogSevPrintf (errlogFatal,
      "myDrvWriteAo %s: myDacSet failed: error code 0x%x\n",
      record->name, status);
    recGblSetSevr (record, WRITE_ALARM, INVALID_ALARM);
  }
  return status;
}
```

Records processing

- Record processing can be periodic or event driven or passive
- **Periodic**:
  - Standard scan rates: 10, 5, 2, 1, 0.5, 0.2 and 0.1 seconds
  - Custom scan rates can be configured up to speeds allowed by operating system and hardware
- **Event driven**:
  - Hardware interrupts
  - EPICS Events (post_event)
- **Passive**:
  - Channel Access Puts (caput)
  - Request from another record via links



Architectures with an intermediate software layer

Custom Device support :
Communication mechanism (shared memory, protocol,..)
Records scan:
Periodic, Events, Passive

Soft App is the server (PCAS, shared variables,etc..)

-"SoftIOC" with Passive scan
-Communication mechanism is actually Channel Access, so the Soft App is also an EPICS client

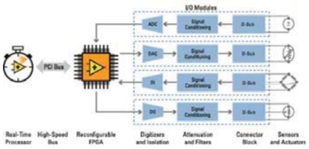
---

EPICS-NI interface

NI Platforms

NI CompactRIO

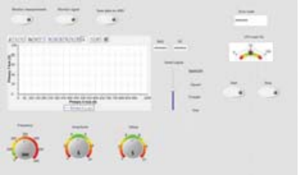
- Rugged form factor with a processor and a reconfigurable FPGA
- Real-Time OS (VxWorks, Linux RT)
- Designed for harsh environments (temperature, shocks, passive cooling, etc..)
- High density hot swappable I/O modules, with built-in conditioning
- **Advanced control, signal processing, modular prototyping, etc…**



PXIe

- PCI/PCIe extended form factor with built-in timing and synchronization
- Windows/Linux/Real-Time embedded/remote controllers
- Until 24GB/s of system throughput, 8GB/s per slot, 3.6 GB/s storage speed
- More than 600 NI instruments (DAQ, digitizers, multimeters, generators, power supplies, switching, RF analyzers and generators, industrial buses…)

Embedded EPICS Base + No software layer

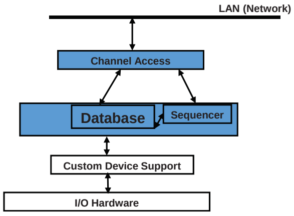


CSS EPICS client

NI Linux RT

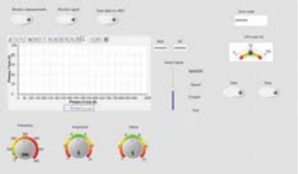
Windows
Linux

Embedded EPICS Base Server
C device support (C drivers)



1

External EPICS Server + “communication mechanism” device support



CSS EPICS client
(remote control
of LV App)

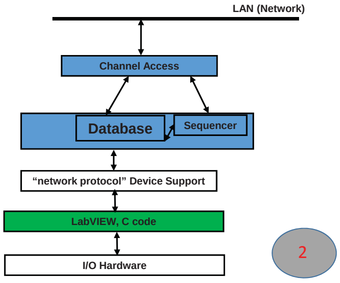
EPICS Server
+ “Network Protocol” device support

VxWorks (LabVIEW
RT), Linux RT

Pharlap (LabVIEW RT),
Windows, Linux

Adapted LabVIEW or C App with a communication
mechanism (TCP/IP, shared memory, etc..)

NATIONAL INSTRUMENTS



LAN (Network)

Channel Access

Database

Sequencer

“network protocol” Device Support

LabVIEW, C code

I/O Hardware

2

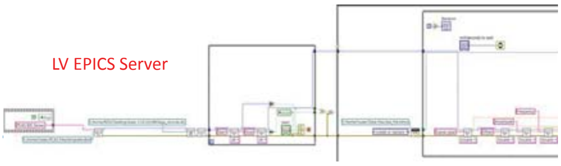
LabVIEW App as a Server

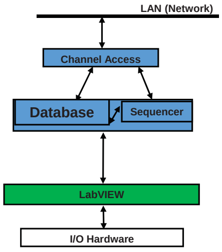
CSS EPICS client (remote
control of LV RT App)

VxWorks (LabVIEW RT),
NI Linux RT

Pharlap (LabVIEW RT),
Windows
Linux

LV EPICS Server





LAN (Network)

Channel Access

Database

Sequencer

LabVIEW

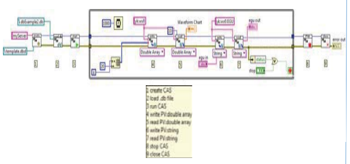
I/O Hardware

3

LabVIEW App as a Server : at least 3 options

PCAS

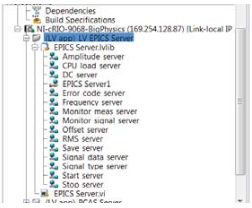
- C++ class library available in EPICS base
- Ai/ao/bi/bo/waveform supported
- Needs additional development to support additional records/fields
- Requires a .dB file
- Supported on Windows, VxWorks, Linux-arm and Linux-x86



1 create CAS
2 load .db file
3 run CAS
4 write PV double array
5 read PV double array
6 write PV string
7 read PV string
8 stop CAS
9 close CAS

Shared variables

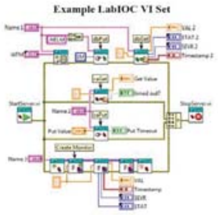
- Built-in LabVIEW RT and DSC
- No dB file
- Programmatic creation of CA Server and variables
- Only VAL field supported (alarms fields on LV DSC)



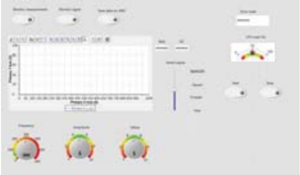
Dependencies
Build Specifications
NI-cRIO-9068-BigPhysics (169.254.128.87) [Link-local IP
(LV app) LV EPICS Server
EPICS Server.lvlib
Amplitude server
CPU load server
DC server
EPICS Server1
Error code server
Frequency server
Monitor meas server
Monitor signal server
Offset server
RMS server
Save server
Signal data server
Signal type server
Start server
Stop server
EPICS Server.vi
(LV app) PCAS Server

LabIOC

- Developed by the observatory of science for ELI beamlines lasers
- Full support of core EPICS records
- Relies only on native LabVIEW functions



LabVIEW App as an EPICS client + Soft IOC

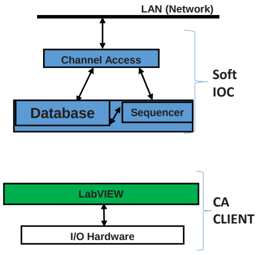


CSS EPICS client
(remote control of LV App)

NI Linux RT, VxWorks (LV RT)

Windows
Linux
Pharlap (LV RT)

Embedded EPICS Base Server (SoftIOC) OR Remote



LV CA Client (via shared variables)

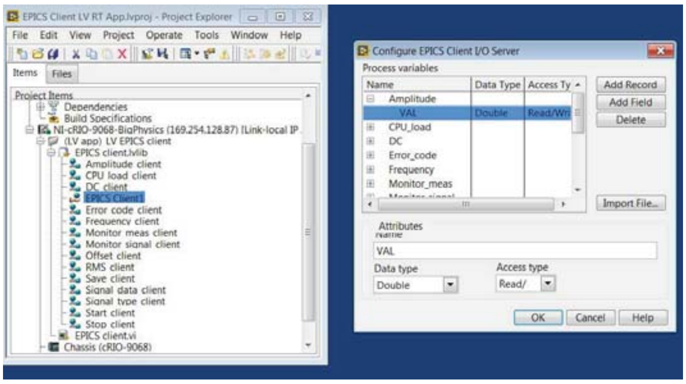
Conclusion

Several options to interface NI products with EPICS…

- Using LabVIEW as an IOC Server/client:
  - ➢ Built-in : shared variables
  - ➢ Add-ons by NI : PCAS VI library
  - ➢ 3rd party add-ons : Shared memory, LabIOC, CALab, etc…
- Without using LabVIEW:
  - ➢ cRIO : NI-RIO C API with NI Linux RT and Embedded Epics Base
  - ➢ PXI : custom device support with instruments C drivers

…. On several operating systems (Windows, Linux desktop, VxWorks, Pharlap, NI Linux RT)

EPICS client configuration



Project Items
- Dependencies
- Build Specifications
- NI-cRIO-9068-BioPhysics (169.254.128.87) [Link-local IP
  - (LV app) LV EPICS client
    - EPICS client.lvlib
      - Amplitude client
      - CPU load client
      - DC client
      - EPICS Client1
      - Error code client
      - Frequency client
      - Monitor meas client
      - Monitor signal client
      - Offset client
      - RMS client
      - Save client
      - Signal data client
      - Signal type client
      - Start client
      - Stop client
    - EPICS client.vi
  - Chassis (cRIO-9068)

Process variables

Name	Data Type	Access Ty
Amplitude		
VAL	Double	Read/Wri
CPU_load		
DC		
Error_code		
Frequency		
Monitor_meas		

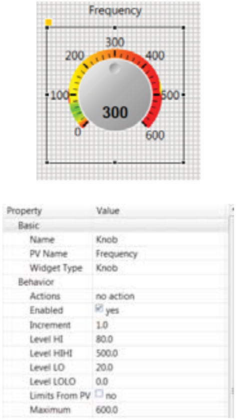
Attributes

Name: VAL

Data type: Double

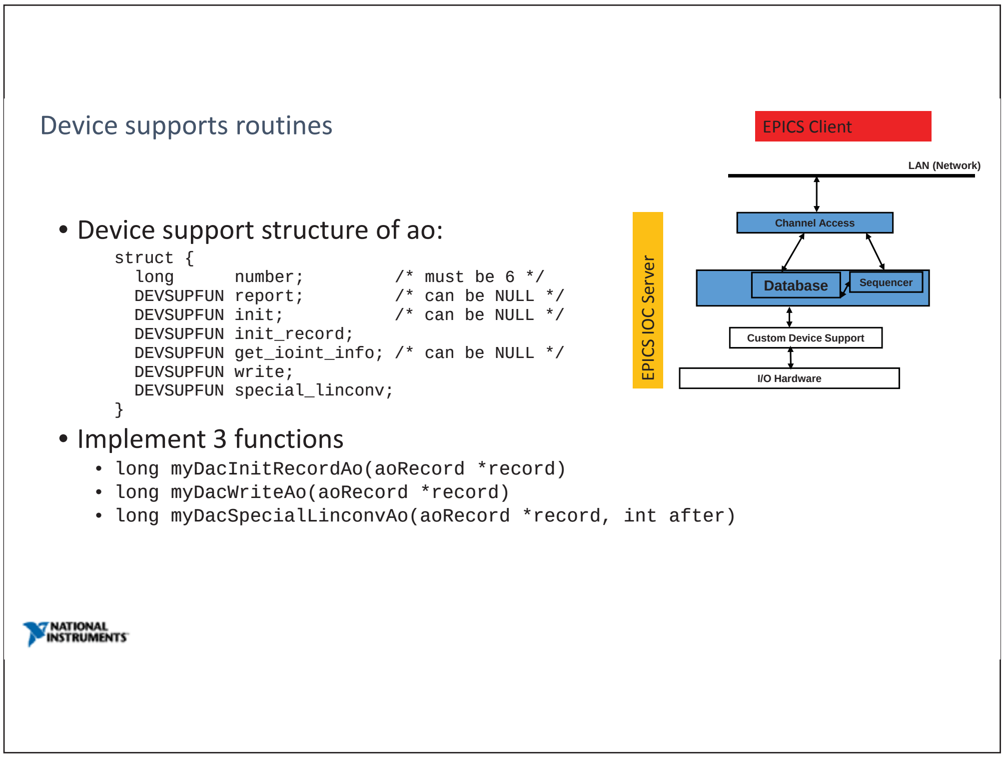
Access type: Read/

LabVIEW



Property	Value
Basic	
Name	Knob
PV Name	Frequency
Widget Type	Knob
Behavior	
Actions	no action
Enabled	☑ yes
Increment	1.0
Level HI	80.0
Level HIHI	500.0
Level LO	20.0
Level LOLO	0.0
Limits From PV	☐ no
Maximum	600.0

CSS



Device supports routines

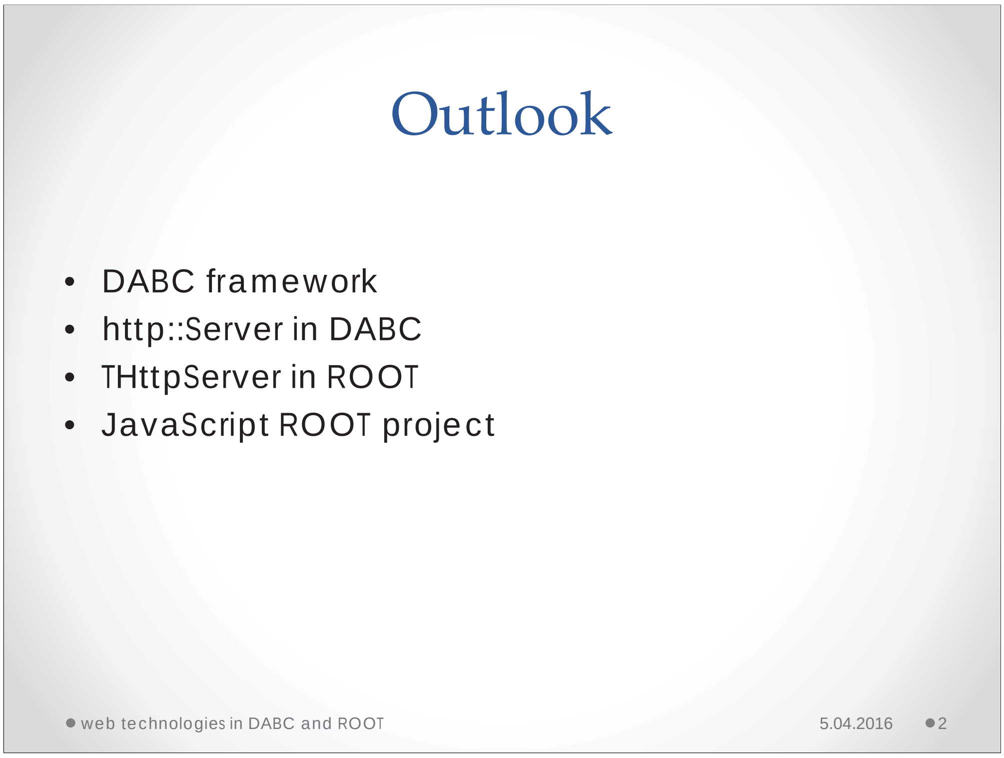
- Device support structure of ao:

```
struct {
  long      number;         /* must be 6 */
  DEVSUPFUN report;         /* can be NULL */
  DEVSUPFUN init;           /* can be NULL */
  DEVSUPFUN init_record;
  DEVSUPFUN get_ioint_info; /* can be NULL */
  DEVSUPFUN write;
  DEVSUPFUN special_linconv;
}
```

- Implement 3 functions
  - `long myDacInitRecordAo(aoRecord *record)`
  - `long myDacWriteAo(aoRecord *record)`
  - `long myDacSpecialLinconvAo(aoRecord *record, int after)`

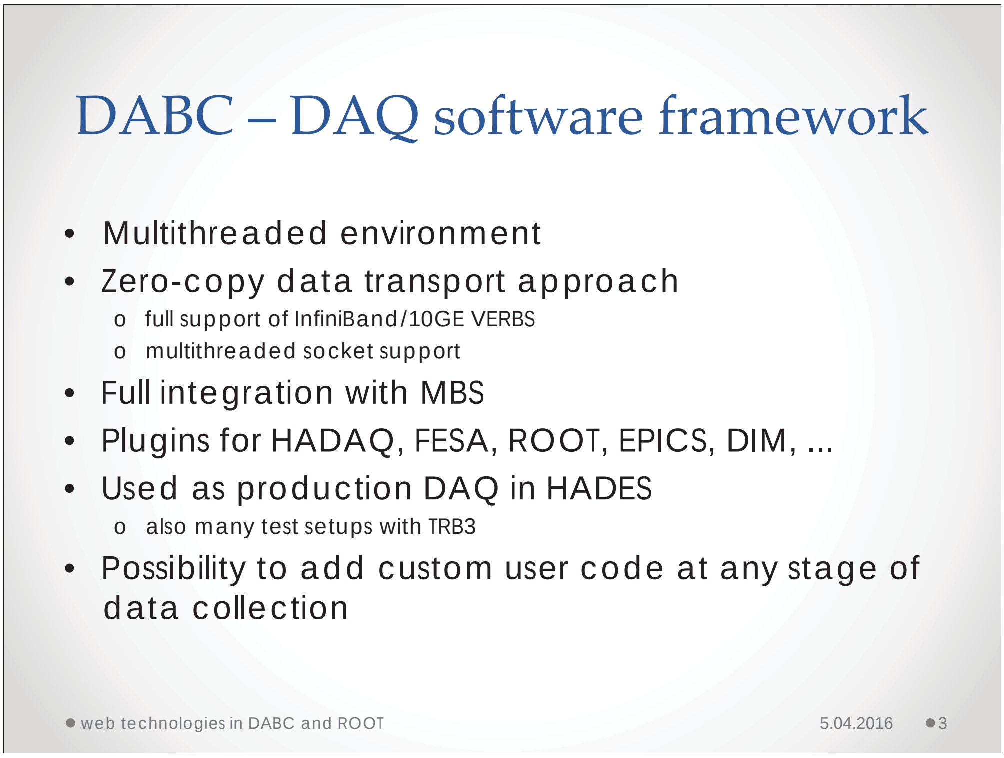
Use of web technologies in DABC and ROOT

Sergey Linev (GSI)



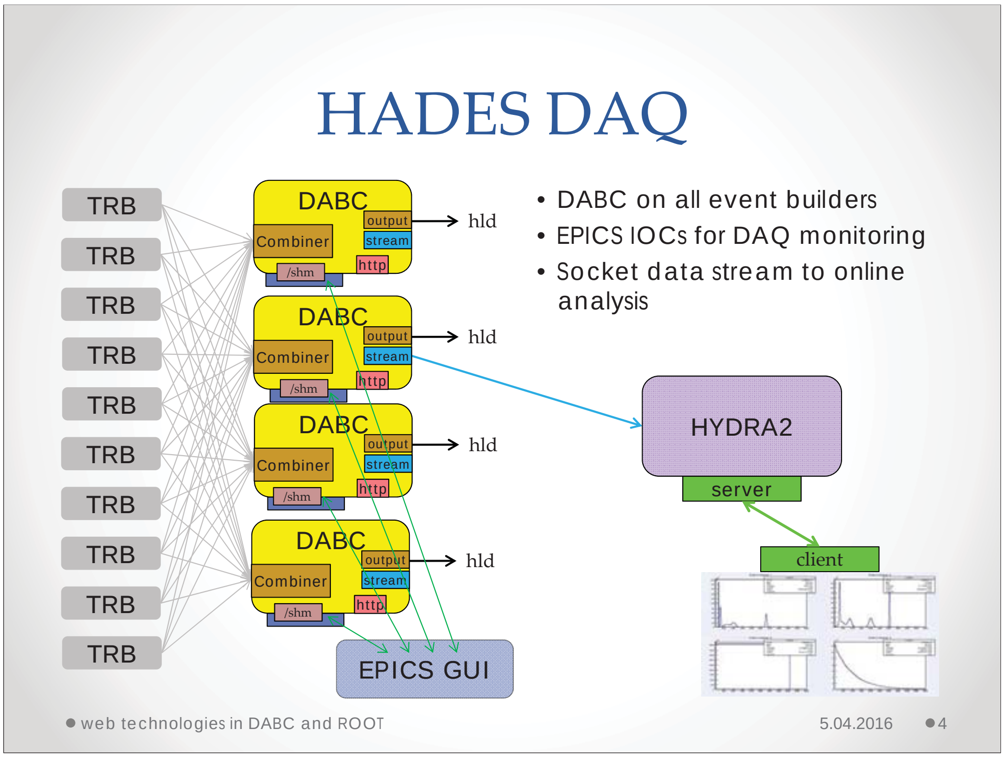
Outlook

- DABC framework
- http::Server in DABC
- THttpServer in ROOT
- JavaScript ROOT project



DABC – DAQ software framework

- Multithreaded environment
- Zero-copy data transport approach
  - full support of InfiniBand/10GE VERBS
  - multithreaded socket support
- Full integration with MBS
- Plugins for HADAQ, FESA, ROOT, EPICS, DIM, ...
- Used as production DAQ in HADES
  - also many test setups with TRB3
- Possibility to add custom user code at any stage of data collection



HADES DAQ

- DABC on all event builders
- EPICS IOCs for DAQ monitoring
- Socket data stream to online analysis

http::Server in DABC

- Uses **civetweb** embed server
- Thread-safe access to DAQ records
  - including history of changes
- Simple HTTP requests syntax
- Access to control data from:
  - MBS – the GSI DAQ system
  - EPICS – the control system
  - DIM – CERN control system
  - FESA – CERN/GSI accelerator control system
  - any other plugin can be implemented
- **JavaScript ROOT** as user interface

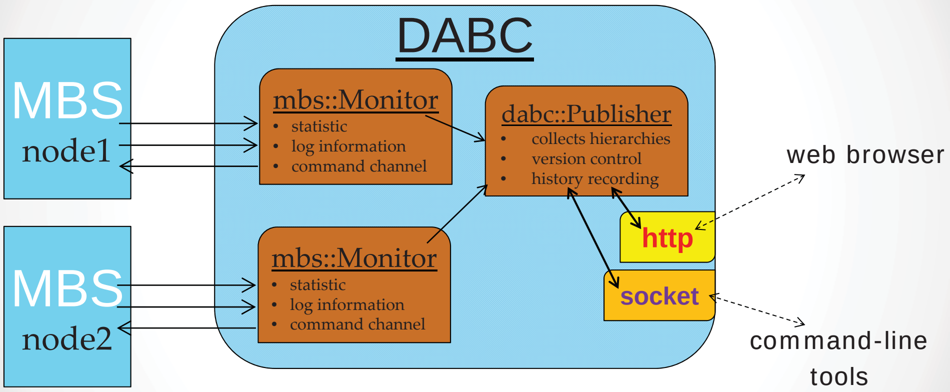
TRB3 DAQ application

Rate: 8.69712 MB/s Ev: 3413.02 Hz Lost:0 Hz

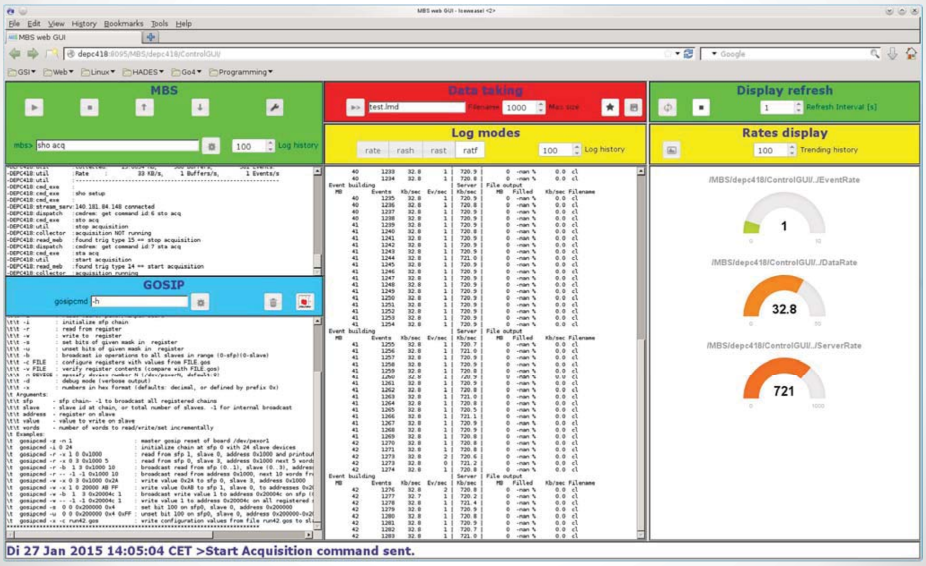
Info: HADAQ Combiner starts. Runid:259424224, numinp:5, numout:1 flush:2.0

```
----------------------------------------
Events:    1.6m  Rate: 3412.3 ev/s  Data:     4.0 GB  Rate: 8.695 MB/s
Dropped:   3404  Rate:    0.0 ev/s  Data:     2.8 MB  Rate: 0.000 MB/s
File: missing, failed or not found on Combiner/Output1
inp port     pkt      data    MB/s   disc  err32   bufs  qu  drop  lost    TRB          TDC         progr state   triggers
 0 50000  795.3k  831.3 MB   1.735      0      0   6218   0  3144   104 0x8000 [3000,3001,3002,3003] 20 Ready   0xa7ebd6 1 1
 1 50001  798.8k  835.0 MB   2.313      0      0   6242   8  7626   104 0x8010 [3010,3011,3012,3013] 23 Ready   0xa7ebd7 1 1
 2 50002  797.8k  833.9 MB   1.735      0      0   6236   9  4140   268 0x8020 [3020,3021,3022,3023] 22 Ready   0xa7ebd7 1 1
 3 50003  795.0k  831.0 MB   2.072      0      0   6212   9    42   218 0x8030 [3030,3031,3032,3033] 20 Ready   0xa7ebd7 1 1
 4 50004  796.1k  832.1 MB   1.721      0      0   6222   6  3040    42 0x8040 [3040,3041,3042,3043] 21 Ready   0xa7ebd7 1 1
```

http access to MBS



MBS web GUI



```
-DEPC418:util       :Rate      :       33 KB/s,     1 Buffers/s,       1 Events/s
-DEPC418:util       :-----------------------------------------------------------
-DEPC418:cmd_exe    :
-DEPC418:cmd_exe    :sho setup
-DEPC418:cmd_exe    :
-DEPC418:stream_serv:140.181.84.148 connected
-DEPC418:dispatch   :cmdrem: get command id:6 sto acq
-DEPC418:cmd_exe    :sto acq
-DEPC418:util       :stop acquisition
-DEPC418:collector  :acquisition NOT running
-DEPC418:read_meb   :found trig type 15 == stop acquisition
-DEPC418:dispatch   :cmdrem: get command id:7 sta acq
-DEPC418:cmd_exe    :sta acq
-DEPC418:util       :start acquisition
-DEPC418:read_meb   :found trig type 14 == start acquisition
-DEPC418:collector  :acquisition running
```

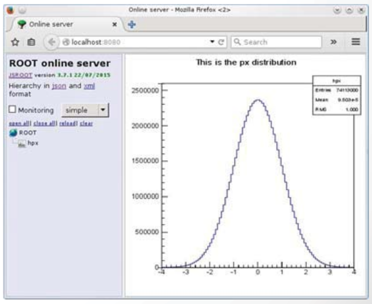
Di 27 Jan 2015 14:05:04 CET >Start Acquisition command sent.

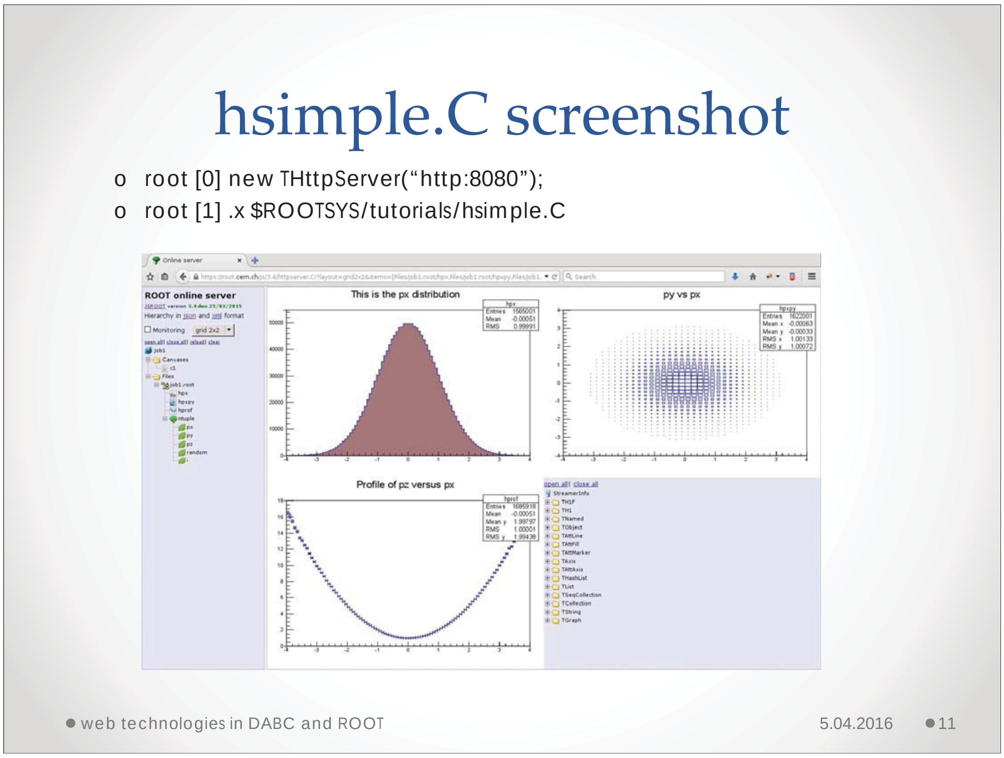
THttpServer class in ROOT

- similar approach as in DABC
- access to application objects
  - files, canvases, histograms via gROOT
  - objects could be registered directly
    - serv->Register(“/graphs”, gr);
- deliver objects data in different formats
  - binary, JSON, XML, image(s)
  - also access to objects members
- execution of objects methods
- user interface with JavaScript ROOT

Simple example

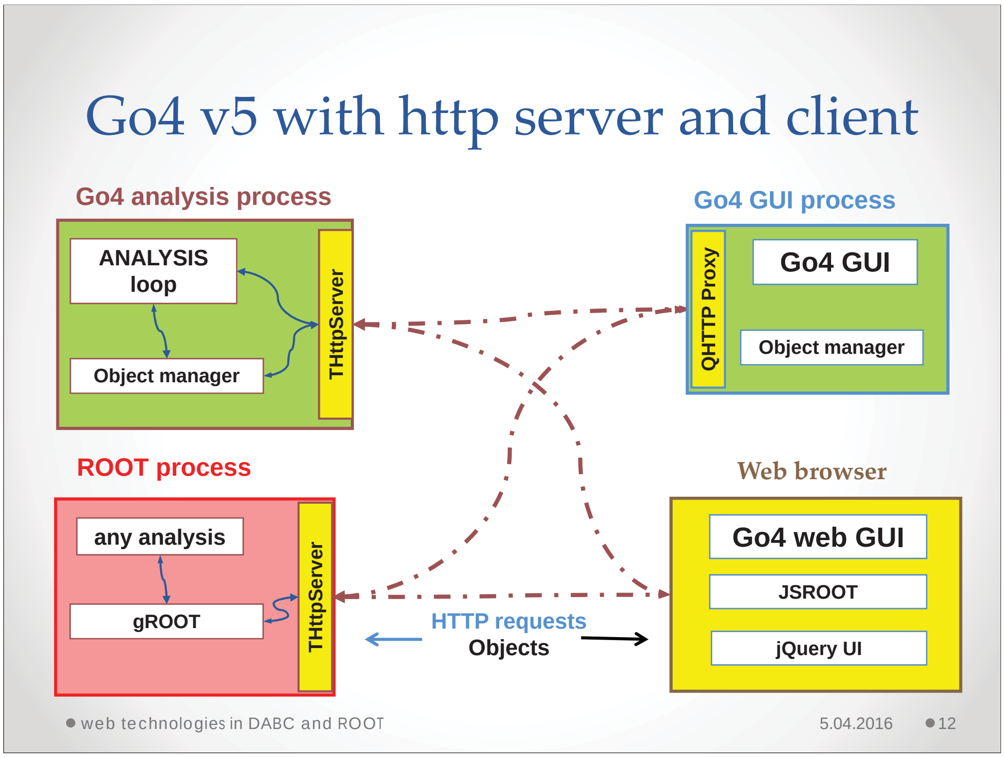
```
{
  // http server with port 8080
  auto serv = new THttpServer("http:8080");

  // Create histogram, accessible via gROOT
  auto hpx = new TH1F("hpx","This is the px distribution",100,-4,4);

  // run event loop
  while (!gSystem->ProcessEvents()) {
     hpx->FillRandom("gaus", 1000);
  }
}
```





hsimple.C screenshot

- root [0] new THttpServer("http:8080");
- root [1] .x $ROOTSYS/tutorials/hsimple.C



Go4 v5 with http server and client

Go4 analysis process

- ANALYSIS loop
- Object manager
- THttpServer

Go4 GUI process

- QHTTP Proxy
- Go4 GUI
- Object manager

ROOT process

- any analysis
- gROOT
- THttpServer

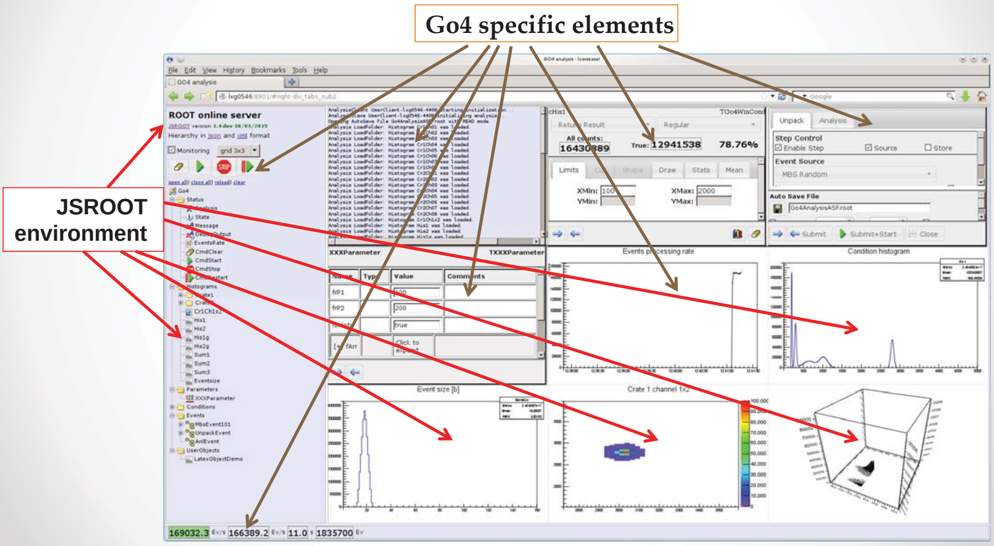
Web browser

- Go4 web GUI
- JSROOT
- jQuery UI

HTTP requests

Objects

Go4 v5 web GUI



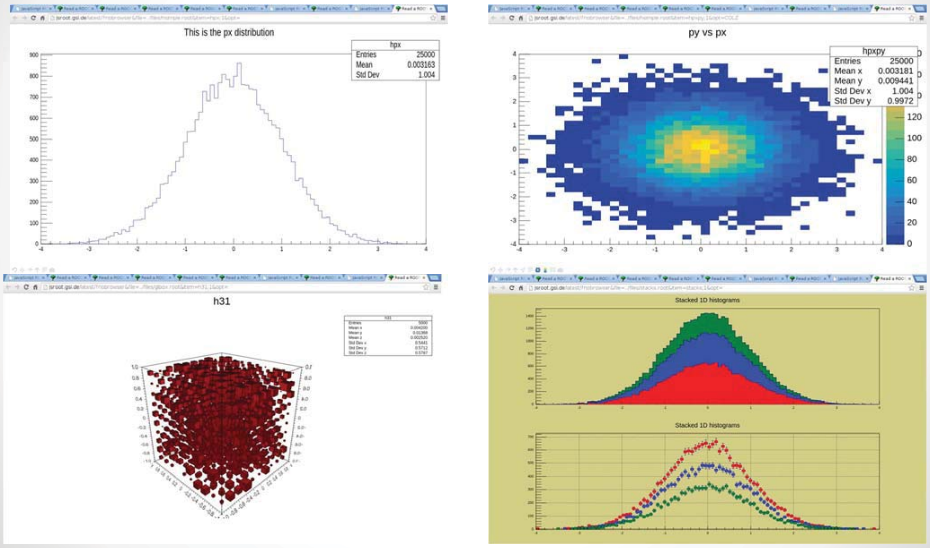
Go4 specific elements

JSROOT environment

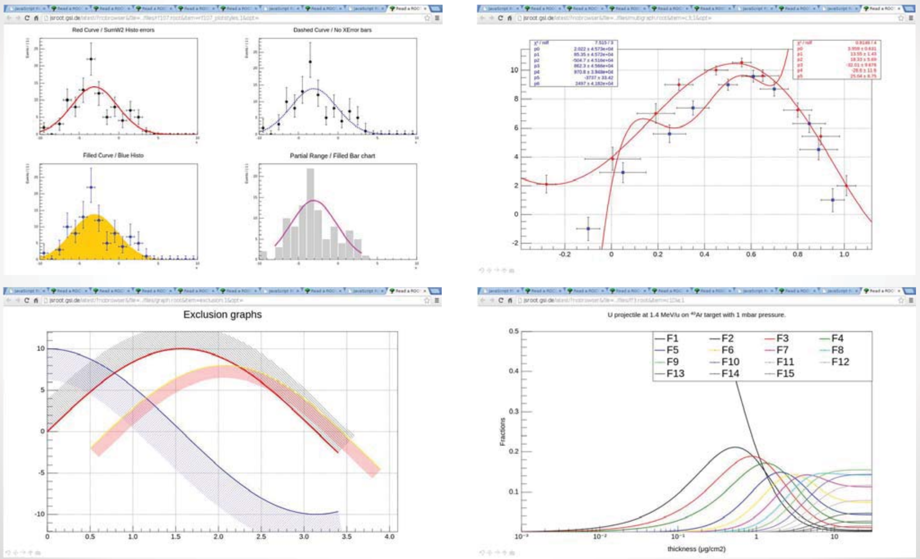
JavaScript ROOT

- https://root.cern.ch/js/
- Reading ROOT files
  - binary I/O using streamer infos
  - direct support of ROOT JSON files
- Interactive display of ROOT objects on HTML page
  - TH1/TH2/TH3, THStack
  - all TGraph-based classes, TMultiGraph
  - TCanvas, TF1, TGaxis, ...
  - Preliminary TGeo support
- Implements generic UI for THttpServer
  - provides simple API to build custom HTML pages
- Can be reused for drawing non-ROOT objects

JSROOT screenshots



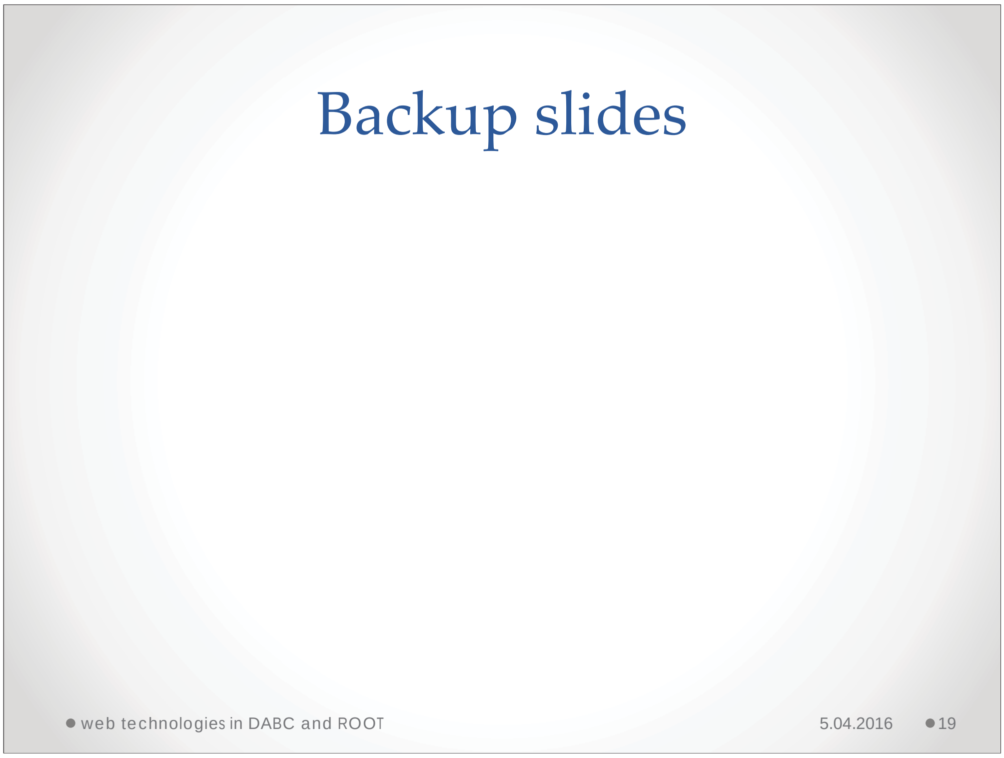
JSROOT screenshots



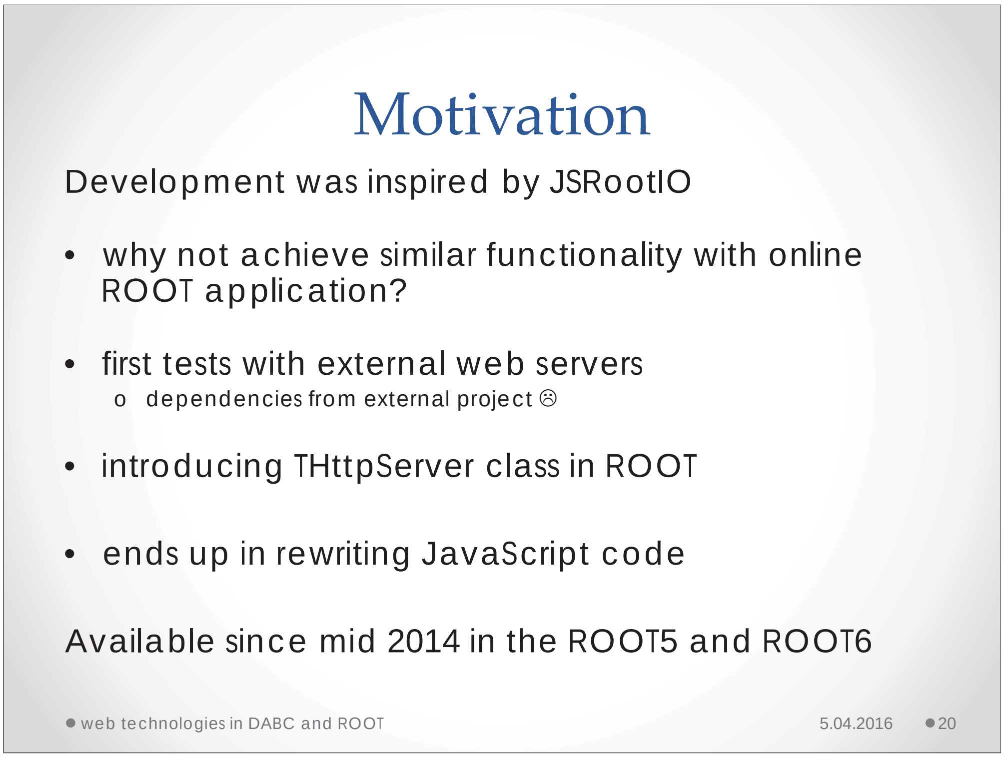
TGeo support in JSROOT

Conclusion

- Use of HTTP for DAQ and ROOT
- Generic and powerful UI with JSROOT
- Easy to extend for custom needs



Backup slides

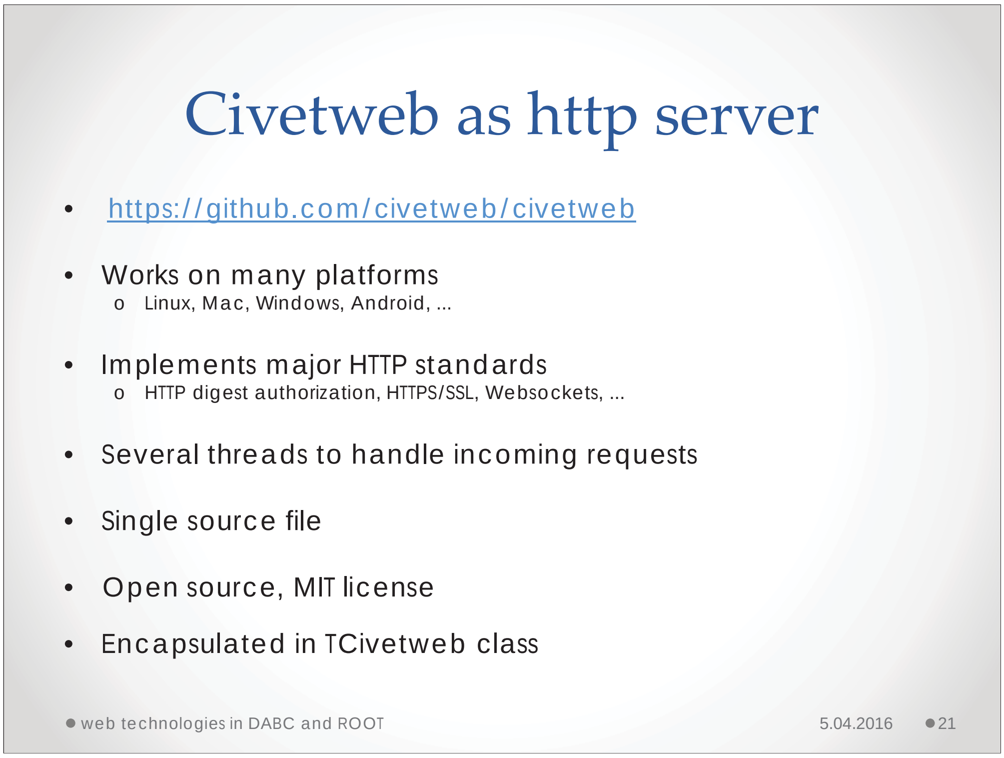


Motivation

Development was inspired by JSRootIO

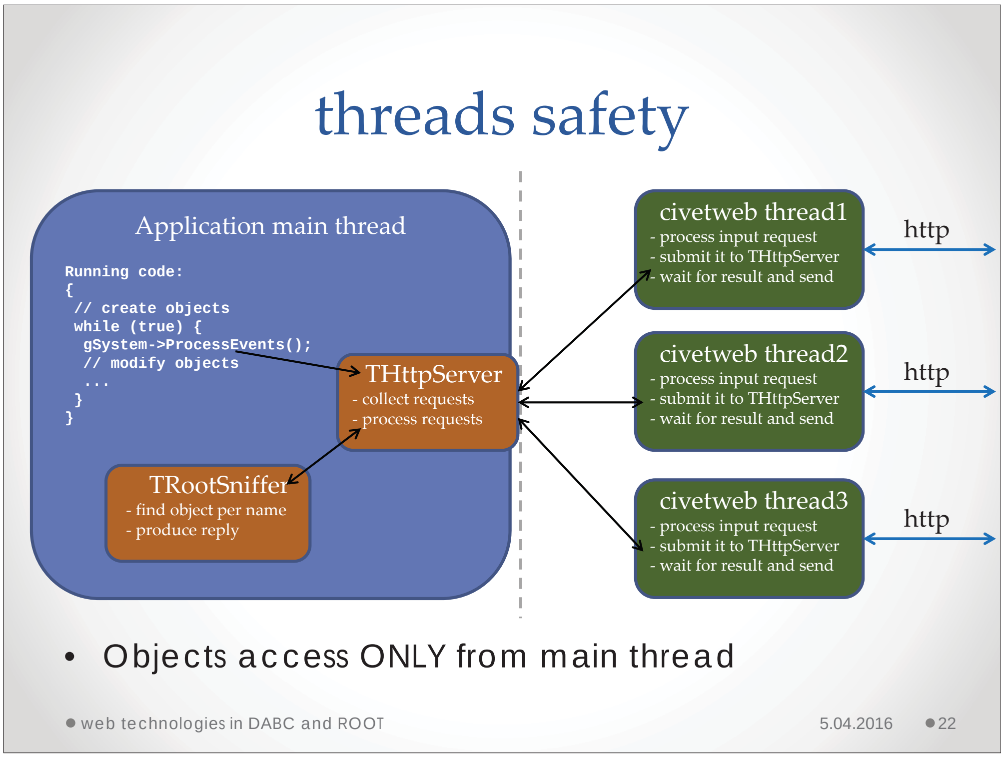
- why not achieve similar functionality with online ROOT application?
- first tests with external web servers
  - dependencies from external project ☹
- introducing THttpServer class in ROOT
- ends up in rewriting JavaScript code

Available since mid 2014 in the ROOT5 and ROOT6



Civetweb as http server

- https://github.com/civetweb/civetweb
- Works on many platforms
  - Linux, Mac, Windows, Android, ...
- Implements major HTTP standards
  - HTTP digest authorization, HTTPS/SSL, Websockets, ...
- Several threads to handle incoming requests
- Single source file
- Open source, MIT license
- Encapsulated in TCivetweb class



threads safety

Application main thread

```
Running code:
{
 // create objects
 while (true) {
  gSystem->ProcessEvents();
  // modify objects
  ...
 }
}
```

THttpServer
- collect requests
- process requests

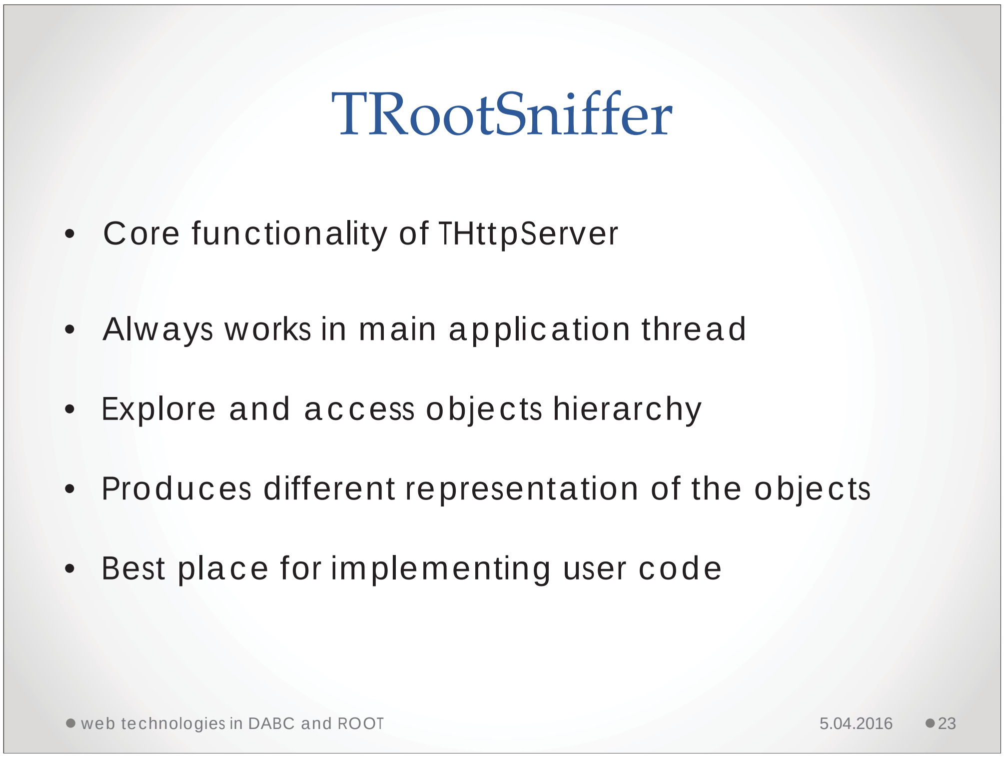
TRootSniffer
- find object per name
- produce reply

civetweb thread1
- process input request
- submit it to THttpServer
- wait for result and send

civetweb thread2
- process input request
- submit it to THttpServer
- wait for result and send

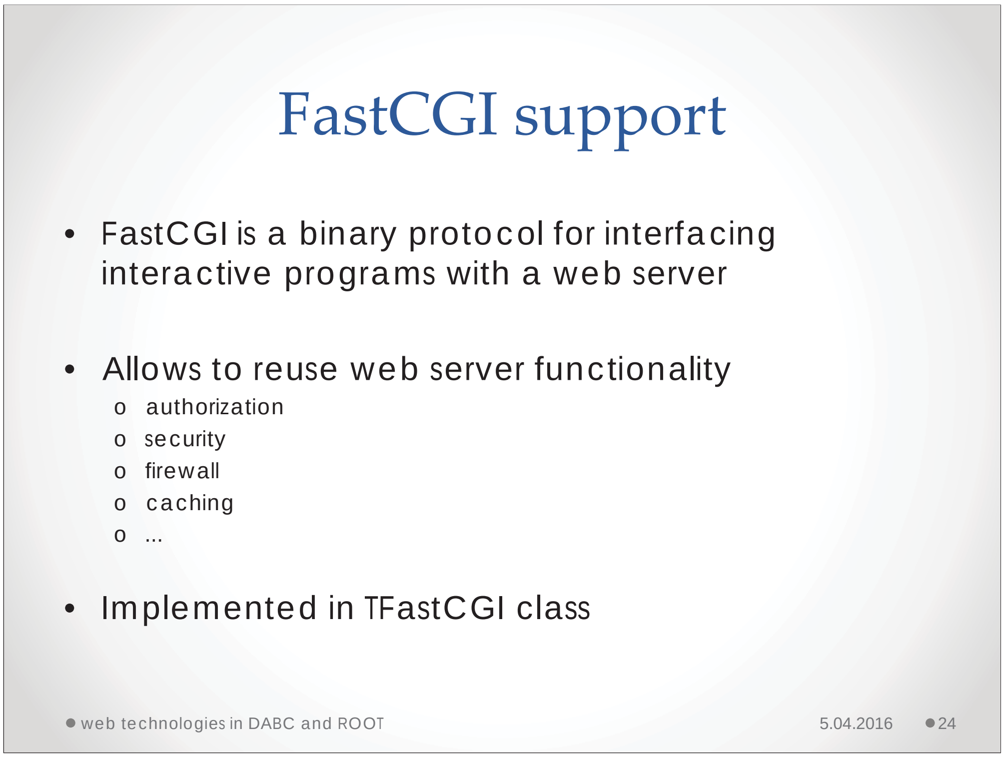
civetweb thread3
- process input request
- submit it to THttpServer
- wait for result and send

- Objects access ONLY from main thread



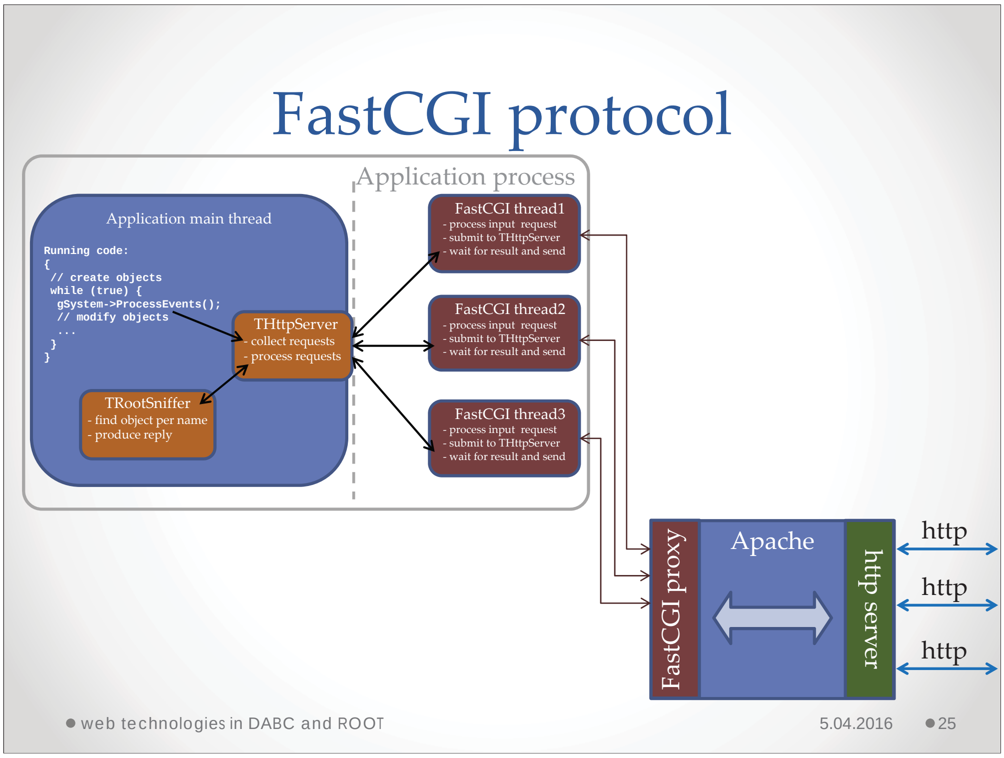
TRootSniffer

- Core functionality of THttpServer
- Always works in main application thread
- Explore and access objects hierarchy
- Produces different representation of the objects
- Best place for implementing user code



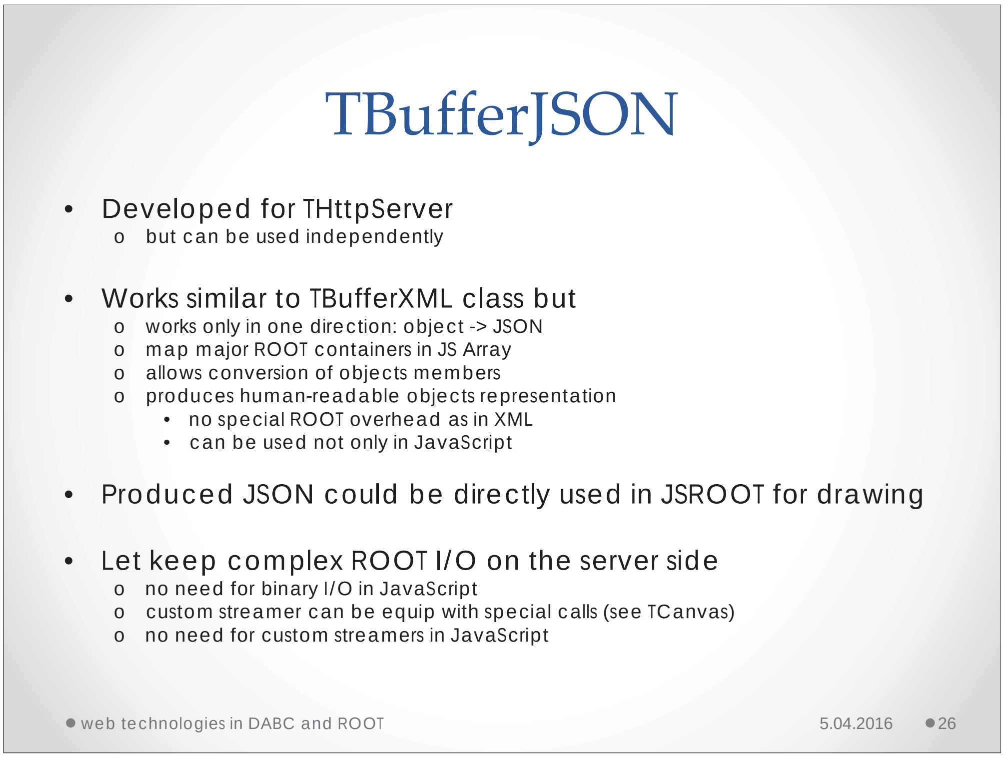
FastCGI support

- FastCGI is a binary protocol for interfacing interactive programs with a web server
- Allows to reuse web server functionality
  - authorization
  - security
  - firewall
  - caching
  - ...
- Implemented in TFastCGI class



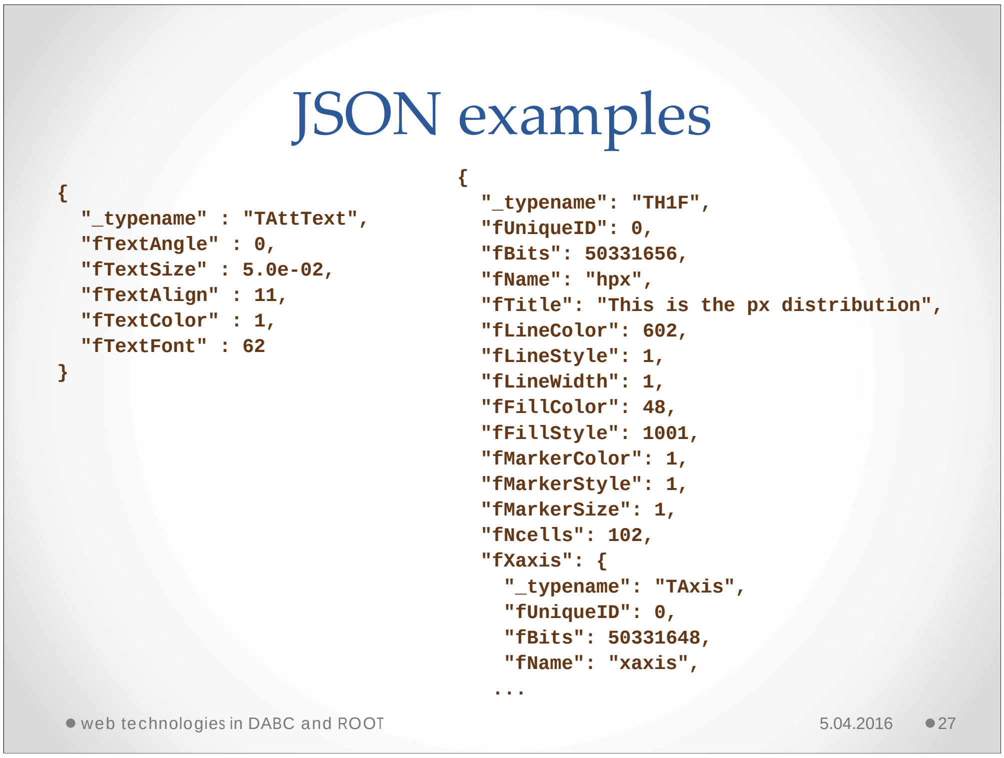
FastCGI protocol

```
Running code:
{
 // create objects
 while (true) {
  gSystem->ProcessEvents();
  // modify objects
   ...
 }
}
```



TBufferJSON

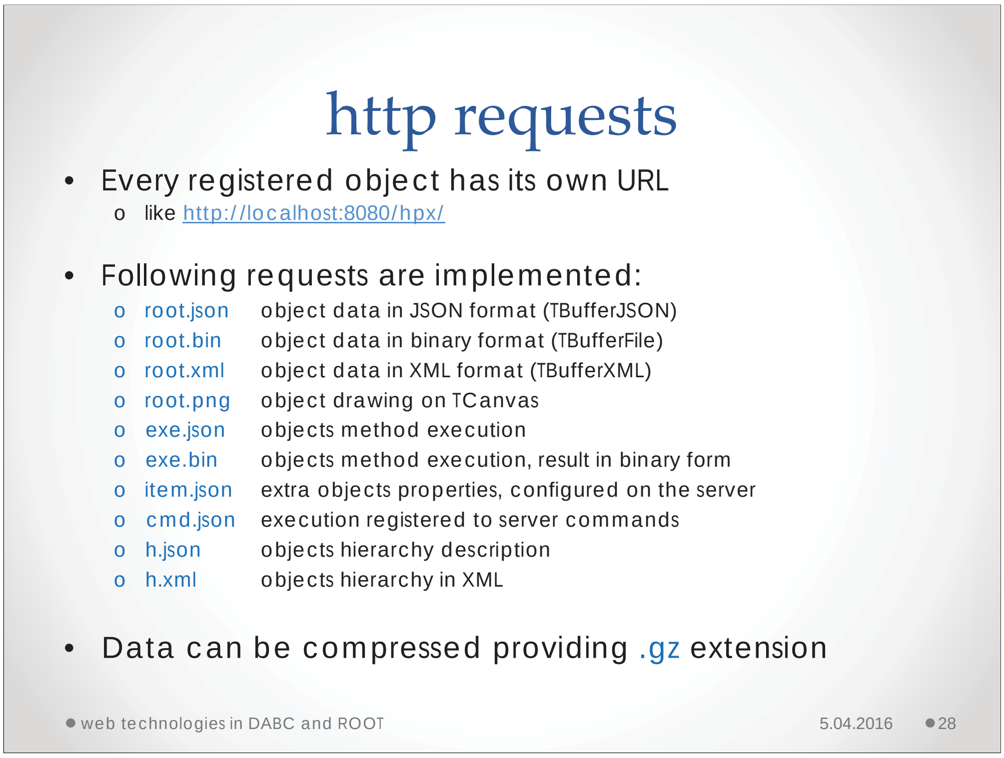
- Developed for THttpServer
  - but can be used independently
- Works similar to TBufferXML class but
  - works only in one direction: object -> JSON
  - map major ROOT containers in JS Array
  - allows conversion of objects members
  - produces human-readable objects representation
    - no special ROOT overhead as in XML
    - can be used not only in JavaScript
- Produced JSON could be directly used in JSROOT for drawing
- Let keep complex ROOT I/O on the server side
  - no need for binary I/O in JavaScript
  - custom streamer can be equip with special calls (see TCanvas)
  - no need for custom streamers in JavaScript



JSON examples

```
{
  "_typename" : "TAttText",
  "fTextAngle" : 0,
  "fTextSize" : 5.0e-02,
  "fTextAlign" : 11,
  "fTextColor" : 1,
  "fTextFont" : 62
}
```

```
{
  "_typename": "TH1F",
  "fUniqueID": 0,
  "fBits": 50331656,
  "fName": "hpx",
  "fTitle": "This is the px distribution",
  "fLineColor": 602,
  "fLineStyle": 1,
  "fLineWidth": 1,
  "fFillColor": 48,
  "fFillStyle": 1001,
  "fMarkerColor": 1,
  "fMarkerStyle": 1,
  "fMarkerSize": 1,
  "fNcells": 102,
  "fXaxis": {
    "_typename": "TAxis",
    "fUniqueID": 0,
    "fBits": 50331648,
    "fName": "xaxis",
   ...
```

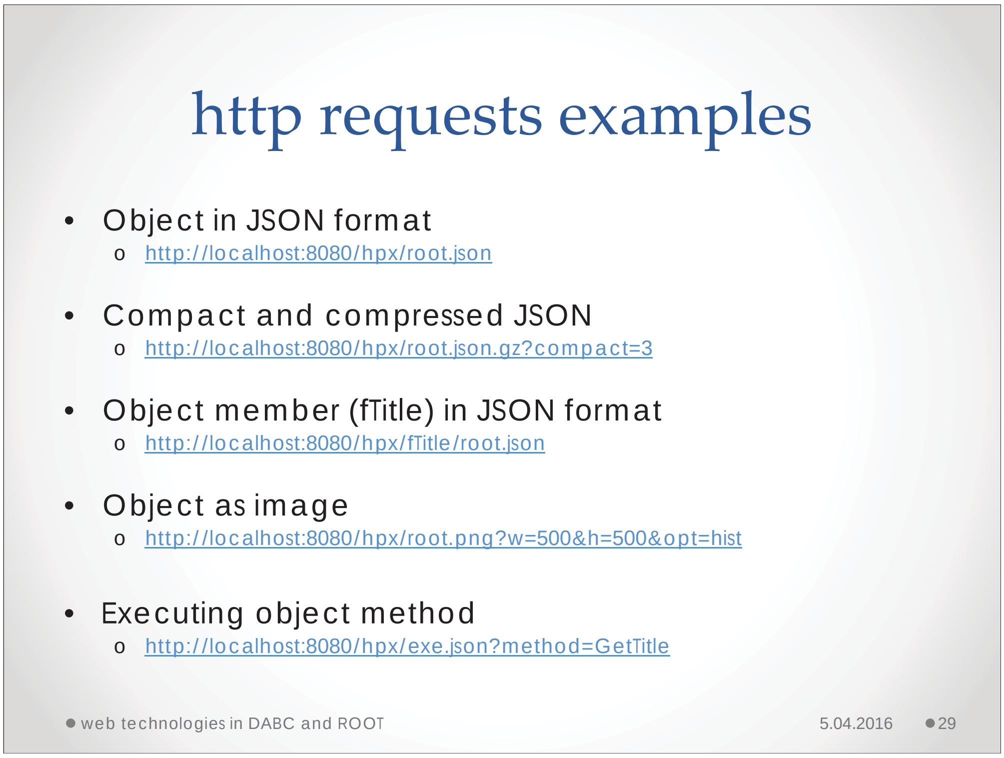


http requests

- Every registered object has its own URL
  - like http://localhost:8080/hpx/
- Following requests are implemented:

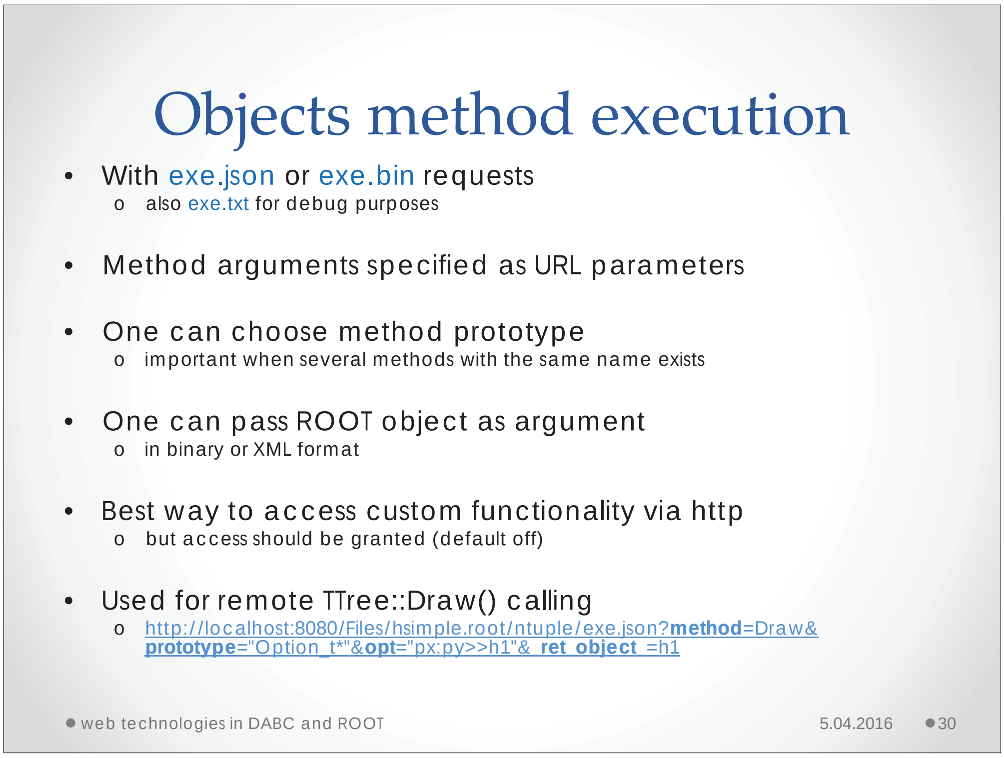
root.json	object data in JSON format (TBufferJSON)
root.bin	object data in binary format (TBufferFile)
root.xml	object data in XML format (TBufferXML)
root.png	object drawing on TCanvas
exe.json	objects method execution
exe.bin	objects method execution, result in binary form
item.json	extra objects properties, configured on the server
cmd.json	execution registered to server commands
h.json	objects hierarchy description
h.xml	objects hierarchy in XML

- Data can be compressed providing .gz extension



http requests examples

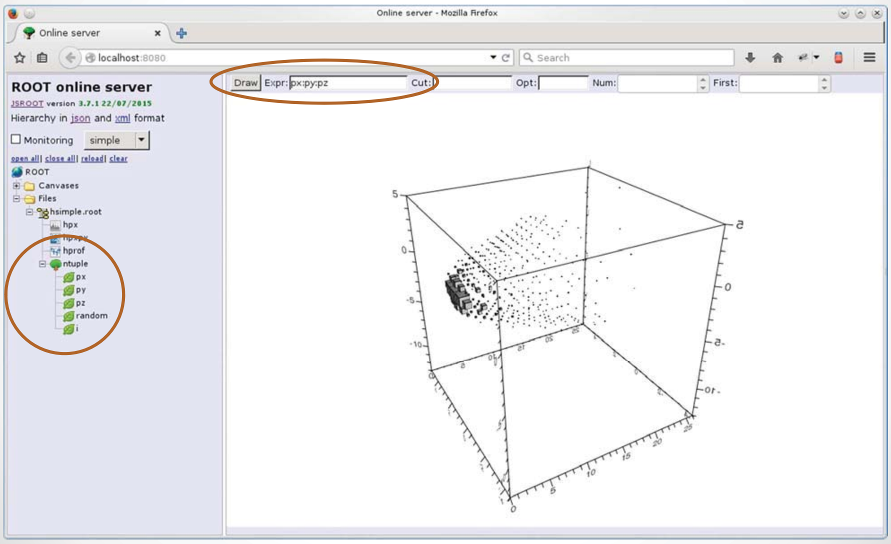
- Object in JSON format
  - http://localhost:8080/hpx/root.json
- Compact and compressed JSON
  - http://localhost:8080/hpx/root.json.gz?compact=3
- Object member (fTitle) in JSON format
  - http://localhost:8080/hpx/fTitle/root.json
- Object as image
  - http://localhost:8080/hpx/root.png?w=500&h=500&opt=hist
- Executing object method
  - http://localhost:8080/hpx/exe.json?method=GetTitle



Objects method execution

- With exe.json or exe.bin requests
  - also exe.txt for debug purposes
- Method arguments specified as URL parameters
- One can choose method prototype
  - important when several methods with the same name exists
- One can pass ROOT object as argument
  - in binary or XML format
- Best way to access custom functionality via http
  - but access should be granted (default off)
- Used for remote TTree::Draw() calling
  - http://localhost:8080/Files/hsimple.root/ntuple/exe.json?**method**=Draw&**prototype**="Option_t*"&**opt**="px:py>>h1"&**_ret_object_**=h1

Remote TTree::Draw

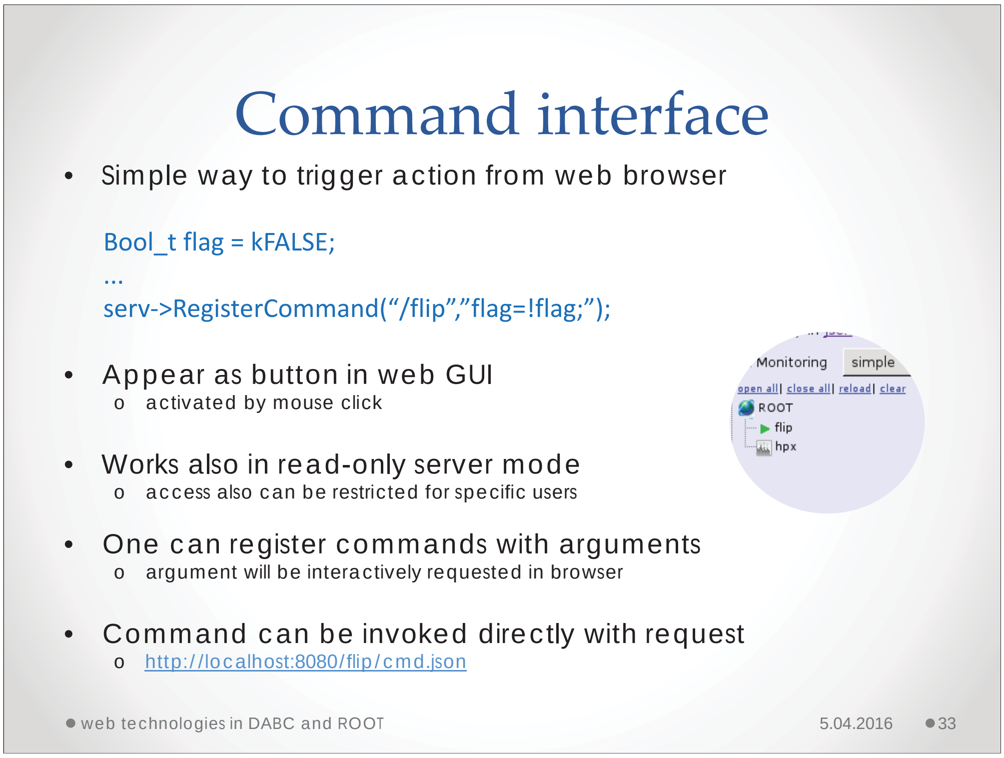


Access control

- By default server started in read-only mode
  - o only objects data can be accessed
  - o methods can not be executed
- One can allow access to objects, folders or methods

```
serv->Restrict("/hpx", "allow=admin");        // allow full access for user with 'admin' account
serv->Restrict("/hpx", "allow=all");           // allow full access for all users
serv->Restrict("/hpx", "allow_method=Rebin");   // allow only Rebin method
```

- Based on authorized user names
  - o either htdigest of civetweb
  - o or user name provided by FastCGI
- One could disable read-only mode completely
  - o serv->SetReadOnly(kFALSE);
    - of course, not recommended



Command interface

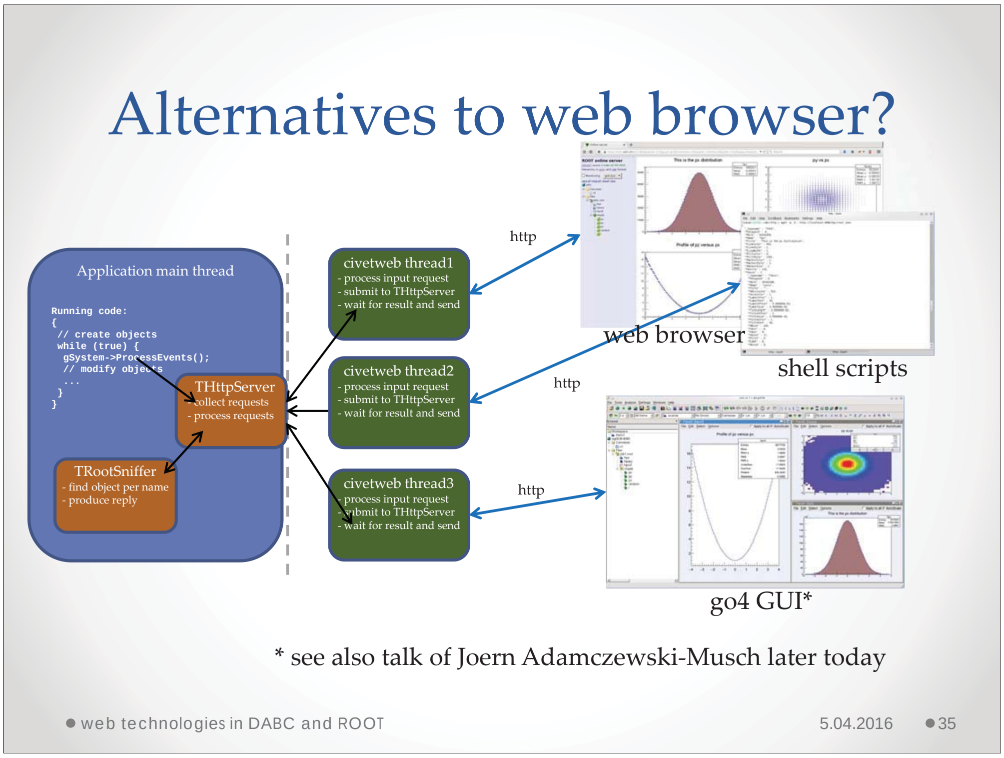
- Simple way to trigger action from web browser

```
Bool_t flag = kFALSE;
...
serv->RegisterCommand("/flip","flag=!flag;");
```

- Appear as button in web GUI
  - activated by mouse click
- Works also in read-only server mode
  - access also can be restricted for specific users
- One can register commands with arguments
  - argument will be interactively requested in browser
- Command can be invoked directly with request
  - http://localhost:8080/flip/cmd.json

Equip user application with http

- Level 0: do nothing
  - just create THttpServer instance
- Level 1: register user objects
- Level 2: add several commands
- Level 3: support user classes
  - write JavaScript code
  - set autoload properties
  - subclass TRootSniffer (to explore user collections)
  - example – go4 classes



Alternatives to web browser?

Application main thread

```
Running code:
{
 // create objects
 while (true) {
  gSystem->ProcessEvents();
  // modify objects
  ...
 }
}
```

THttpServer
- collect requests
- process requests

TRootSniffer
- find object per name
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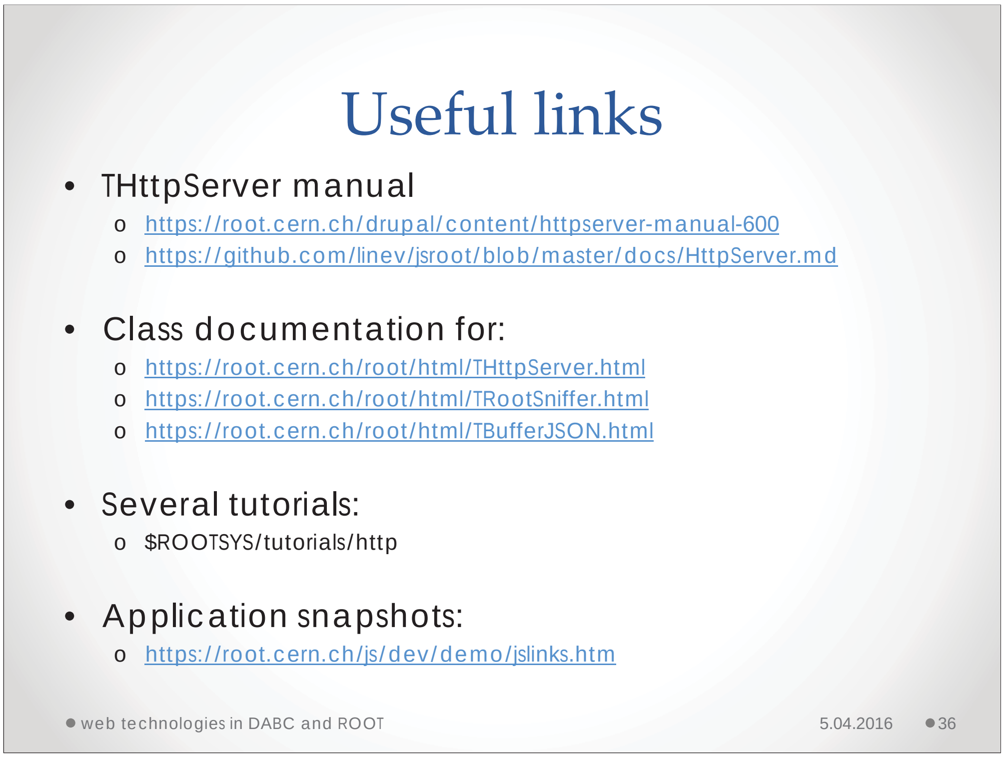
civetweb thread3
- process input request
- submit to THttpServer
- wait for result and send

* see also talk of Joern Adamczewski-Musch later today



Useful links

- THttpServer manual
  - https://root.cern.ch/drupal/content/httpserver-manual-600
  - https://github.com/linev/jsroot/blob/master/docs/HttpServer.md
- Class documentation for:
  - https://root.cern.ch/root/html/THttpServer.html
  - https://root.cern.ch/root/html/TRootSniffer.html
  - https://root.cern.ch/root/html/TBufferJSON.html
- Several tutorials:
  - $ROOTSYS/tutorials/http
- Application snapshots:
  - https://root.cern.ch/js/dev/demo/jslinks.htm

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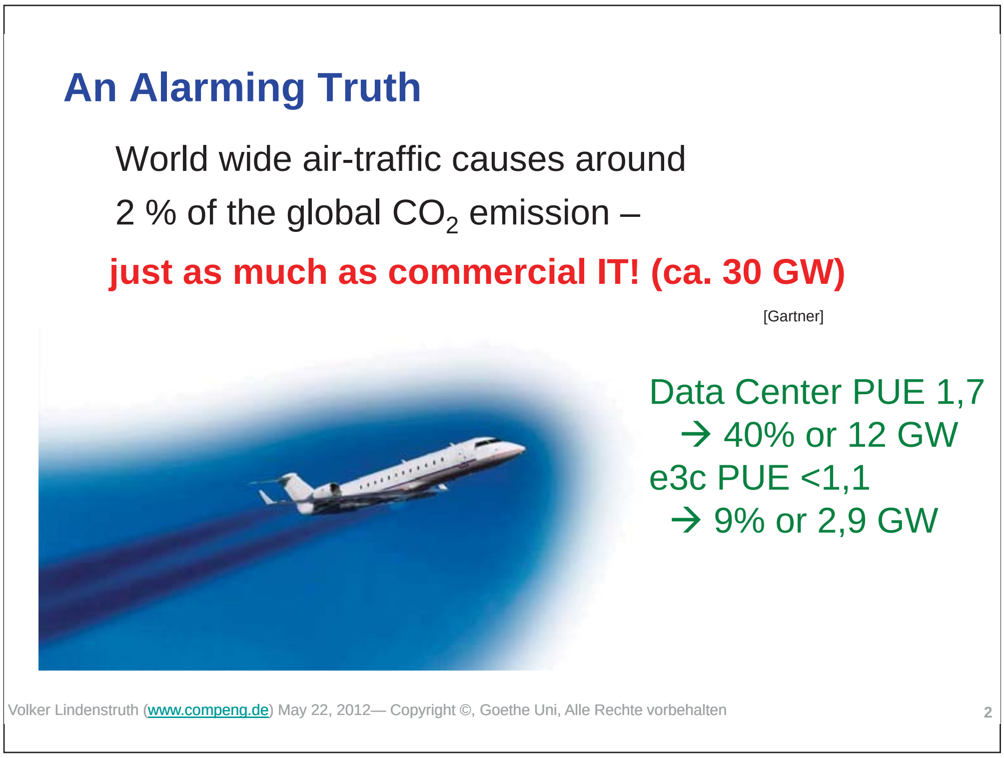


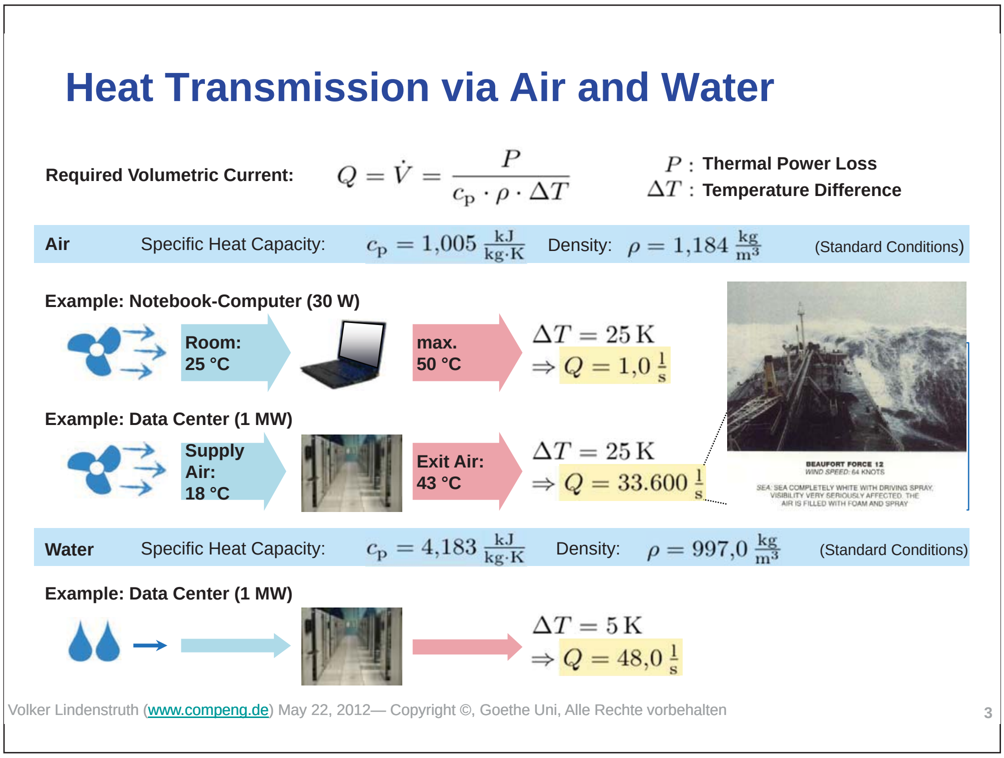
An Alarming Truth

World wide air-traffic causes around
2 % of the global CO_2 emission –

just as much as commercial IT! (ca. 30 GW)

[Gartner]

Data Center PUE 1,7
→ 40% or 12 GW
e3c PUE <1,1
→ 9% or 2,9 GW



Heat Transmission via Air and Water

Required Volumetric Current: $Q = \dot{V} = \frac{P}{c_p \cdot \rho \cdot \Delta T}$

P : **Thermal Power Loss**
ΔT : **Temperature Difference**

Air Specific Heat Capacity: $c_p = 1{,}005\,\frac{\mathrm{kJ}}{\mathrm{kg \cdot K}}$ Density: $\rho = 1{,}184\,\frac{\mathrm{kg}}{\mathrm{m^3}}$ (Standard Conditions)

Example: Notebook-Computer (30 W)

Room: 25 °C → **max. 50 °C**

$\Delta T = 25\,\mathrm{K}$
$\Rightarrow Q = 1{,}0\,\frac{\mathrm{l}}{\mathrm{s}}$

Example: Data Center (1 MW)

Supply Air: 18 °C → **Exit Air: 43 °C**

$\Delta T = 25\,\mathrm{K}$
$\Rightarrow Q = 33.600\,\frac{\mathrm{l}}{\mathrm{s}}$

BEAUFORT FORCE 12
WIND SPEED: 64 KNOTS

SEA: SEA COMPLETELY WHITE WITH DRIVING SPRAY. VISIBILITY VERY SERIOUSLY AFFECTED. THE AIR IS FILLED WITH FOAM AND SPRAY

Water Specific Heat Capacity: $c_p = 4{,}183\,\frac{\mathrm{kJ}}{\mathrm{kg \cdot K}}$ Density: $\rho = 997{,}0\,\frac{\mathrm{kg}}{\mathrm{m^3}}$ (Standard Conditions)

Example: Data Center (1 MW)

$\Delta T = 5\,\mathrm{K}$
$\Rightarrow Q = 48{,}0\,\frac{\mathrm{l}}{\mathrm{s}}$

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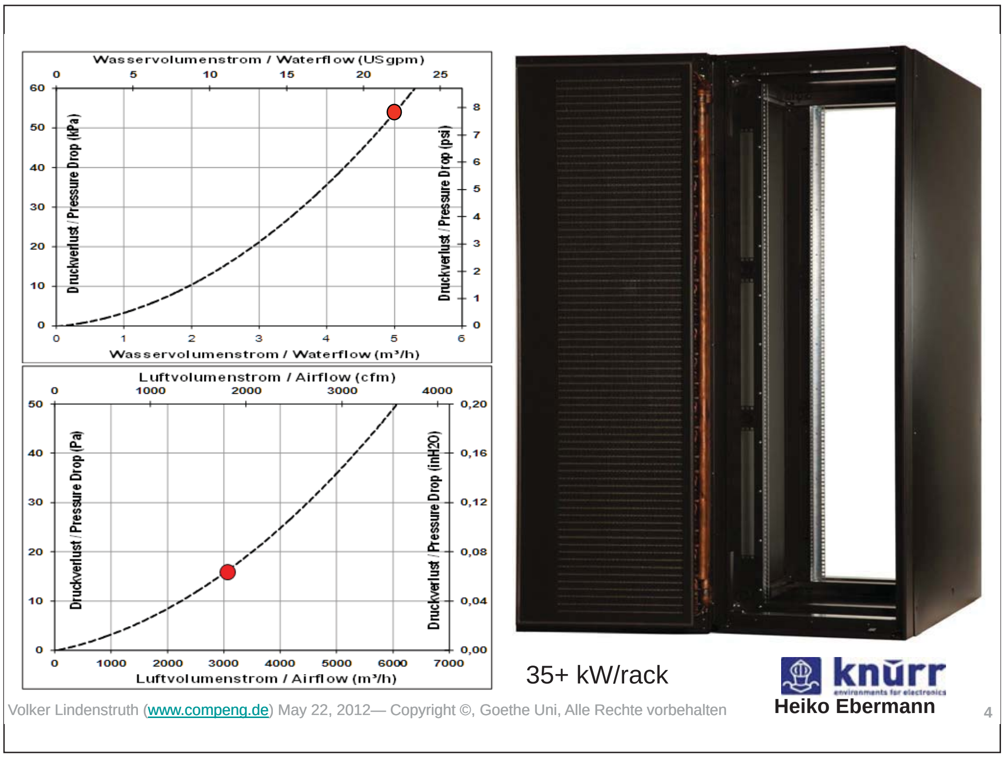

35+ kW/rack

knürr environments for electronics
Heiko Ebermann

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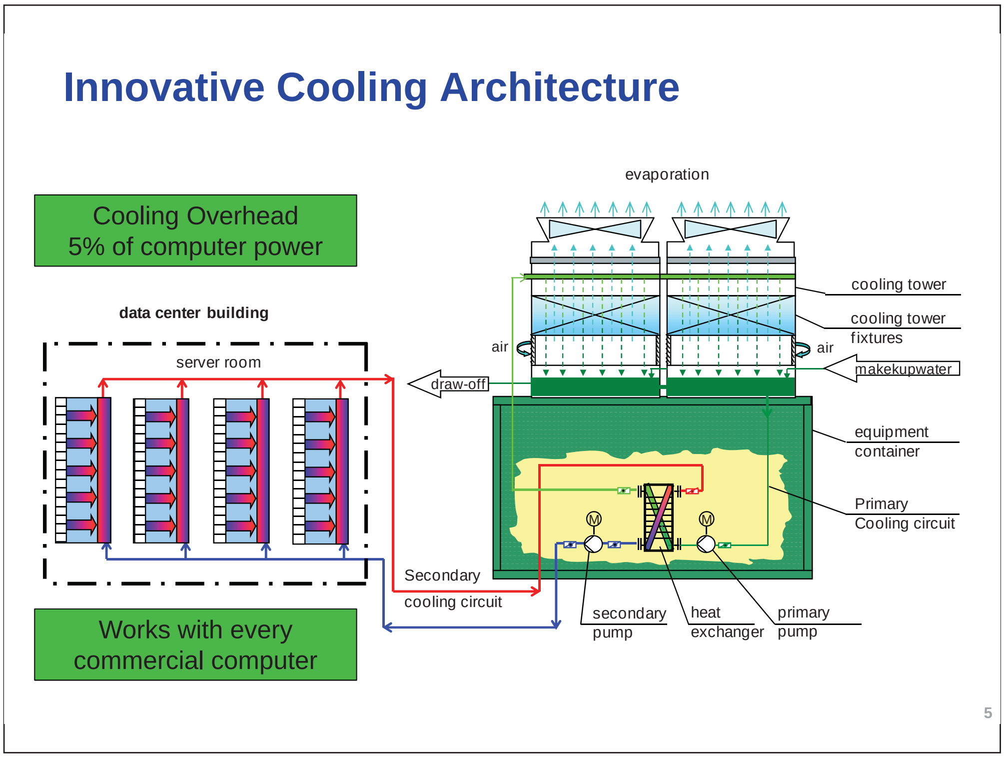
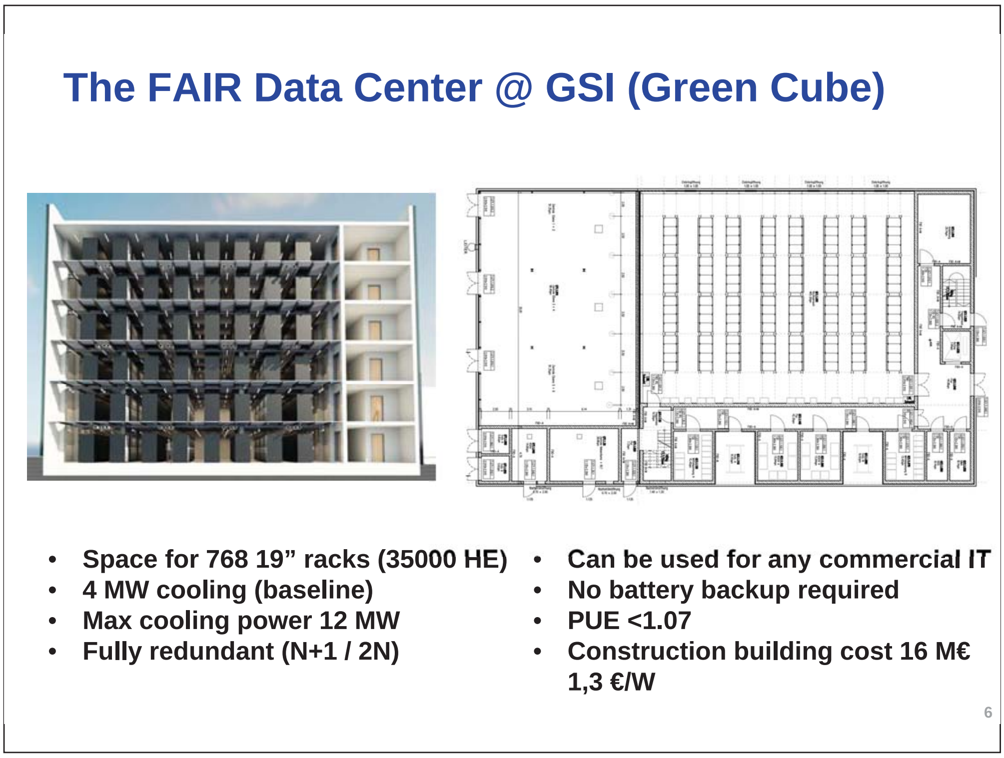


Innovative Cooling Architecture

Cooling Overhead
5% of computer power

Works with every
commercial computer



The FAIR Data Center @ GSI (Green Cube)

- Space for 768 19” racks (35000 HE)
- 4 MW cooling (baseline)
- Max cooling power 12 MW
- Fully redundant (N+1 / 2N)
- Can be used for any commercial IT
- No battery backup required
- PUE <1.07
- Construction building cost 16 M€ 1,3 €/W

Die Elektroleistungsbilanz Kälte/RLT ist in nachfolgender Tabelle zusammengestellt:

ELEKTRISCHER LEISTUNGSBEDARF	**elektrischer Leistungsbedarf Kälte/RLT im** **theoretischen Maximallastfall** (22°C Feuchtkugeltemperatur)		**elektrischer Leistungsbedarf Kälte/RLT im** **Vollast-Auslegungsfall** (22°C Feuchtkugeltemperatur)		**elektrischer Leistungsbedarf Kälte/RLT bei** **Jahresmitteltemperatur** (Frankfurt/Main, ca. 10,1°C / ca. 76%rF) / ca. 8,0°C Feuchtkugeltemp.)	
Bezeichnung	Leistung elektrisch gesamt kW_{el}	Anteil an "Zwischen-summe"	Leistung elektrisch gesamt kW_{el}	Anteil an "Zwischen-summe"	Leistung elektrisch gesamt kW_{el}	Anteil an "Zwischen-summe"
Kühlwassererzeugung						
Summe Kühlturmventilatoren	264,0	27,7%	220,0	24,7%	132,0	48,9%
IT-Kühlwasserzentralen						
Summe Pumpengruppen Vebraucherseite	237,4	24,9%	237,4	26,6%	47,5	17,6%
Summe Pumpengruppen Erzeugerseite	417,2	43,8%	415,1	46,6%	83,0	30,8%
Technik-Kühlwasserzentrale						
Summe Pumpengruppe Vebraucherseite	3,5	0,4%	3,5	0,4%	0,7	0,3%
Summe Pumpengruppe Erzeugerseite	5,2	0,5%	5,2	0,6%	1,0	0,4%
Umluftkühlgeräte ELT-Räume GC						
Summe Umluftkühlgeräte ELT-Räume GC	17,1	1,8%	2,7	0,3%	0,8	0,3%
Be- und Entlüftung GC						
Ventilator RLT-Zuluftgerät	2,0	0,2%	2,0	0,2%	2,0	0,7%
Summe Abluftventilatoren	0,2	0,0%	0,2	0,0%	0,2	0,1%
Entlüftung GT						
Abluftventilator Kühlwasserzentralen GC-Ebenen	4,5	0,5%	4,5	0,5%	2,3	0,8%
Abluftventilator Kühlwasserzentrale Technik + NSHV TGA	0,4	0,0%	0,4	0,0%	0,2	0,1%
Zwischensumme	***952,1***		***891,6***		***269,8***	
Rundung	7,9	0,8%	8,4	0,9%	10,2	3,8%
Elektrischer Leistungsbedarf gesamt	**960**		**900**		**280**	
IT-Kühlleistungsbedarf	12.000,0		12.000		12.000	
Elektrischer Leistungsbedarf gesamt / IT-Kühlleistungsbedarf	8,0%		7,5%		2,3%	

Tabelle: Elektroleistungsbilanz Kälte/RLT

Awards

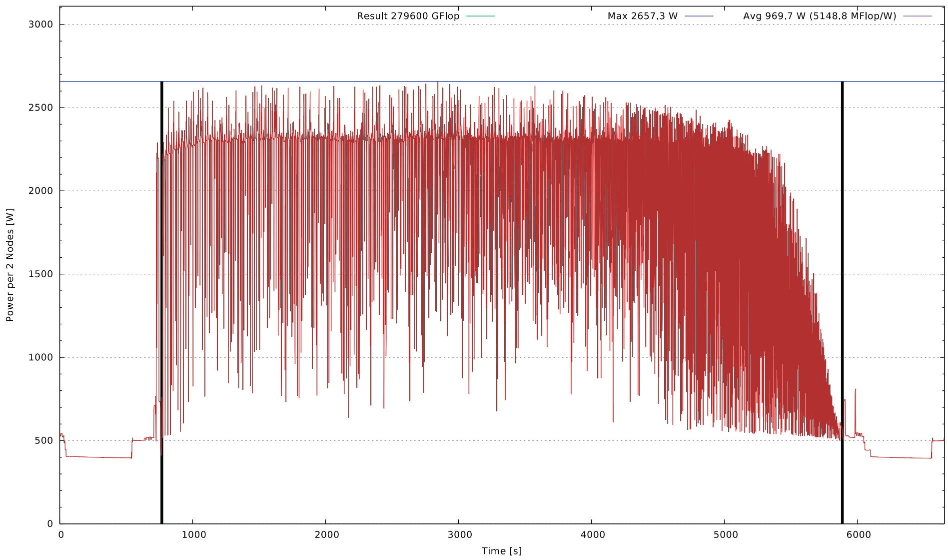
- Green-IT Award Bundesregierung „Visionäre Gesamtkonzepte“
- Deutscher Rechenzentrumpreis 2012 - Energieeffizienz
- Deutscher Rechenzentrumspreis 2013 – Visionäre RZ Architektur
- Nominiert für den Deutschen Rechenzentrumspreis 2014 - Energieefizienz
- DataCenterDynamics EMEA Award 2013 – Data Center Blueprint
- BroadGroup EMEA Awards Special Commendation – Energy Efficiency
- „Land der Ideen“2012 for LOEWE-CSC
- *Green Cube* Project the Month, BMBF
- 5 Nominierungen mit 4 zweiten Plätzen für Data Center Dynamics EMEA Awards – 2011, 2012, 2013
- 2 Platz bei den Deutschen Internet Awards 2012
- 1. Platz DataCloud Awards 2015, Monaco

L-CSC

The Green500 Top 10
November 2014

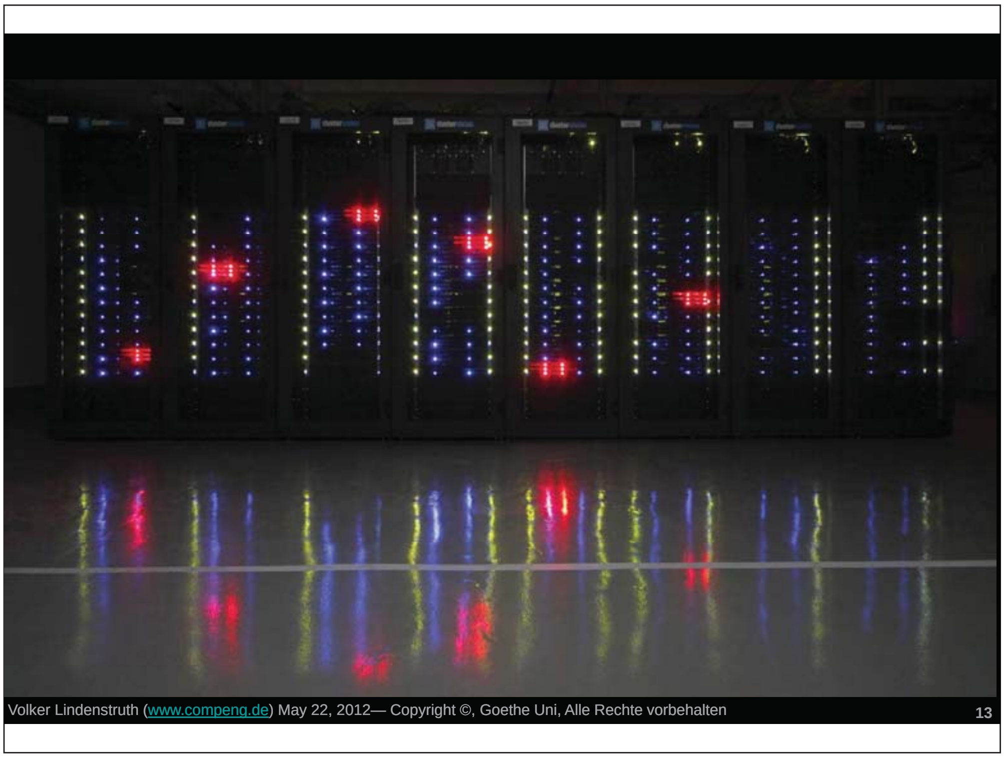
#1 L-CSC-GSI Helmholtz Center 5200 MF/W
#2 Suiren-High Energy Accelerator Research Organization /KEK

HPL power profile



Summary

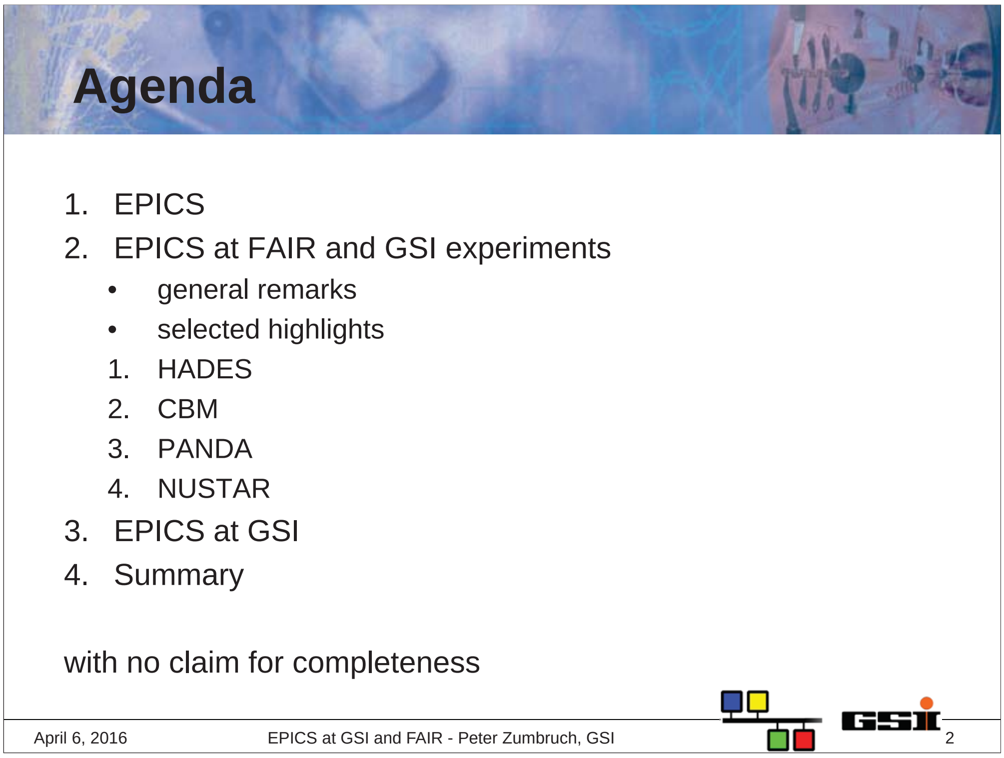
- **Data Center**
  - Data center architecture allows cost significant savings:
    - » CAPEX: 3.7 €/W for Tier-3 data center
    - » OPEX: PUE < 1,2
    - » Very small foot print, Green Cube: >50 kW/m^2
  - No assumptions about computer hardware required
  - Backup power can be avoided with redundant energy supplies
  - Indirect free cooling most cost effective
- **Computer**
  - Computers do not get faster they get more parallel
  - Memory bandwidth will improve only slowly
  - Power and cost efficiency in GPGPU/CPU >10x
  - Dramatic cost savings potential in algorithm
  - HPC Architecture developes towards hybrid clusters of NUMA nodes with GPGPU enhancers, connected with a low latency network like Infiniband



EPICS @ GSI and FAIR

Peter Zumbruch

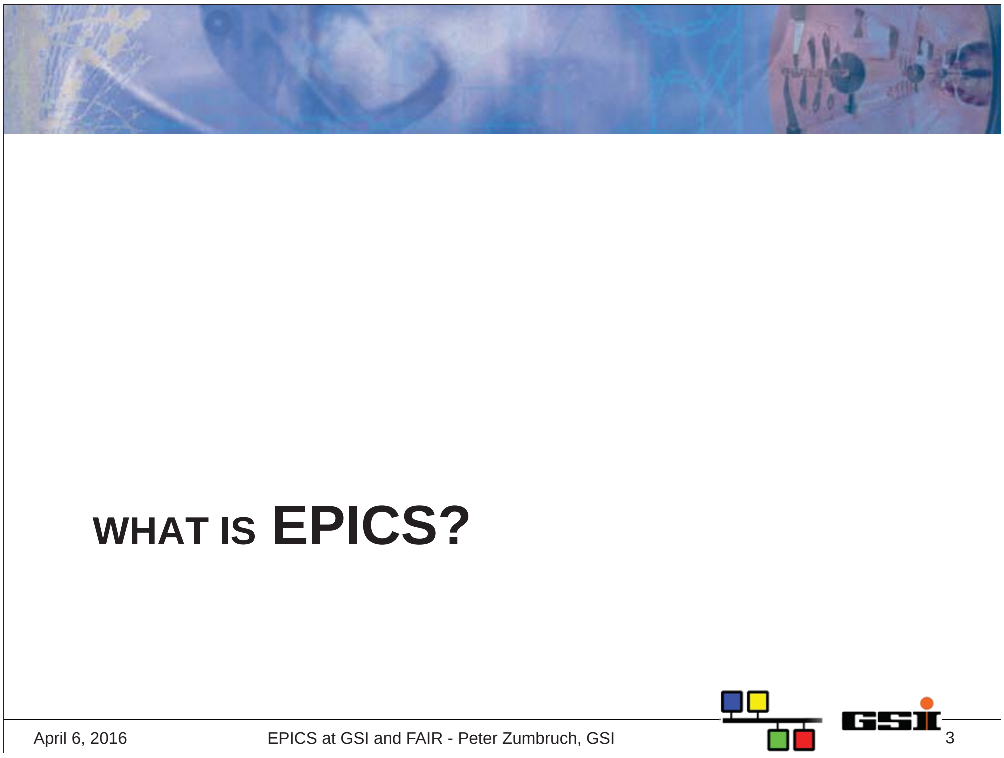
Experiment control systems group GSI
(KS/EE)



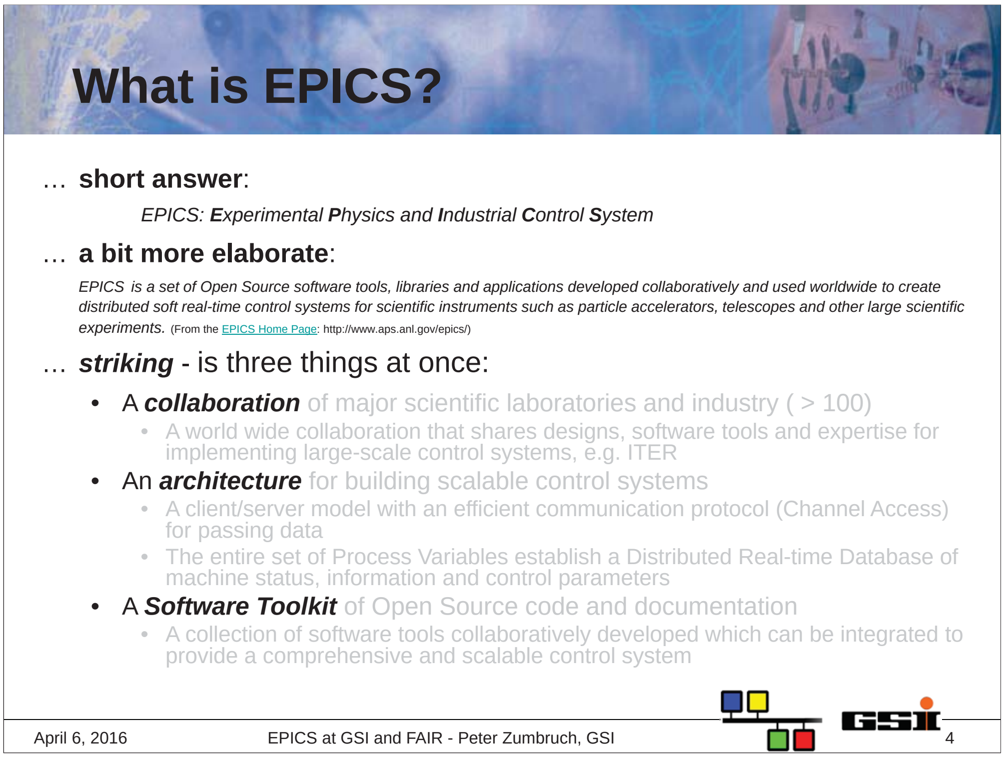
Agenda

1. EPICS
2. EPICS at FAIR and GSI experiments
   - general remarks
   - selected highlights
   1. HADES
   2. CBM
   3. PANDA
   4. NUSTAR
3. EPICS at GSI
4. Summary

with no claim for completeness



WHAT IS EPICS?



What is EPICS?

… **short answer**:

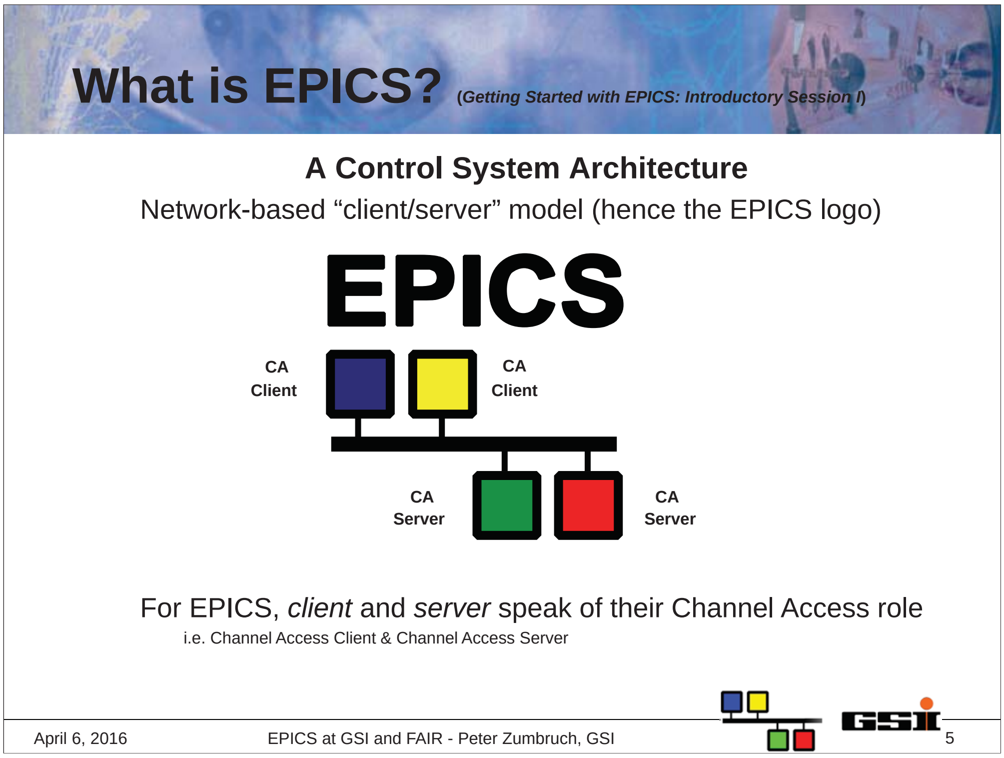
*EPICS: **E**xperimental **P**hysics and **I**ndustrial **C**ontrol **S**ystem*

… **a bit more elaborate**:

EPICS is a set of Open Source software tools, libraries and applications developed collaboratively and used worldwide to create distributed soft real-time control systems for scientific instruments such as particle accelerators, telescopes and other large scientific experiments. (From the EPICS Home Page: http://www.aps.anl.gov/epics/)

… ***striking*** - is three things at once:

- A ***collaboration*** of major scientific laboratories and industry (> 100)
  - A world wide collaboration that shares designs, software tools and expertise for implementing large-scale control systems, e.g. ITER
- An ***architecture*** for building scalable control systems
  - A client/server model with an efficient communication protocol (Channel Access) for passing data
  - The entire set of Process Variables establish a Distributed Real-time Database of machine status, information and control parameters
- A ***Software Toolkit*** of Open Source code and documentation
  - A collection of software tools collaboratively developed which can be integrated to provide a comprehensive and scalable control system



What is EPICS? *(Getting Started with EPICS: Introductory Session I)*

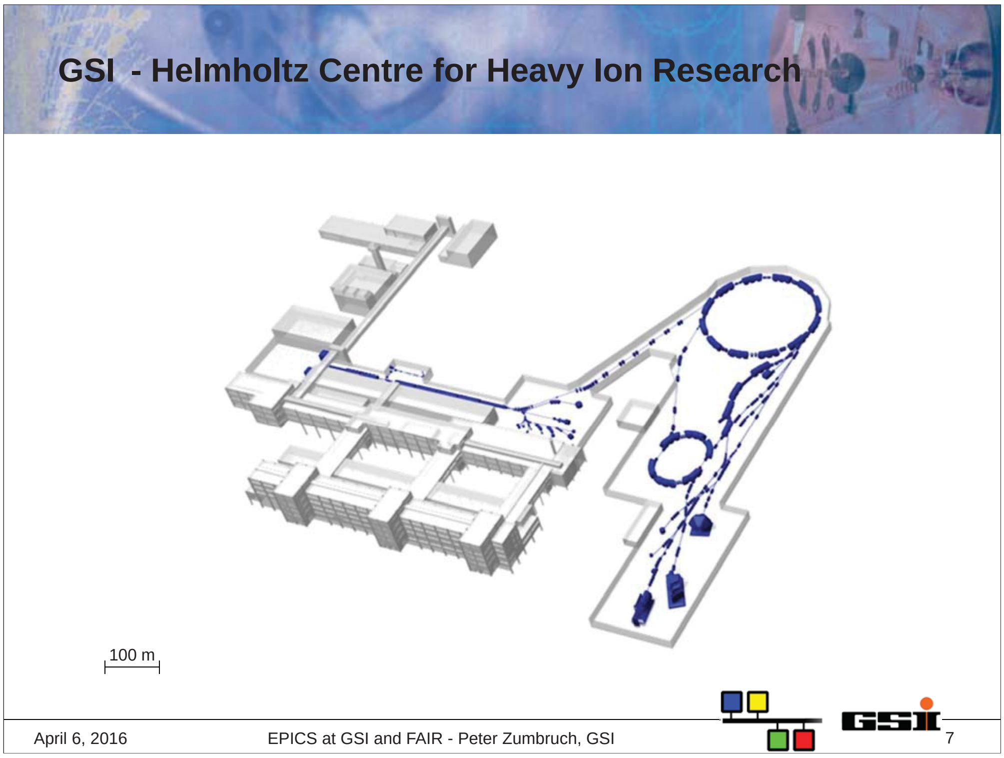
A Control System Architecture

Network-based "client/server" model (hence the EPICS logo)

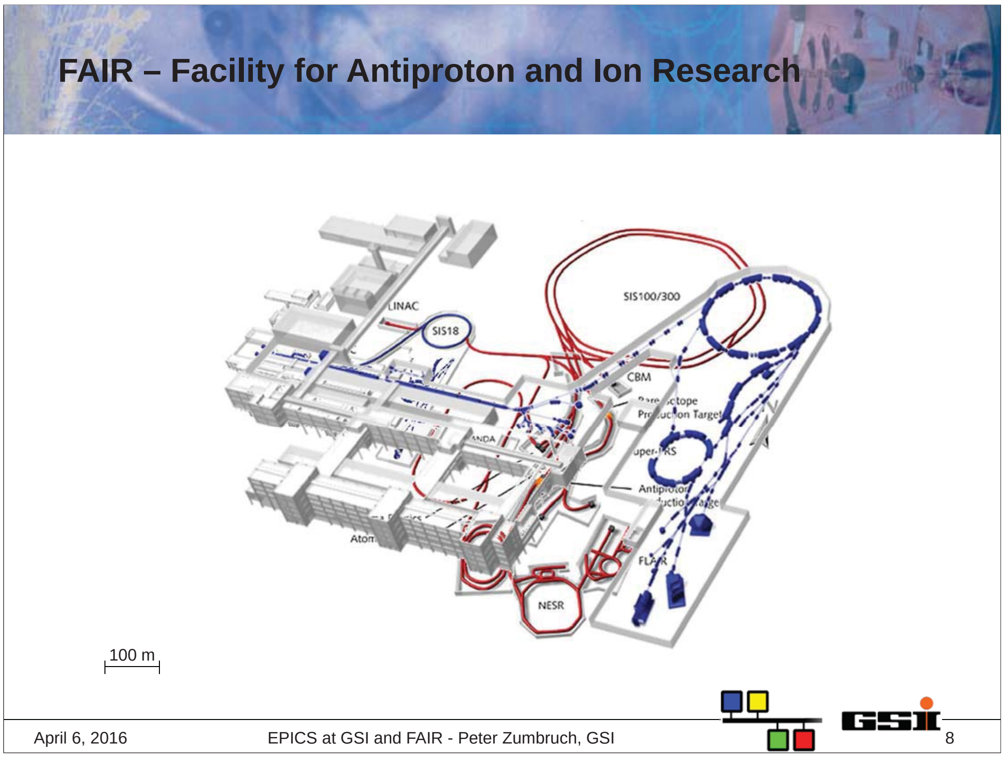
For EPICS, *client* and *server* speak of their Channel Access role

i.e. Channel Access Client & Channel Access Server

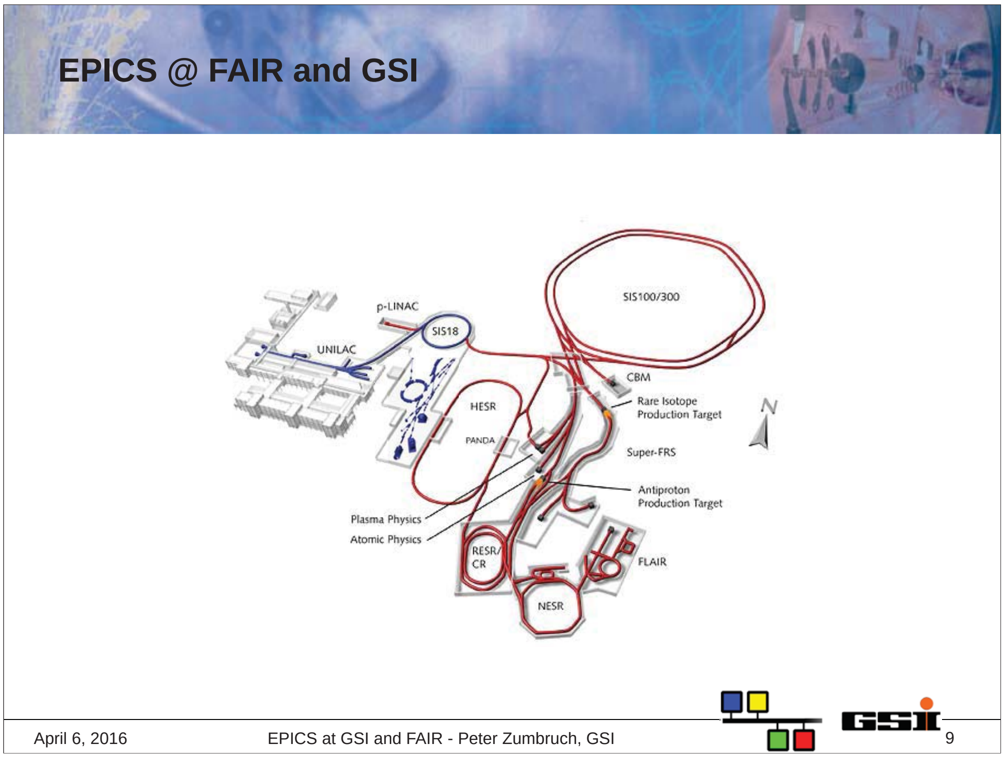
EPICS AT FAIR AND GSI EXPERIMENTS



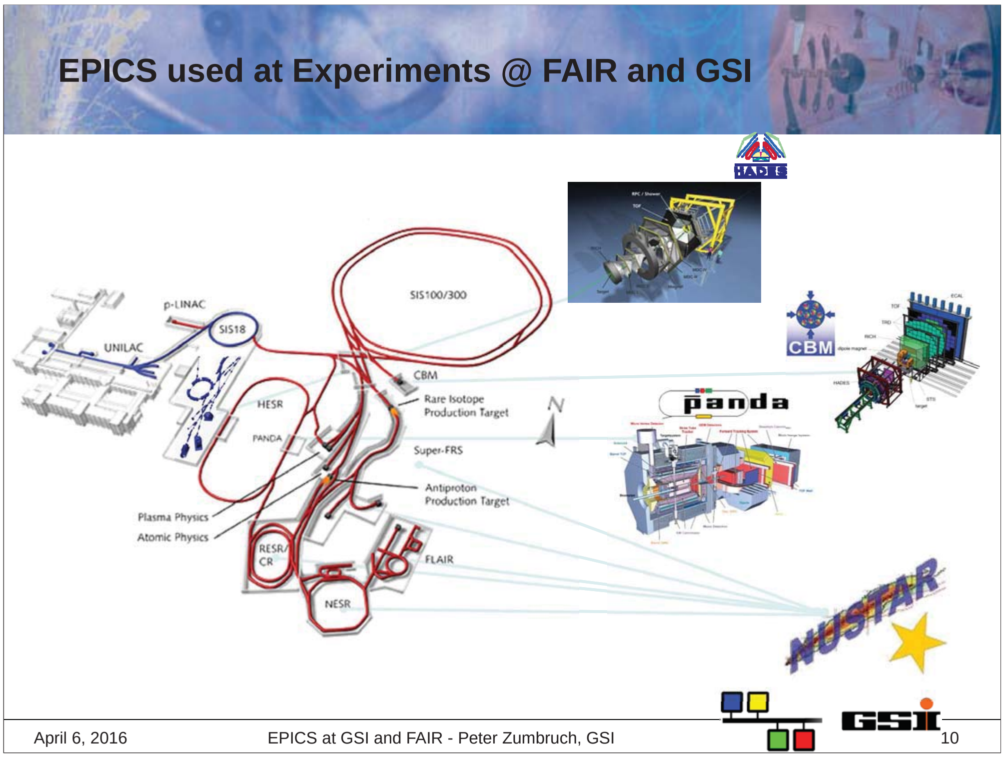
GSI - Helmholtz Centre for Heavy Ion Research



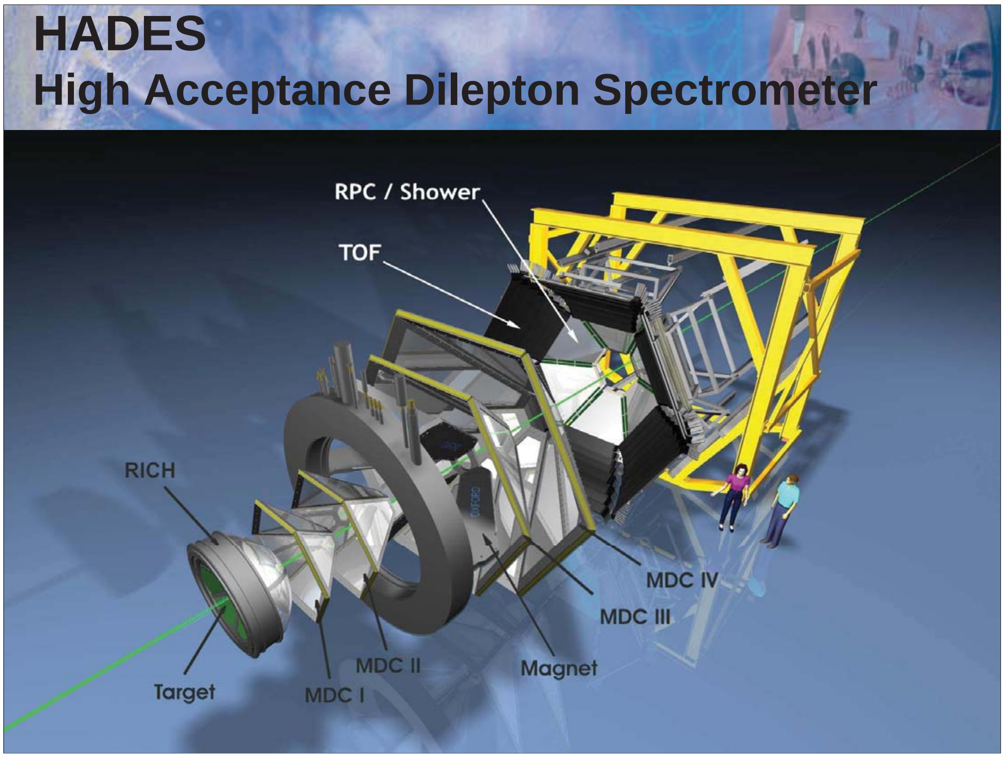
FAIR – Facility for Antiproton and Ion Research



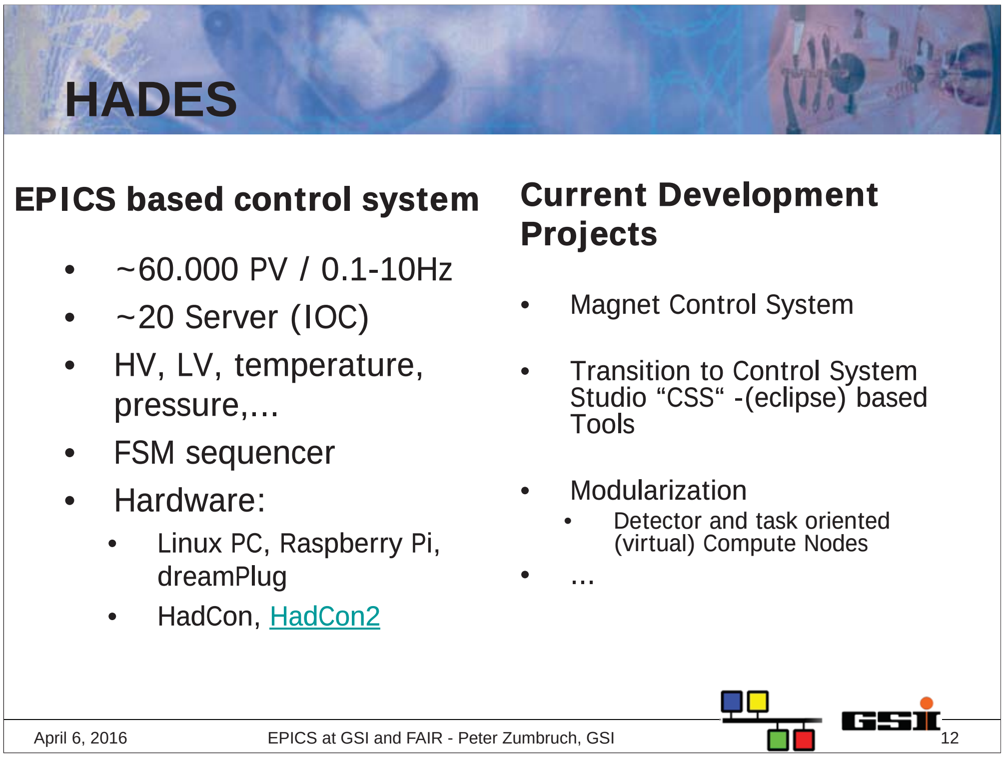
EPICS @ FAIR and GSI



EPICS used at Experiments @ FAIR and GSI



HADES
High Acceptance Dilepton Spectrometer



HADES

EPICS based control system

- ~60.000 PV / 0.1-10Hz
- ~20 Server (IOC)
- HV, LV, temperature, pressure,…
- FSM sequencer
- Hardware:
  - Linux PC, Raspberry Pi, dreamPlug
  - HadCon, HadCon2

Current Development Projects

- Magnet Control System
- Transition to Control System Studio “CSS“ -(eclipse) based Tools
- Modularization
  - Detector and task oriented (virtual) Compute Nodes
- …

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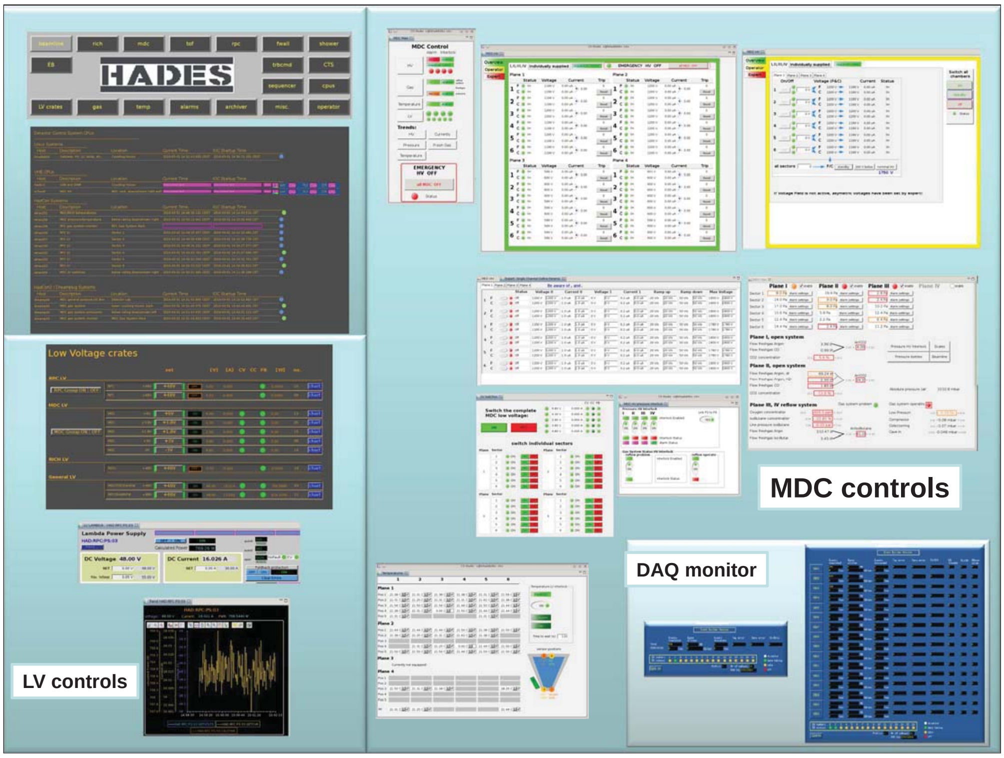


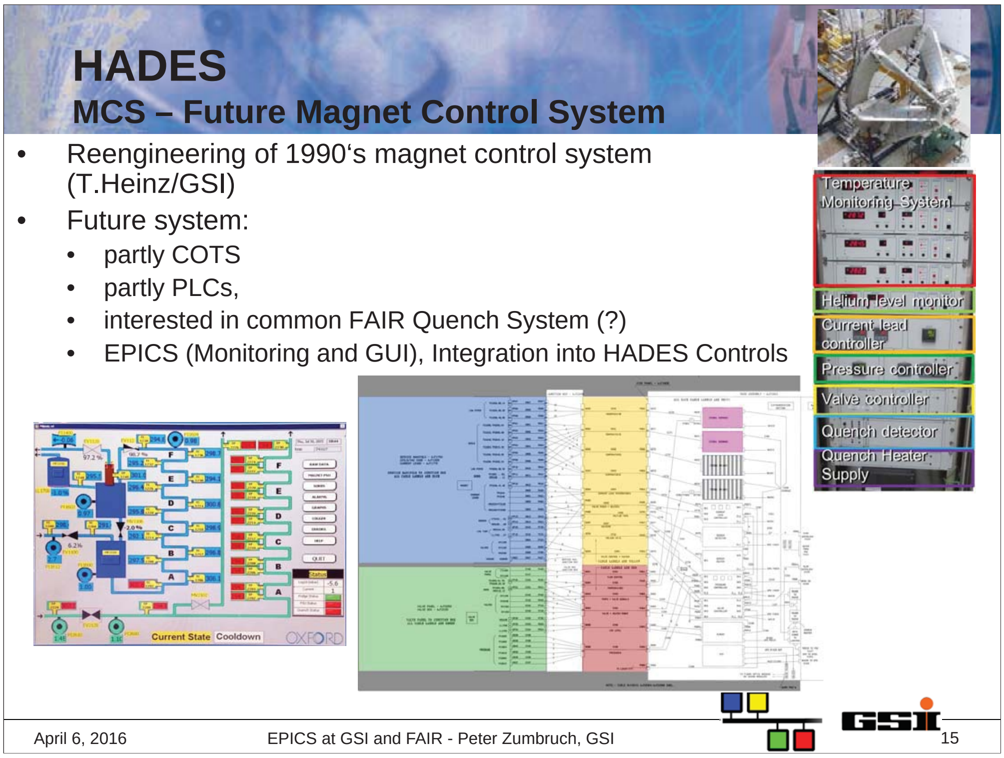
complementary DAQ controls

```
Other-HV Sequencer (15:16:14): Severe Error
HAD:TOFHV:G1 stopped, HAD:TOFHV:G2 stopped, HAD:TOFHV:G3 stopped,
HAD:TOFHV:G4 stopped, HAD:TOFHV:G5 stopped, HAD:TOFHV:G6 stopped,
HAD:RPCHV:G8 stopped, HAD:RPCHV:G9 stopped, HAD:RICH:HV:G25 stopped,
HAD:SHWR:HV:G26 stopped, HAD:SHWR:HV:G27 stopped, HAD:SHWR:HV:G28 stopped,
HAD:SHWR:HV:G29 stopped, HAD:SHWR:HV:G30 stopped, HAD:SHWR:HV:G31 stopped.
```

tactical overview

guide

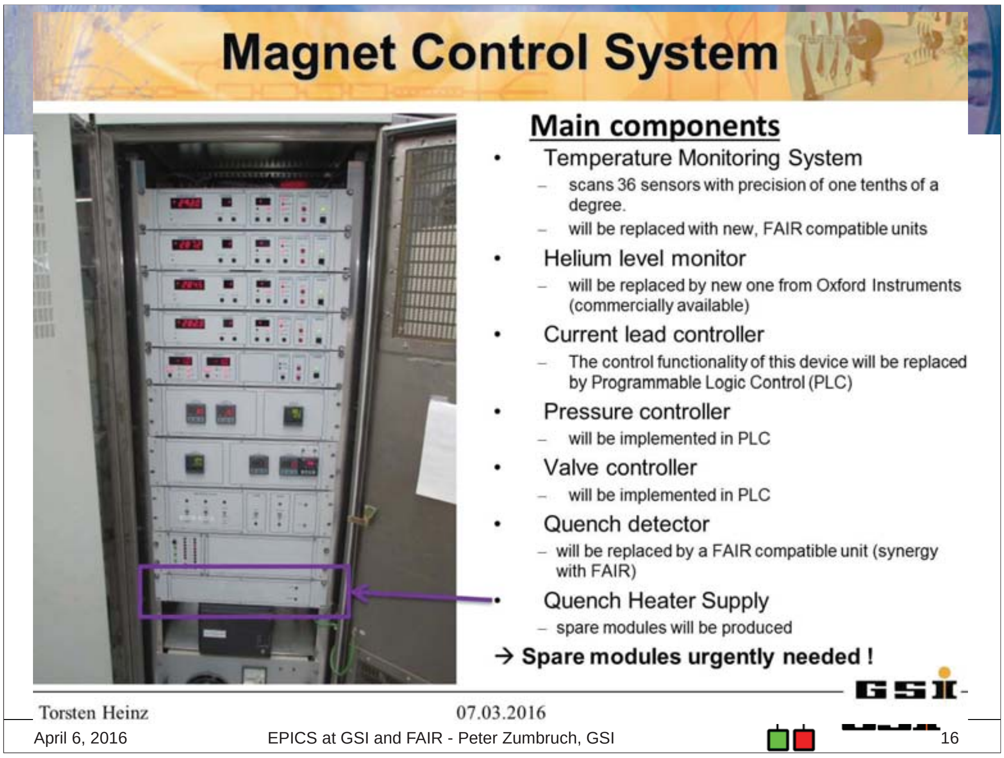
- Perl based
- Accessable via Web
- accesses EPICS data and DAQ “trbnet“ sources
- custom „hand-made“ J.Michel, IKF



HADES

MCS – Future Magnet Control System

- Reengineering of 1990‘s magnet control system (T.Heinz/GSI)
- Future system:
  - partly COTS
  - partly PLCs,
  - interested in common FAIR Quench System (?)
  - EPICS (Monitoring and GUI), Integration into HADES Controls



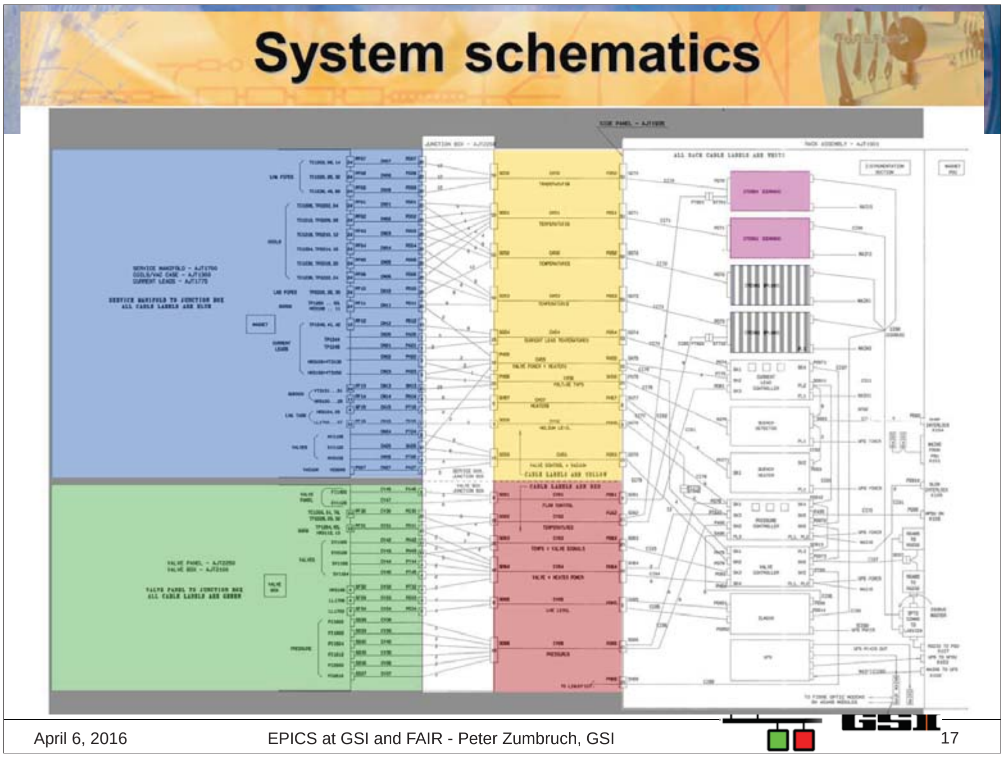
Magnet Control System

Main components

- Temperature Monitoring System
  - scans 36 sensors with precision of one tenths of a degree.
  - will be replaced with new, FAIR compatible units
- Helium level monitor
  - will be replaced by new one from Oxford Instruments (commercially available)
- Current lead controller
  - The control functionality of this device will be replaced by Programmable Logic Control (PLC)
- Pressure controller
  - will be implemented in PLC
- Valve controller
  - will be implemented in PLC
- Quench detector
  - will be replaced by a FAIR compatible unit (synergy with FAIR)
- Quench Heater Supply
  - spare modules will be produced

→ **Spare modules urgently needed !**

Torsten Heinz 07.03.2016



System schematics

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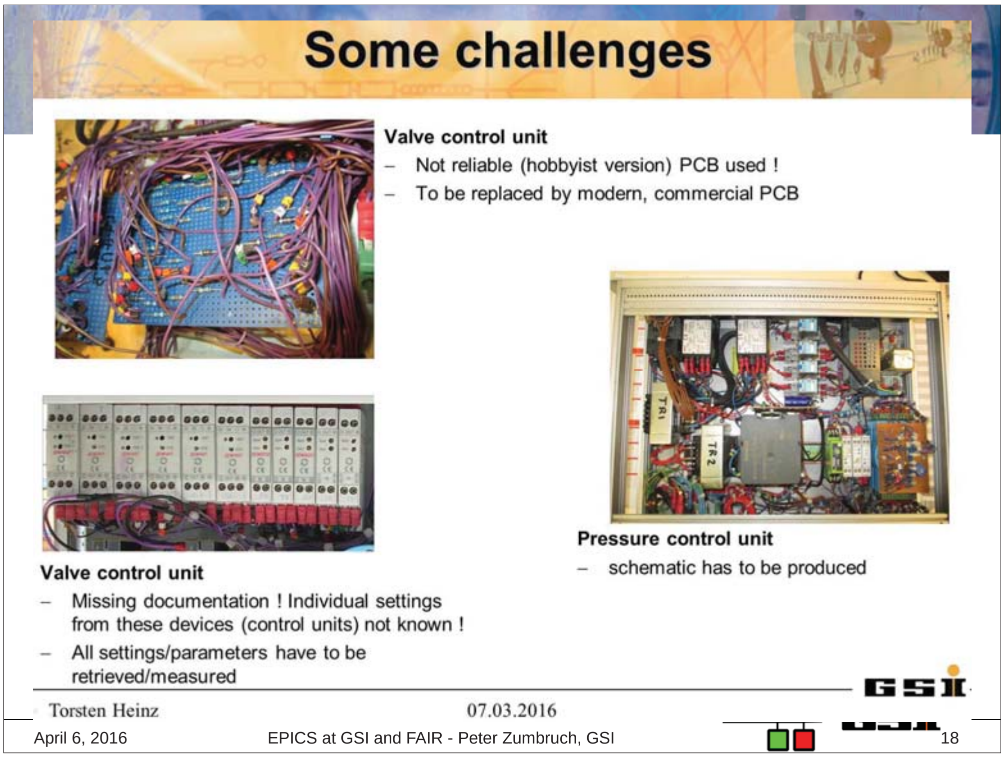

Some challenges

Valve control unit
- Not reliable (hobbyist version) PCB used !
- To be replaced by modern, commercial PCB

Valve control unit
- Missing documentation ! Individual settings from these devices (control units) not known !
- All settings/parameters have to be retrieved/measured

Pressure control unit
- schematic has to be produced

Torsten Heinz 07.03.2016

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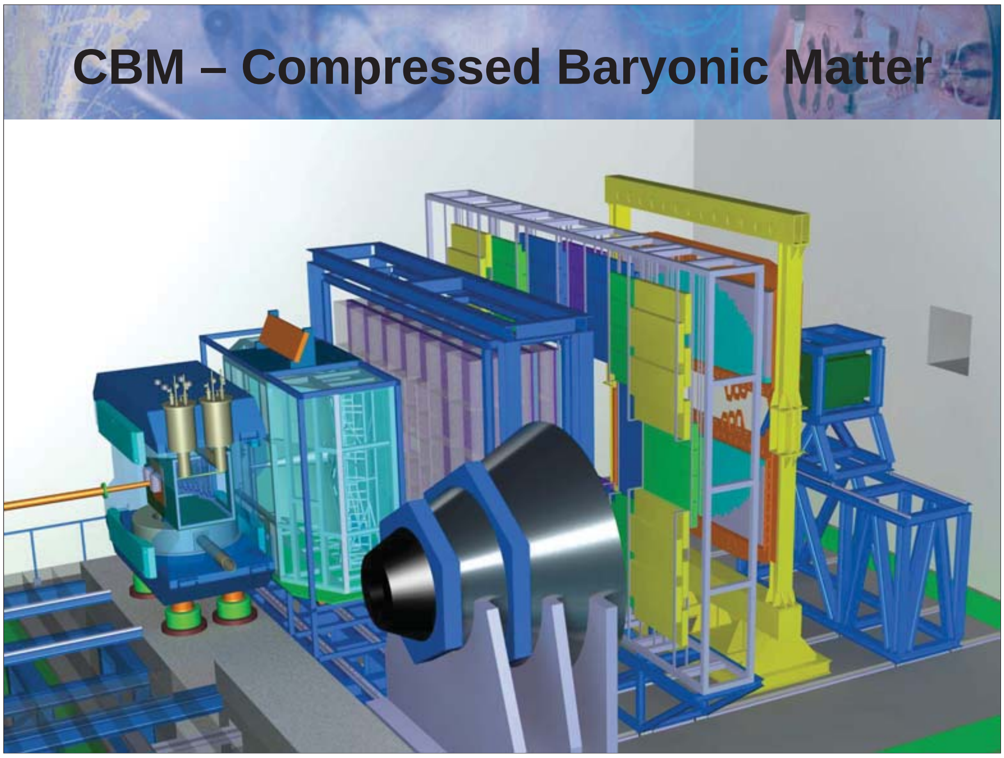
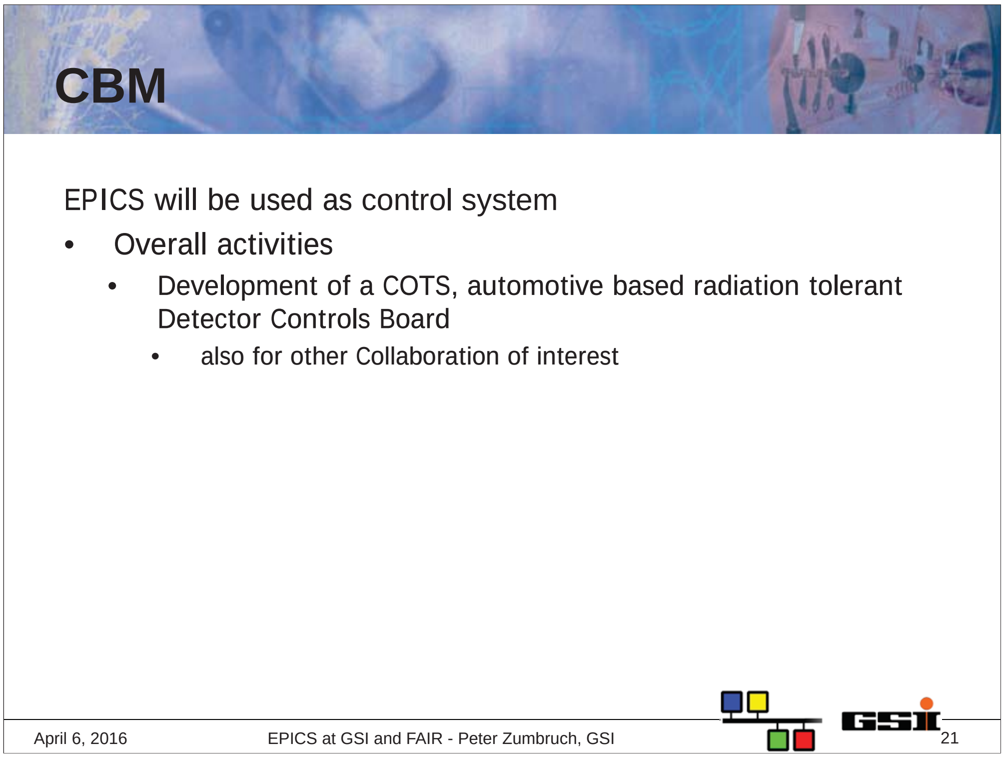


CBM – Compressed Baryonic Matter

CBM

EPICS will be used as control system

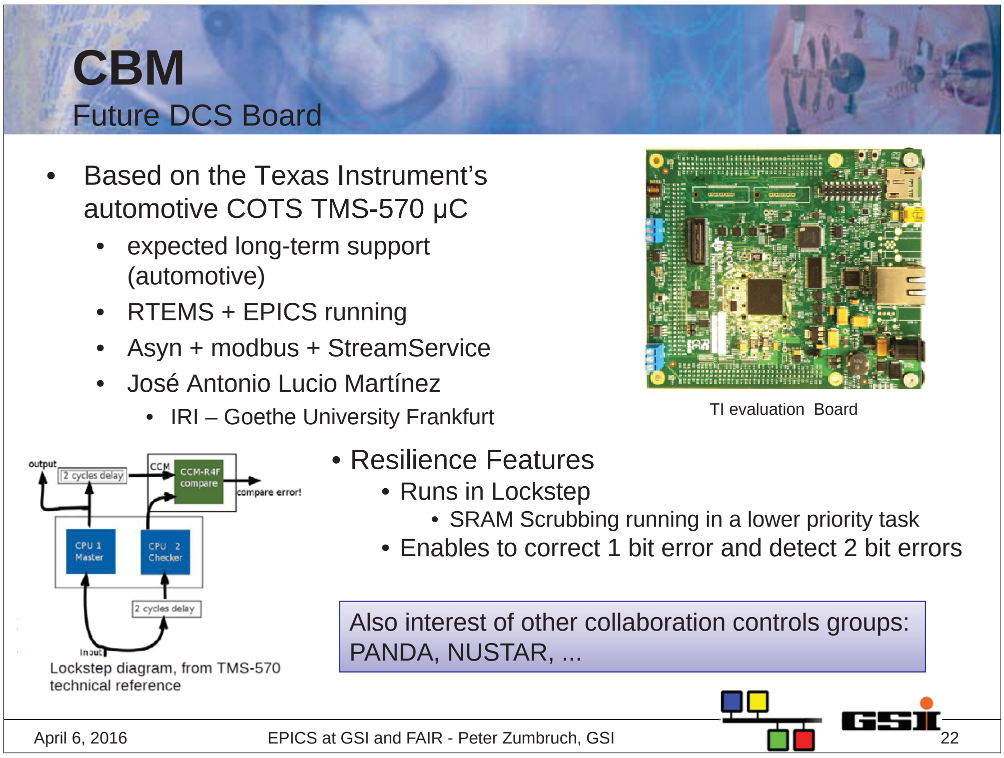
- Detector oriented activities
  - STS:
    - EPICS controlled detector setups for test beamtimes
      - Motion, T, LV, HV, Humidity
    - Laser Test Stand, x-y quality scanning
  - RICH:
    - Mirror Rotation System, HV, LV,
    - MAPMT Laser Test Stand, x-y quality scanning
  - TOF
    - kick-off for EPICS controlled detector setup for STAR participation



CBM

EPICS will be used as control system

- Overall activities
  - Development of a COTS, automotive based radiation tolerant Detector Controls Board
    - also for other Collaboration of interest



CBM

Future DCS Board

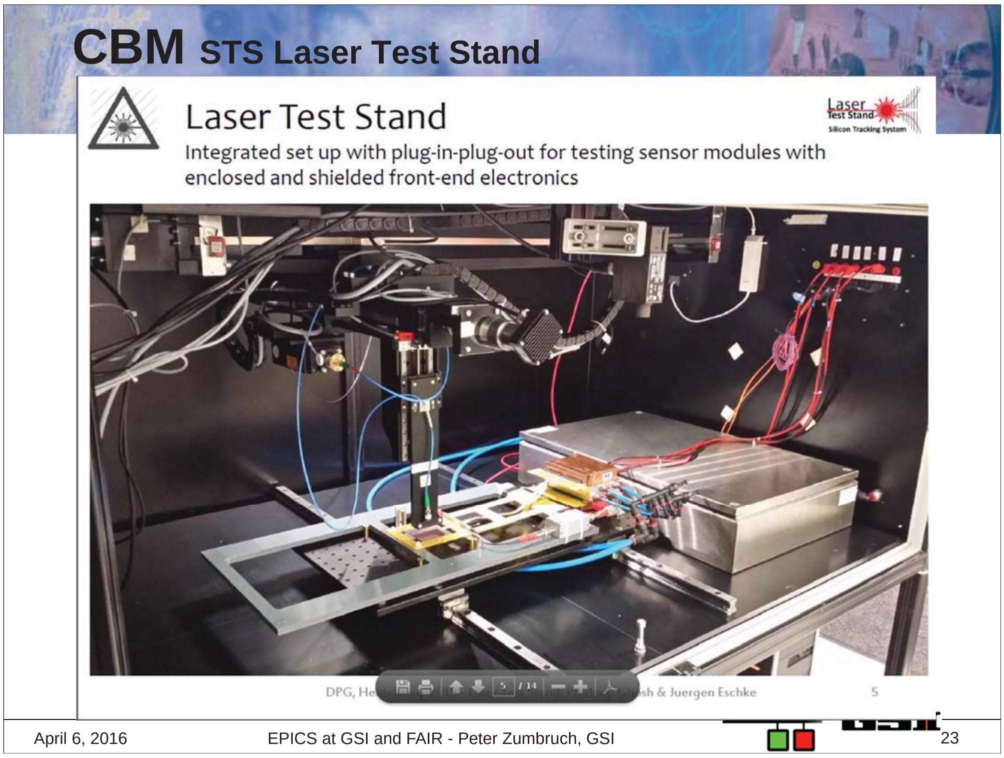
- Based on the Texas Instrument's automotive COTS TMS-570 µC
  - expected long-term support (automotive)
  - RTEMS + EPICS running
  - Asyn + modbus + StreamService
  - José Antonio Lucio Martínez
    - IRI – Goethe University Frankfurt

TI evaluation Board

Lockstep diagram, from TMS-570 technical reference

- Resilience Features
  - Runs in Lockstep
    - SRAM Scrubbing running in a lower priority task
  - Enables to correct 1 bit error and detect 2 bit errors

Also interest of other collaboration controls groups: PANDA, NUSTAR, ...



CBM STS Laser Test Stand

Laser Test Stand

Integrated set up with plug-in-plug-out for testing sensor modules with enclosed and shielded front-end electronics

DPG, He… …sh & Juergen Eschke 5

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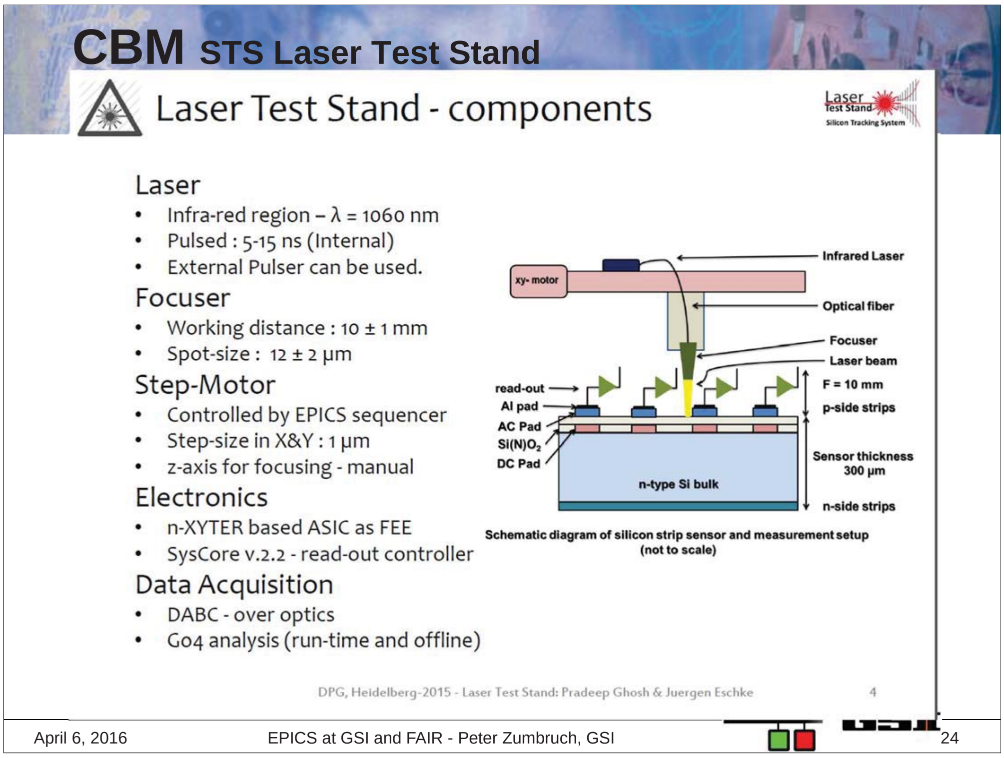

CBM STS Laser Test Stand

Laser Test Stand - components

Laser
- Infra-red region – λ = 1060 nm
- Pulsed : 5-15 ns (Internal)
- External Pulser can be used.

Focuser
- Working distance : 10 ± 1 mm
- Spot-size : 12 ± 2 μm

Step-Motor
- Controlled by EPICS sequencer
- Step-size in X&Y : 1 μm
- z-axis for focusing - manual

Electronics
- n-XYTER based ASIC as FEE
- SysCore v.2.2 - read-out controller

Data Acquisition
- DABC - over optics
- Go4 analysis (run-time and offline)

Schematic diagram of silicon strip sensor and measurement setup (not to scale)

DPG, Heidelberg-2015 - Laser Test Stand: Pradeep Ghosh & Juergen Eschke 4

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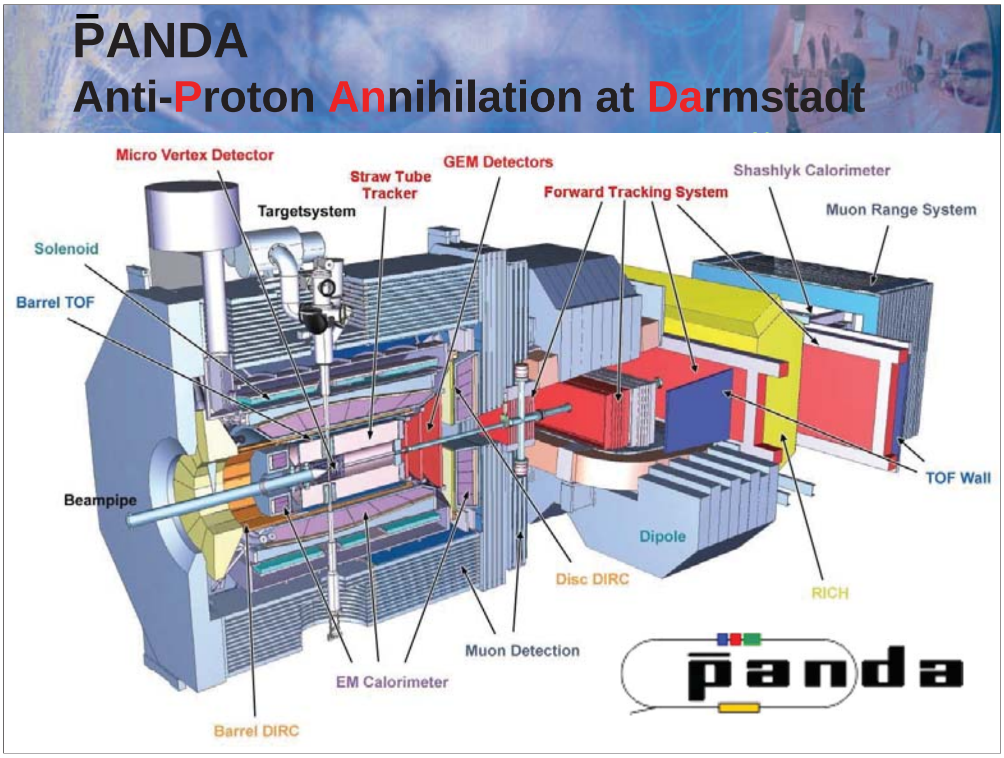
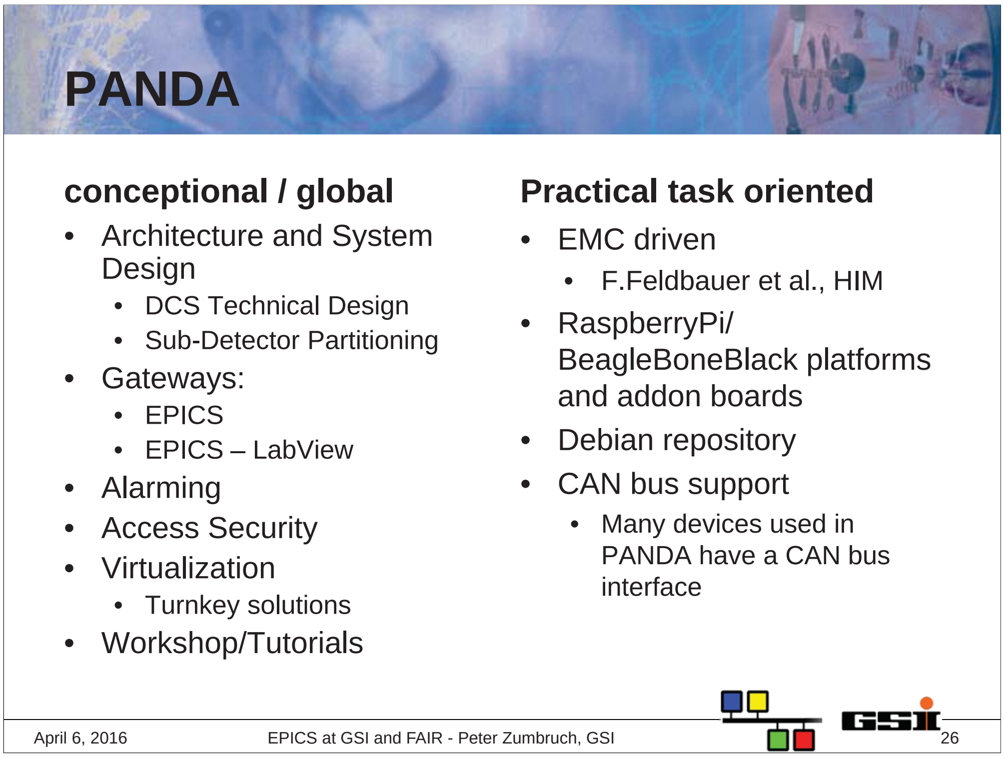


P̄ANDA
Anti-Proton Annihilation at Darmstadt



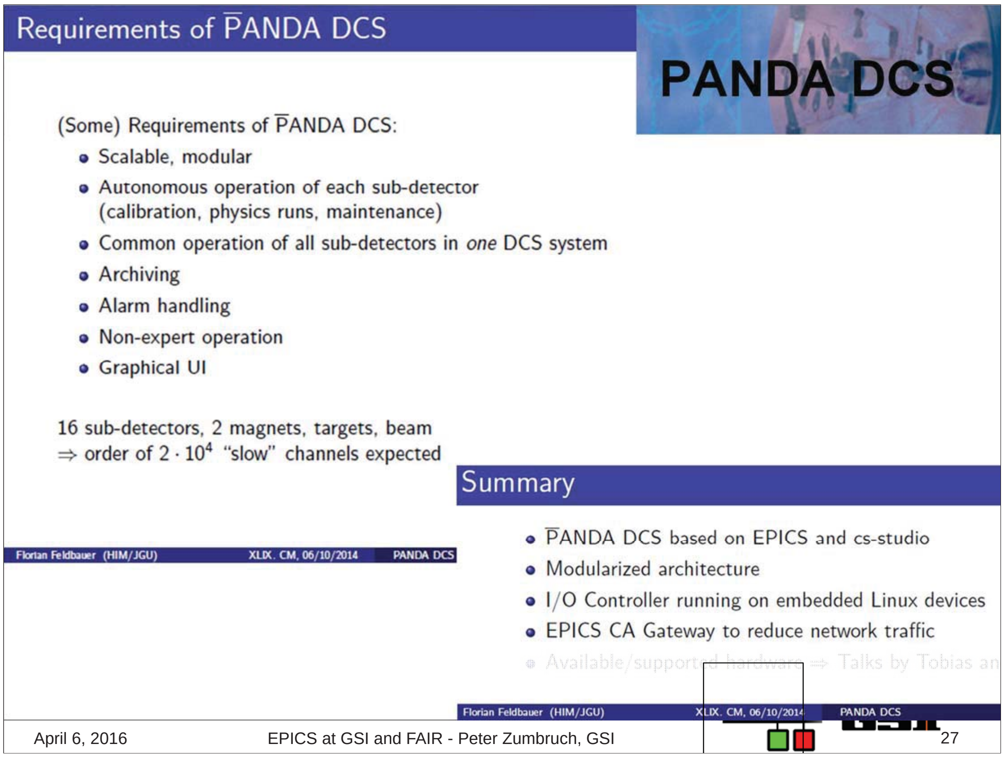
PANDA

conceptional / global

- Architecture and System Design
  - DCS Technical Design
  - Sub-Detector Partitioning
- Gateways:
  - EPICS
  - EPICS – LabView
- Alarming
- Access Security
- Virtualization
  - Turnkey solutions
- Workshop/Tutorials

Practical task oriented

- EMC driven
  - F.Feldbauer et al., HIM
- RaspberryPi/ BeagleBoneBlack platforms and addon boards
- Debian repository
- CAN bus support
  - Many devices used in PANDA have a CAN bus interface



Requirements of $\overline{\text{P}}$ANDA DCS

(Some) Requirements of $\overline{\text{P}}$ANDA DCS:

- Scalable, modular
- Autonomous operation of each sub-detector (calibration, physics runs, maintenance)
- Common operation of all sub-detectors in *one* DCS system
- Archiving
- Alarm handling
- Non-expert operation
- Graphical UI

16 sub-detectors, 2 magnets, targets, beam
⇒ order of $2 \cdot 10^4$ “slow” channels expected

Florian Feldbauer (HIM/JGU) XLIX. CM, 06/10/2014 PANDA DCS

Summary

- $\overline{\text{P}}$ANDA DCS based on EPICS and cs-studio
- Modularized architecture
- I/O Controller running on embedded Linux devices
- EPICS CA Gateway to reduce network traffic
- Available/supported hardware ⇒ Talks by Tobias an

Florian Feldbauer (HIM/JGU) XLIX. CM, 06/10/2014 PANDA DCS

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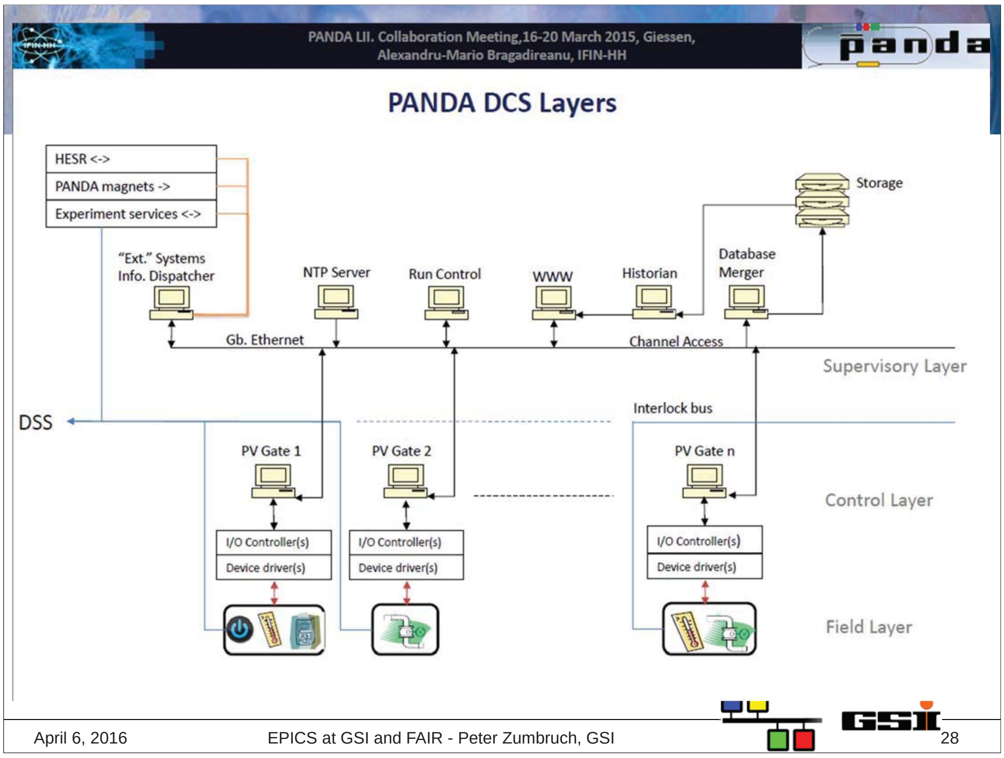

PANDA LII. Collaboration Meeting,16-20 March 2015, Giessen,
Alexandru-Mario Bragadireanu, IFIN-HH

PANDA DCS Layers

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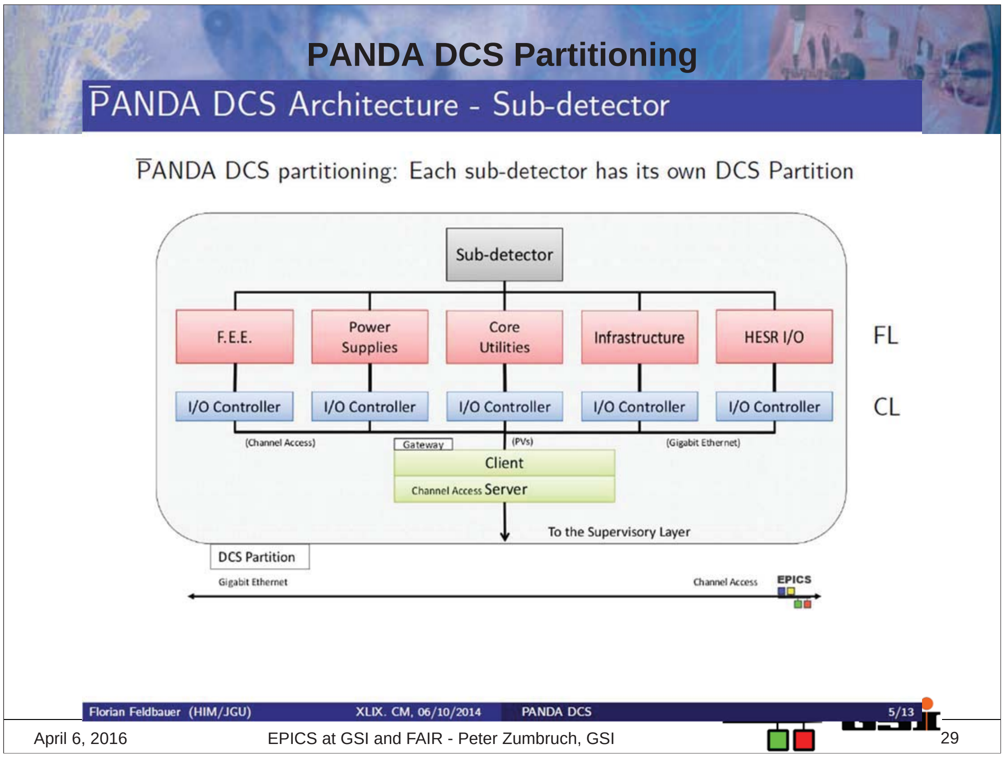


PANDA DCS Partitioning

P̄ANDA DCS Architecture - Sub-detector

P̄ANDA DCS partitioning: Each sub-detector has its own DCS Partition

Sub-detector

F.E.E. | Power Supplies | Core Utilities | Infrastructure | HESR I/O — FL

I/O Controller | I/O Controller | I/O Controller | I/O Controller | I/O Controller — CL

(Channel Access) Gateway (PVs) (Gigabit Ethernet)

Client

Channel Access Server

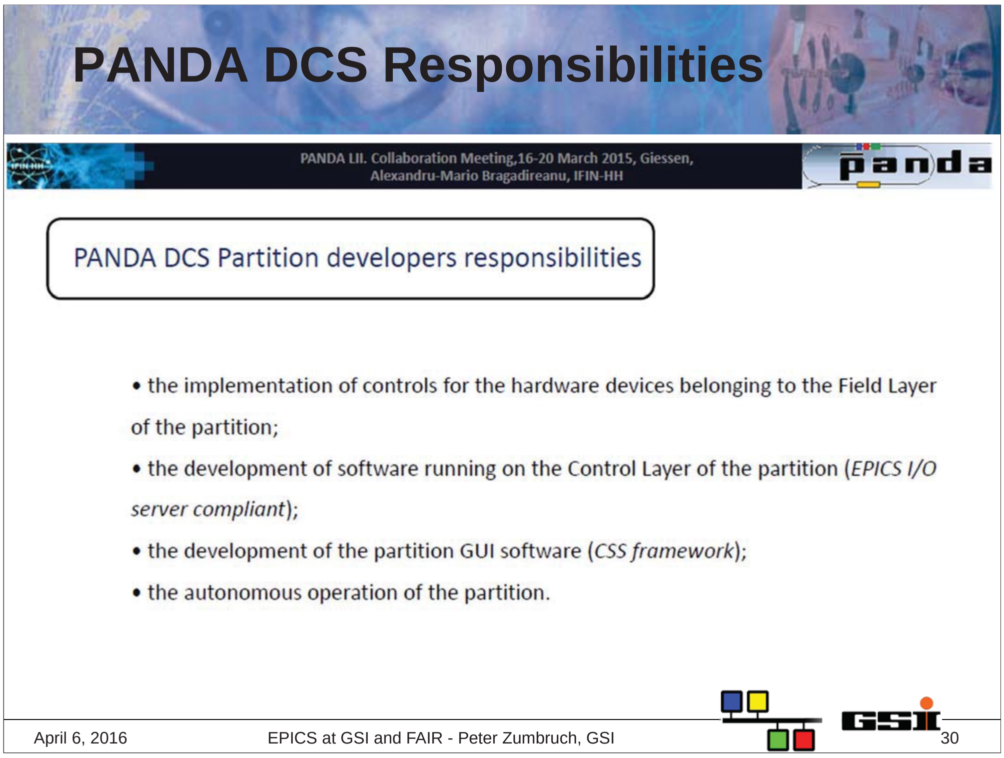
To the Supervisory Layer

DCS Partition

Gigabit Ethernet — Channel Access — EPICS

Florian Feldbauer (HIM/JGU) XLIX. CM, 06/10/2014 PANDA DCS 5/13

April 6, 2016 EPICS at GSI and FAIR - Peter Zumbruch, GSI 29



PANDA DCS Responsibilities

PANDA LII. Collaboration Meeting,16-20 March 2015, Giessen,
Alexandru-Mario Bragadireanu, IFIN-HH

PANDA DCS Partition developers responsibilities

- the implementation of controls for the hardware devices belonging to the Field Layer of the partition;
- the development of software running on the Control Layer of the partition (*EPICS I/O server compliant*);
- the development of the partition GUI software (*CSS framework*);
- the autonomous operation of the partition.

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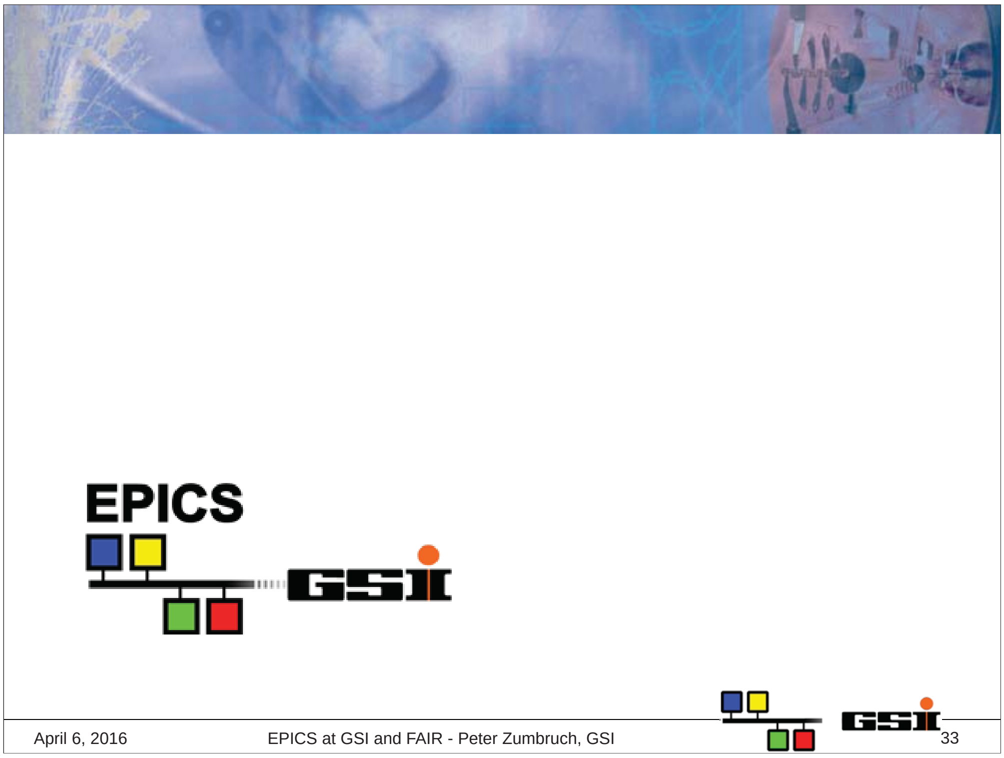
NUSTAR

NUclear STructure, Astrophysics and Reactions

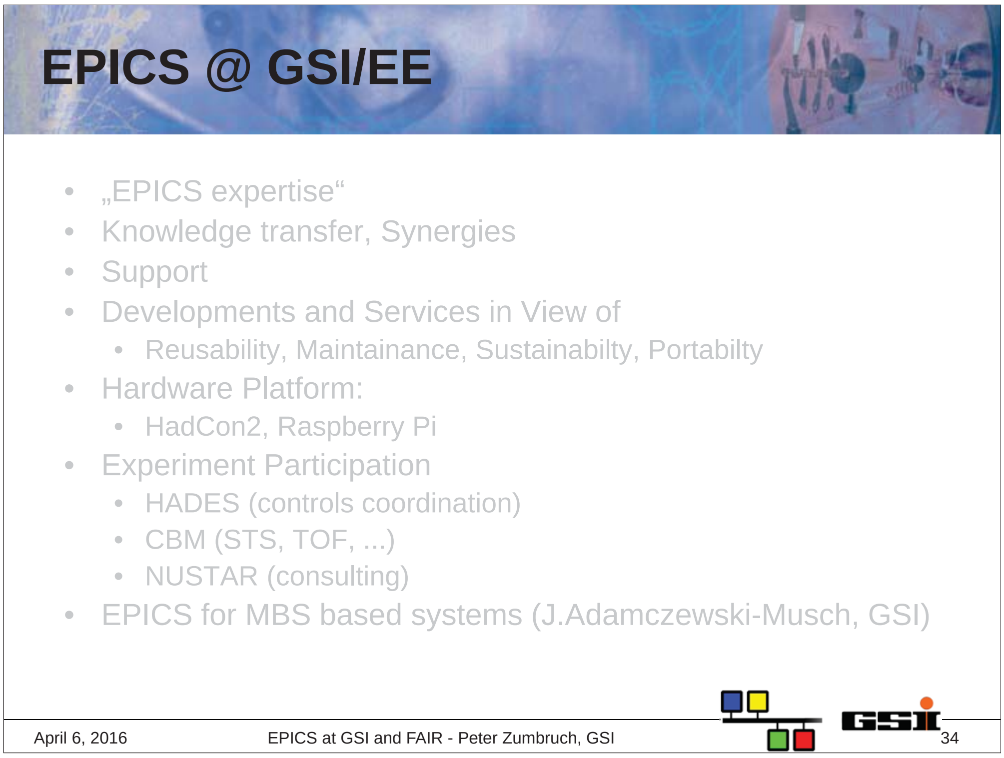
NUSTAR

Common Agreement:
EPICS as supervisory control system for several Experiments

Several EPICS applications:
- often standalone, single developments
- Gamma-Spectroscopy:
  - BeagleBoneBlack and HadCon2 based control of I2C DACs to drive HV supply close to FEE
- Gas Mixing Station
- Magnet Control
  - HadCon based Control of retired ALADIN Magnet
  - planned GLAD Magnet Control
    - requires interface to Accelerator Control System
- Threshold, Multiplexer settings
  - current LAND Tacquilla Electronic, 400 channels
  - in future new NeuLAND FQT / Tamex, 400 channels
- HV settings
  - LAND, 400 channels
  - NeuLAND, russian development, 6000 channels
- Motion control, slit system “ROLU“ („Rechts, Oben, Links, Unten“)
- Gas scales



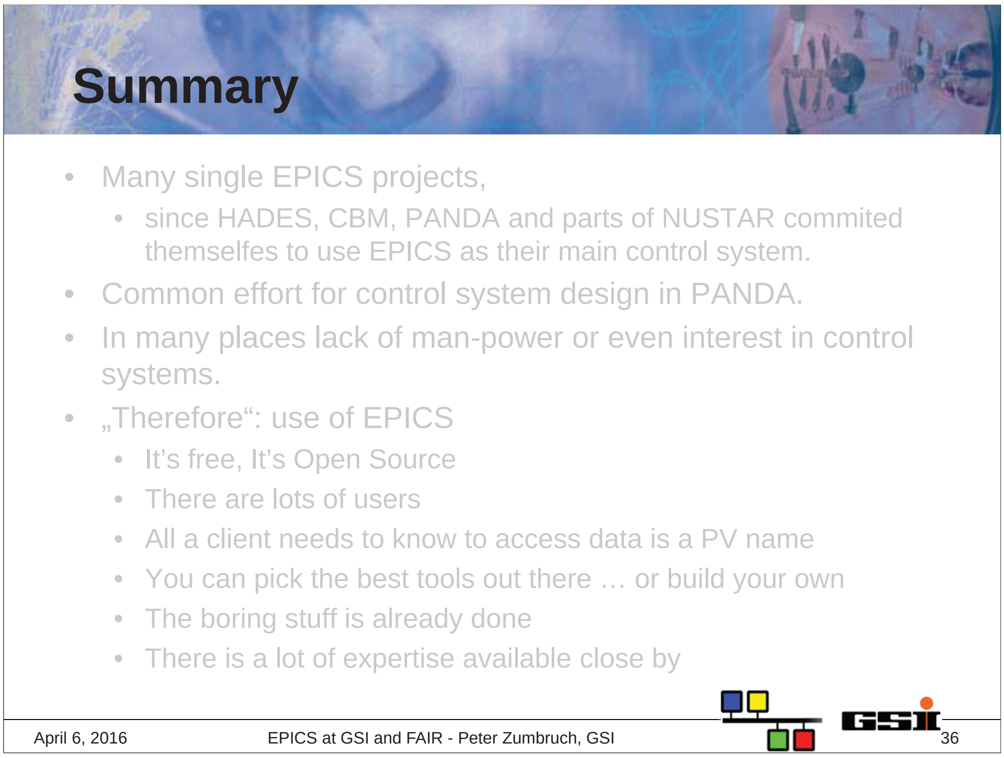
EPICS



EPICS @ GSI/EE

- „EPICS expertise“
- Knowledge transfer, Synergies
- Support
- Developments and Services in View of
  - Reusability, Maintainance, Sustainabilty, Portabilty
- Hardware Platform:
  - HadCon2, Raspberry Pi
- Experiment Participation
  - HADES (controls coordination)
  - CBM (STS, TOF, ...)
  - NUSTAR (consulting)
- EPICS for MBS based systems (J.Adamczewski-Musch, GSI)

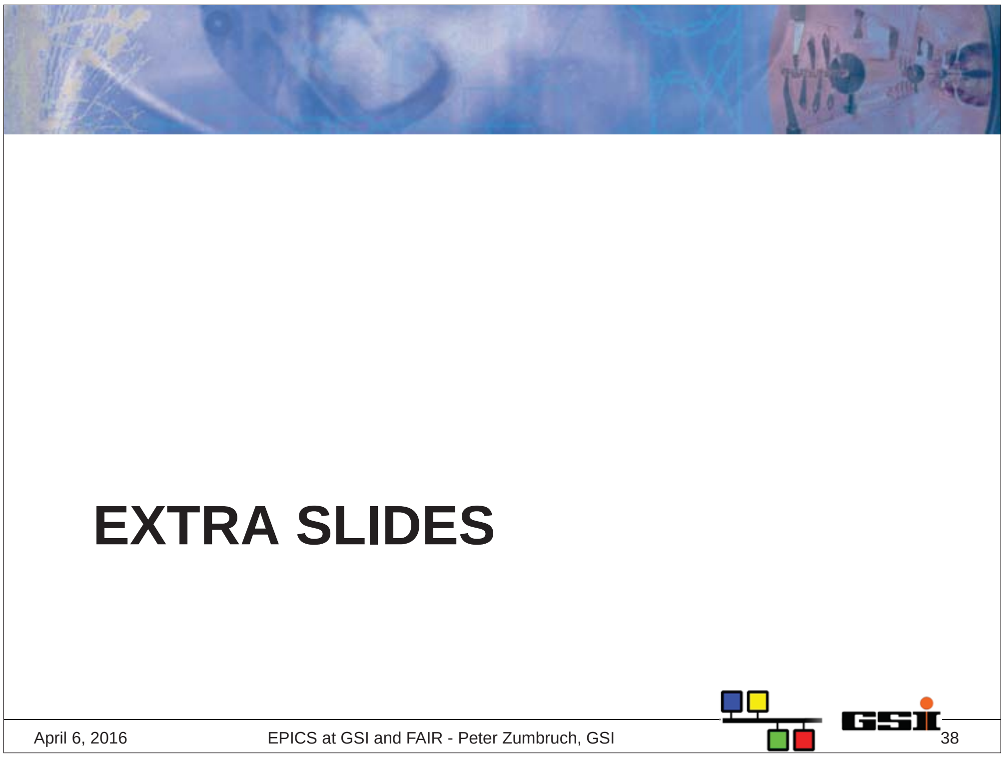
SUMMARY



Summary

- Many single EPICS projects,
  - since HADES, CBM, PANDA and parts of NUSTAR commited themselfes to use EPICS as their main control system.
- Common effort for control system design in PANDA.
- In many places lack of man-power or even interest in control systems.
- „Therefore“: use of EPICS
  - It’s free, It’s Open Source
  - There are lots of users
  - All a client needs to know to access data is a PV name
  - You can pick the best tools out there … or build your own
  - The boring stuff is already done
  - There is a lot of expertise available close by

THANK YOU.



EXTRA SLIDES

HadCon2

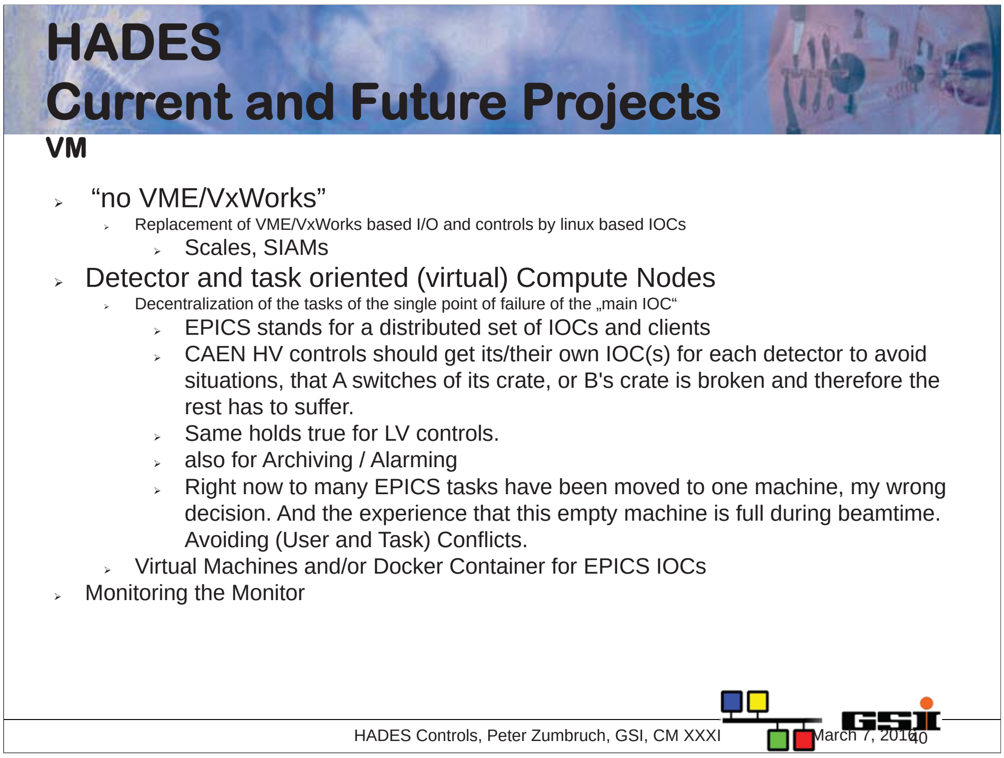
HadCon2 is a credit-card sized general purpose I/O module for detector and experiment controls as well as for small data acquisition systems.

https://wiki.gsi.de/EE/HadCon2

It is the successor of the discontinued first version HadCon (HADControl/HadShoPoMo general purpose board, HadCon @ Epics Wiki).

The module has an ATMEL AT90CAN128 microcontroller providing a multitude of connectivity:

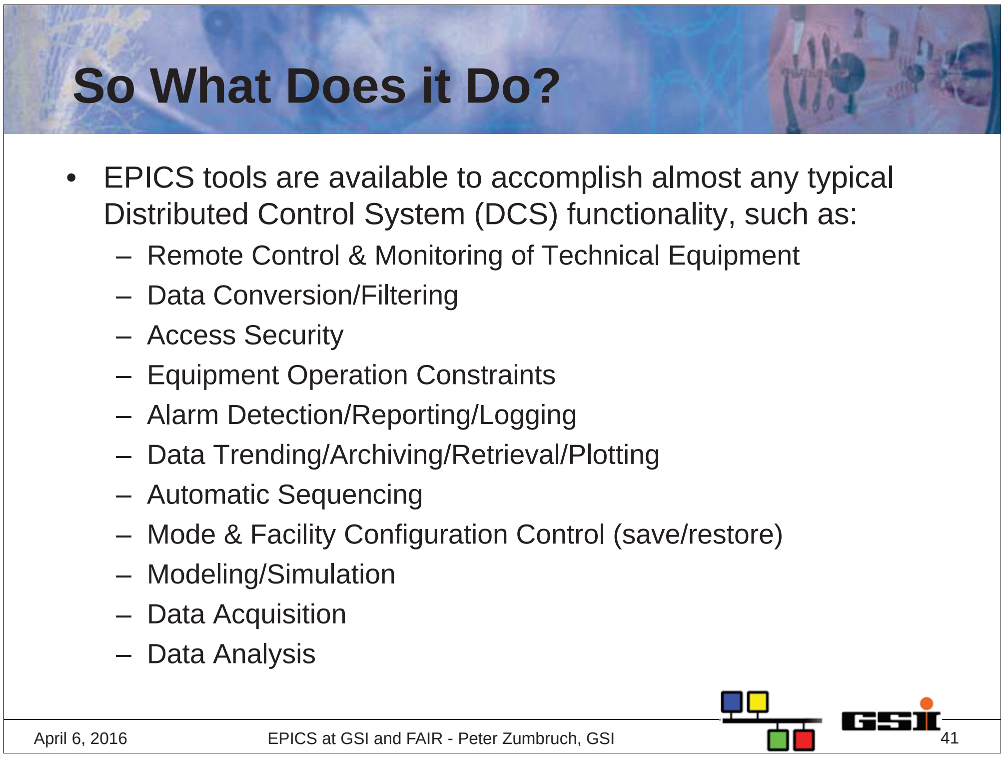
I^2C (8/4 fold (intern/extern) multiplexer), 6 channel 1-wire master, 8-channel 8bit DAC, galvanically isolated CAN - high-speed transceiver, 8-channel 10-bit SAR ADC, byte-oriented SPI, in total up-to 53 programmable I/O lines and optionally a Lattice MachX02 FPGA for fast data processing tasks.



HADES
Current and Future Projects

VM

- “no VME/VxWorks”
  - Replacement of VME/VxWorks based I/O and controls by linux based IOCs
    - Scales, SIAMs
- Detector and task oriented (virtual) Compute Nodes
  - Decentralization of the tasks of the single point of failure of the „main IOC“
    - EPICS stands for a distributed set of IOCs and clients
    - CAEN HV controls should get its/their own IOC(s) for each detector to avoid situations, that A switches of its crate, or B's crate is broken and therefore the rest has to suffer.
    - Same holds true for LV controls.
    - also for Archiving / Alarming
    - Right now to many EPICS tasks have been moved to one machine, my wrong decision. And the experience that this empty machine is full during beamtime. Avoiding (User and Task) Conflicts.
  - Virtual Machines and/or Docker Container for EPICS IOCs
- Monitoring the Monitor



So What Does it Do?

- EPICS tools are available to accomplish almost any typical Distributed Control System (DCS) functionality, such as:
  - Remote Control & Monitoring of Technical Equipment
  - Data Conversion/Filtering
  - Access Security
  - Equipment Operation Constraints
  - Alarm Detection/Reporting/Logging
  - Data Trending/Archiving/Retrieval/Plotting
  - Automatic Sequencing
  - Mode & Facility Configuration Control (save/restore)
  - Modeling/Simulation
  - Data Acquisition
  - Data Analysis

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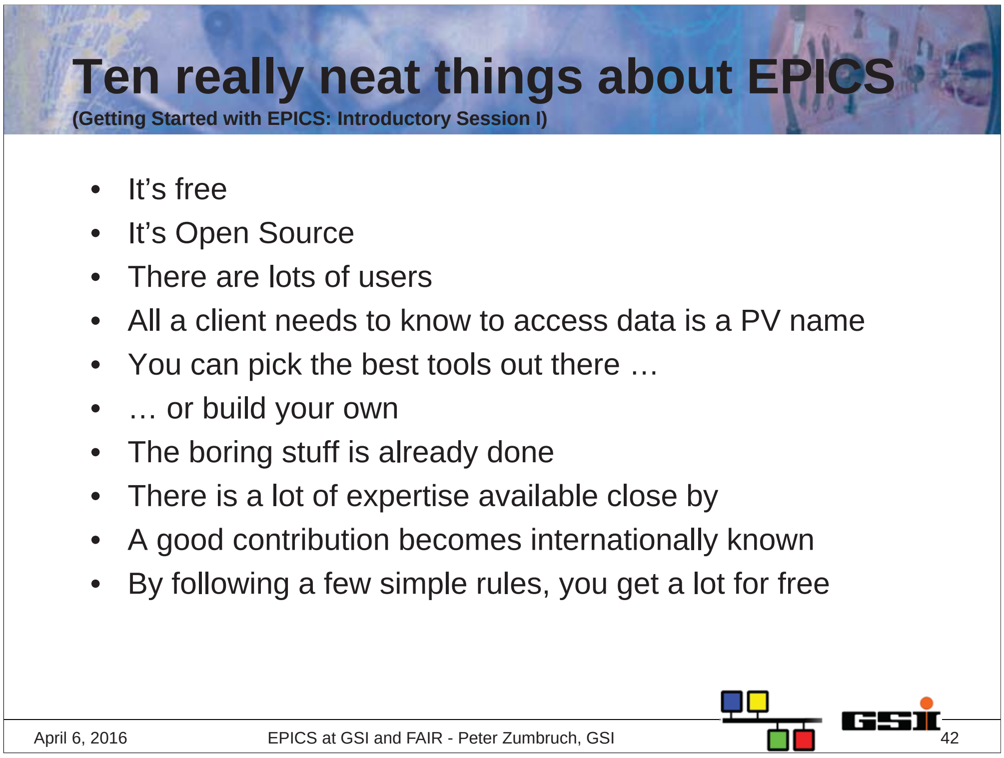

Ten really neat things about EPICS

(Getting Started with EPICS: Introductory Session I)

- It’s free
- It’s Open Source
- There are lots of users
- All a client needs to know to access data is a PV name
- You can pick the best tools out there …
- … or build your own
- The boring stuff is already done
- There is a lot of expertise available close by
- A good contribution becomes internationally known
- By following a few simple rules, you get a lot for free

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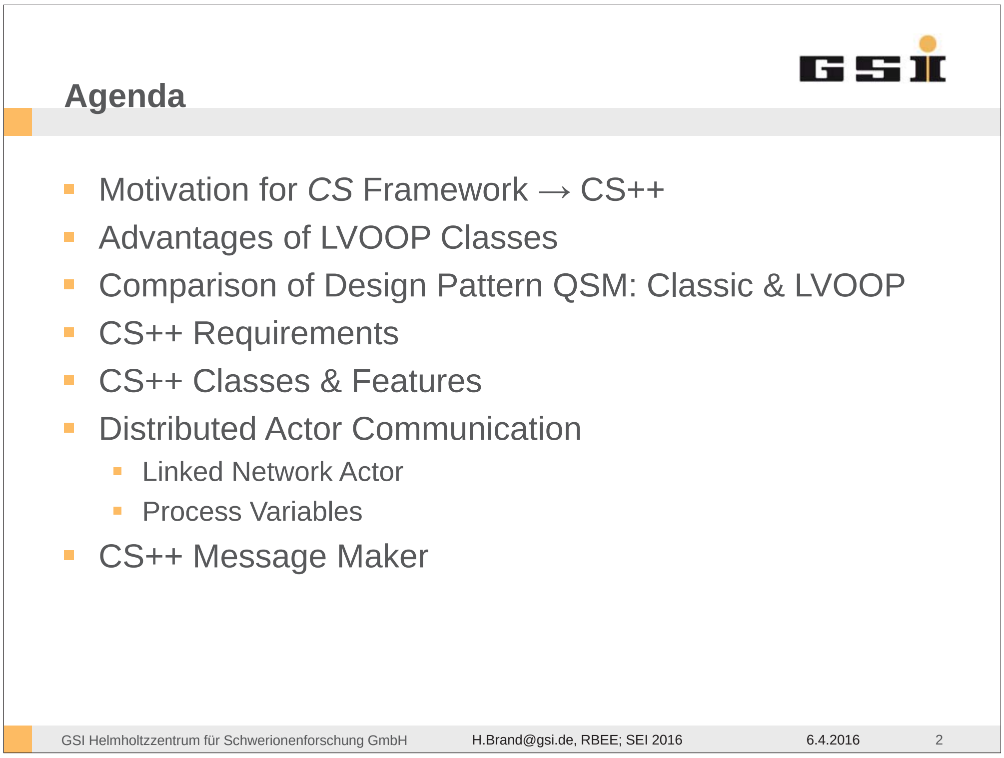
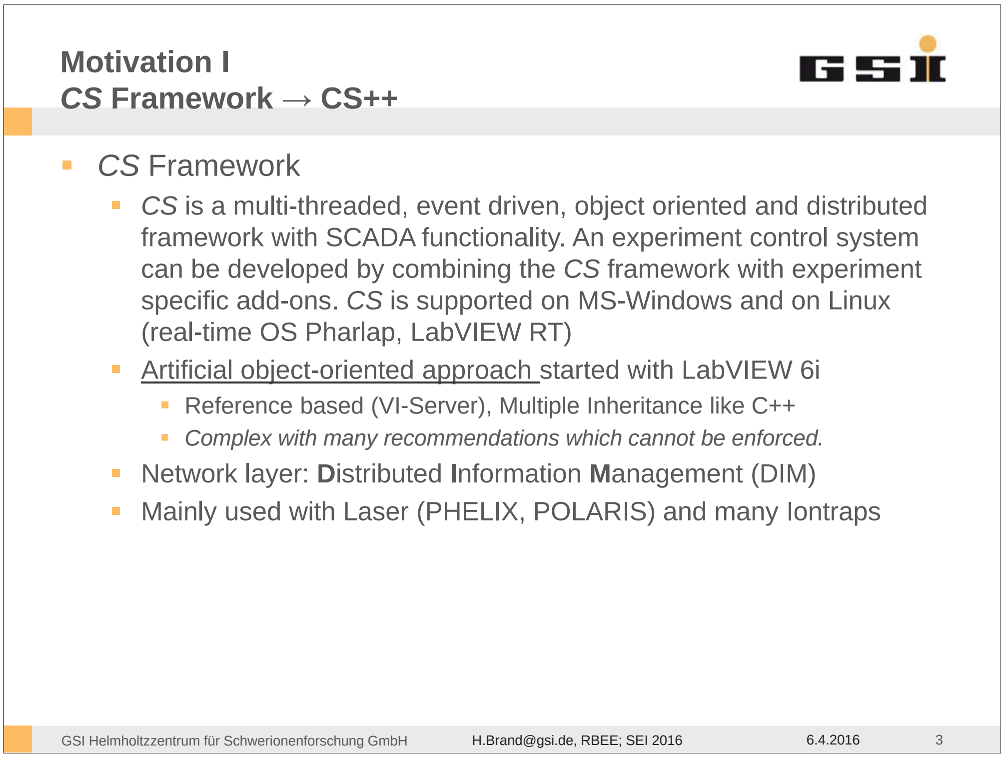
CS++ - The Actor based Successor of the *CS* Framework

Holger Brand, RBEE, GSI
Dennis Neidherr, RBEE, GSI



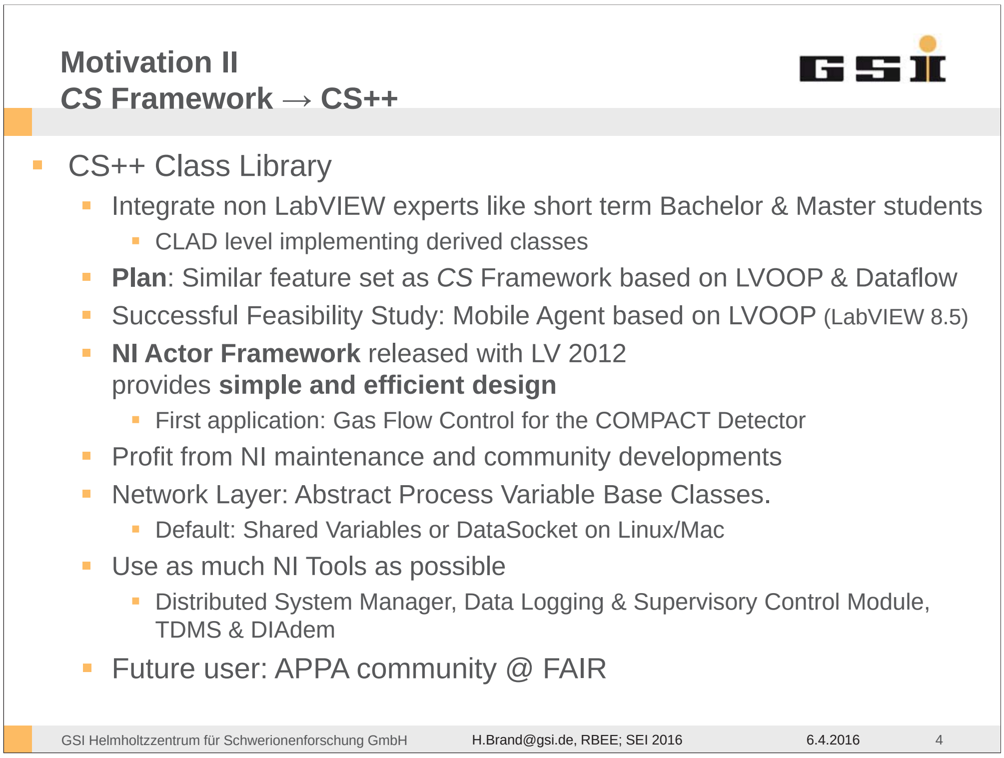
Agenda

- Motivation for *CS* Framework → CS++
- Advantages of LVOOP Classes
- Comparison of Design Pattern QSM: Classic & LVOOP
- CS++ Requirements
- CS++ Classes & Features
- Distributed Actor Communication
  - Linked Network Actor
  - Process Variables
- CS++ Message Maker



Motivation I
CS Framework → CS++

- *CS* Framework
  - *CS* is a multi-threaded, event driven, object oriented and distributed framework with SCADA functionality. An experiment control system can be developed by combining the *CS* framework with experiment specific add-ons. *CS* is supported on MS-Windows and on Linux (real-time OS Pharlap, LabVIEW RT)
  - Artificial object-oriented approach started with LabVIEW 6i
    - Reference based (VI-Server), Multiple Inheritance like C++
    - *Complex with many recommendations which cannot be enforced.*
  - Network layer: **D**istributed **I**nformation **M**anagement (DIM)
  - Mainly used with Laser (PHELIX, POLARIS) and many Iontraps



Motivation II
CS Framework → CS++

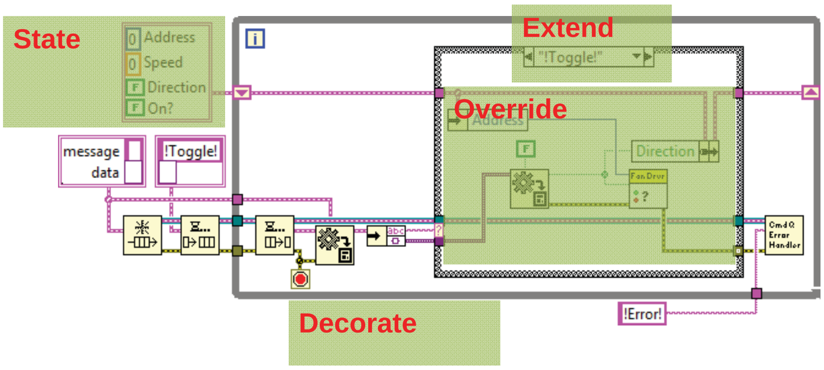
- CS++ Class Library
  - Integrate non LabVIEW experts like short term Bachelor & Master students
    - CLAD level implementing derived classes
  - **Plan**: Similar feature set as *CS* Framework based on LVOOP & Dataflow
  - Successful Feasibility Study: Mobile Agent based on LVOOP (LabVIEW 8.5)
  - **NI Actor Framework** released with LV 2012 provides **simple and efficient design**
    - First application: Gas Flow Control for the COMPACT Detector
  - Profit from NI maintenance and community developments
  - Network Layer: Abstract Process Variable Base Classes.
    - Default: Shared Variables or DataSocket on Linux/Mac
  - Use as much NI Tools as possible
    - Distributed System Manager, Data Logging & Supervisory Control Module, TDMS & DIAdem
  - Future user: APPA community @ FAIR

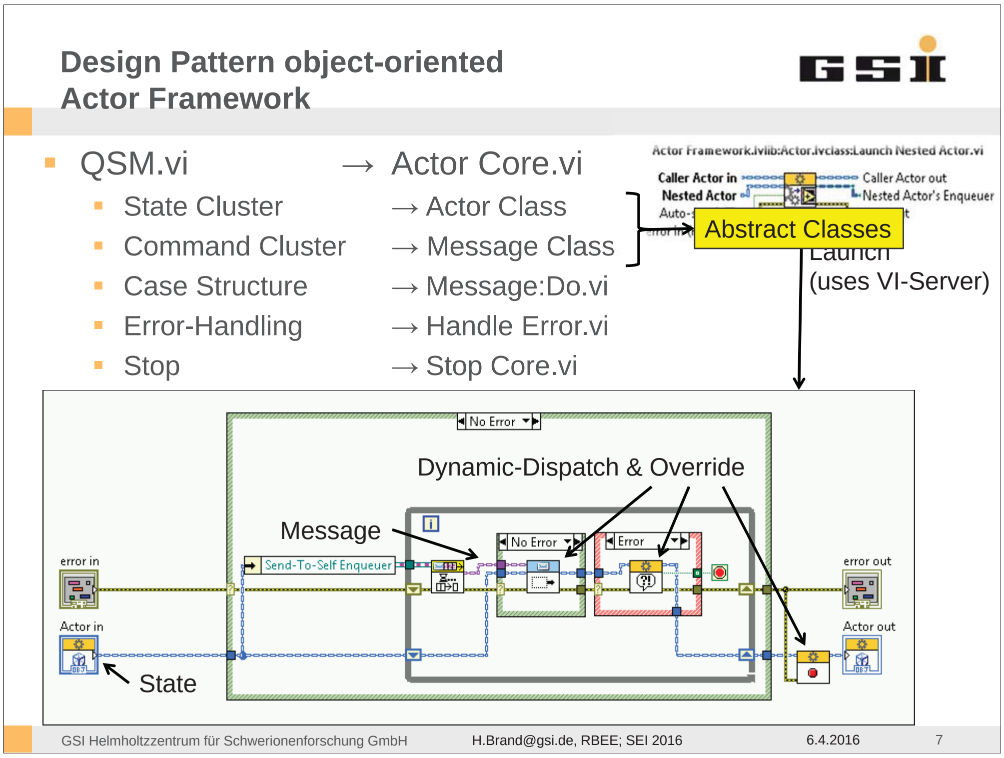
Advantages of LVOOP Classes
(with respect to type definition)

- **Encapsulation**
  - Attribute data is always private. It can be modified by member-VIs only.
  - Interne data structure is hidden.
  - Access: *Public, Protected, Private, Community* (friend)
- **Modularity**
  - Each class has a specified responsibility.
  - Public interface should be well defined.
    - It shouldn't be modifies without really good reason.
  - Simplifies testability.
- **Extensibility**
  - Derived classes extend the attributes and behavior of their ancestor class.
- **Specialization**
  - Derived classes specialize the behavior of their ancestor class.
  - → Override-VI overrides Dynamic-Dispatch-VI
- LabVIEW Objects behave exactly like other Datatypes!
  - They respect LabVIEW‘s dataflow paradigm!

Design Pattern classic: Queued State Maschine
Three Sources of Code Replication

1. **Override** the handling of one message
2. **Extend** the set of handled messages
3. **Decorate** the machine with additional behavior





Design Pattern object-oriented Actor Framework

- QSM.vi → Actor Core.vi
  - State Cluster → Actor Class
  - Command Cluster → Message Class
  - Case Structure → Message:Do.vi
  - Error-Handling → Handle Error.vi
  - Stop → Stop Core.vi

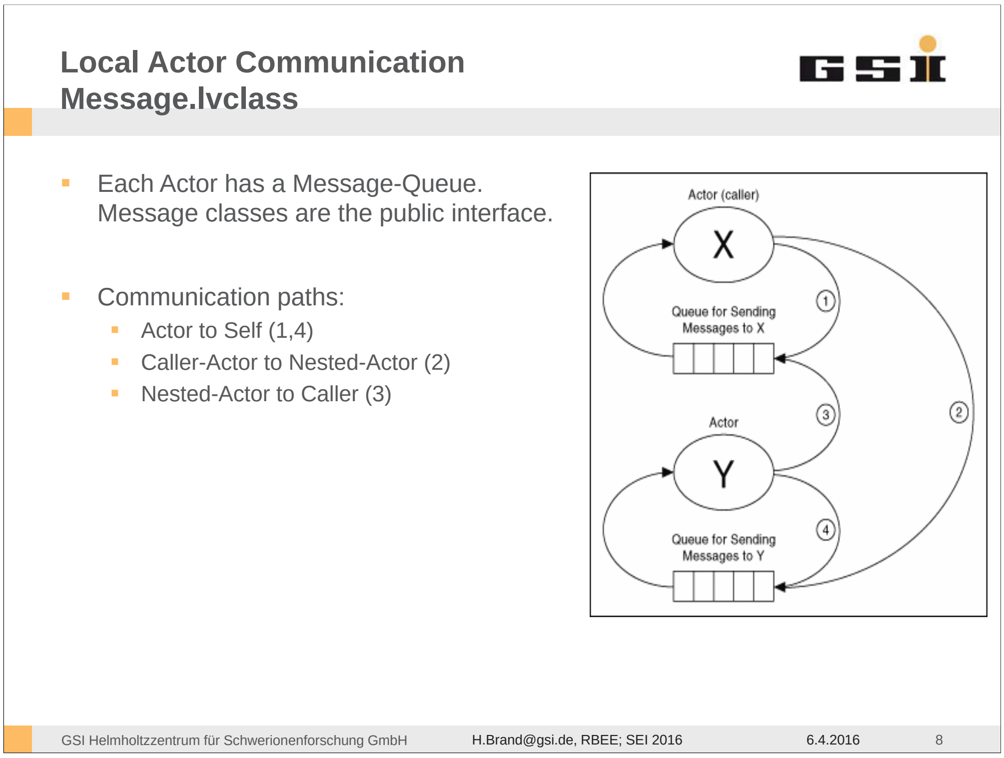
Abstract Classes

Launch (uses VI-Server)

Dynamic-Dispatch & Override

Message

State



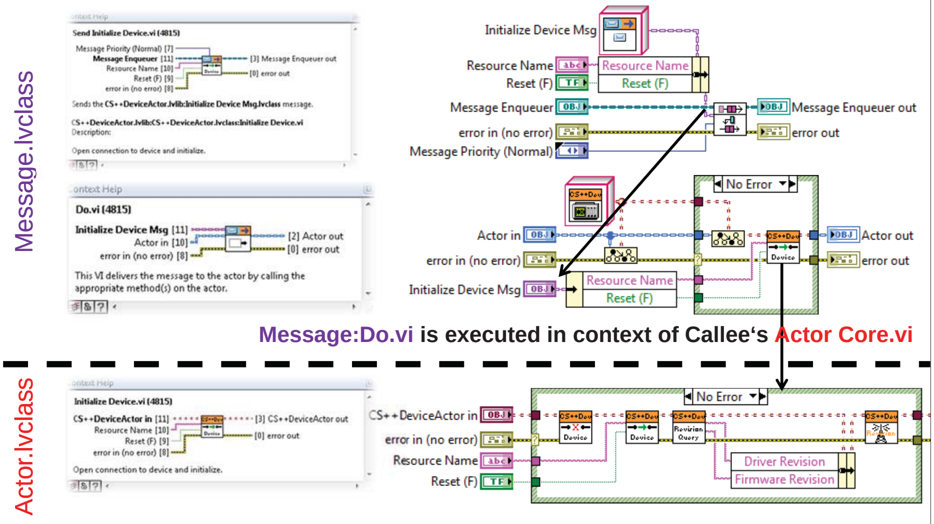
Local Actor Communication Message.lvclass

- Each Actor has a Message-Queue.
  Message classes are the public interface.
- Communication paths:
  - Actor to Self (1,4)
  - Caller-Actor to Nested-Actor (2)
  - Nested-Actor to Caller (3)

Local Actor Communication
Message.lvclass

- **Example:** Initialize Device.vi

Executed in context of Caller Actor



Message.lvclass

Send Initialize Device.vi (4815)

Sends the **CS++DeviceActor.lvlib:Initialize Device Msg.lvclass** message.

CS++DeviceActor.lvlib:CS++DeviceActor.lvclass:Initialize Device.vi
Description:

Open connection to device and initialize.

Do.vi (4815)

This VI delivers the message to the actor by calling the appropriate method(s) on the actor.

Message:Do.vi is executed in context of Callee‘s **Actor Core.vi**

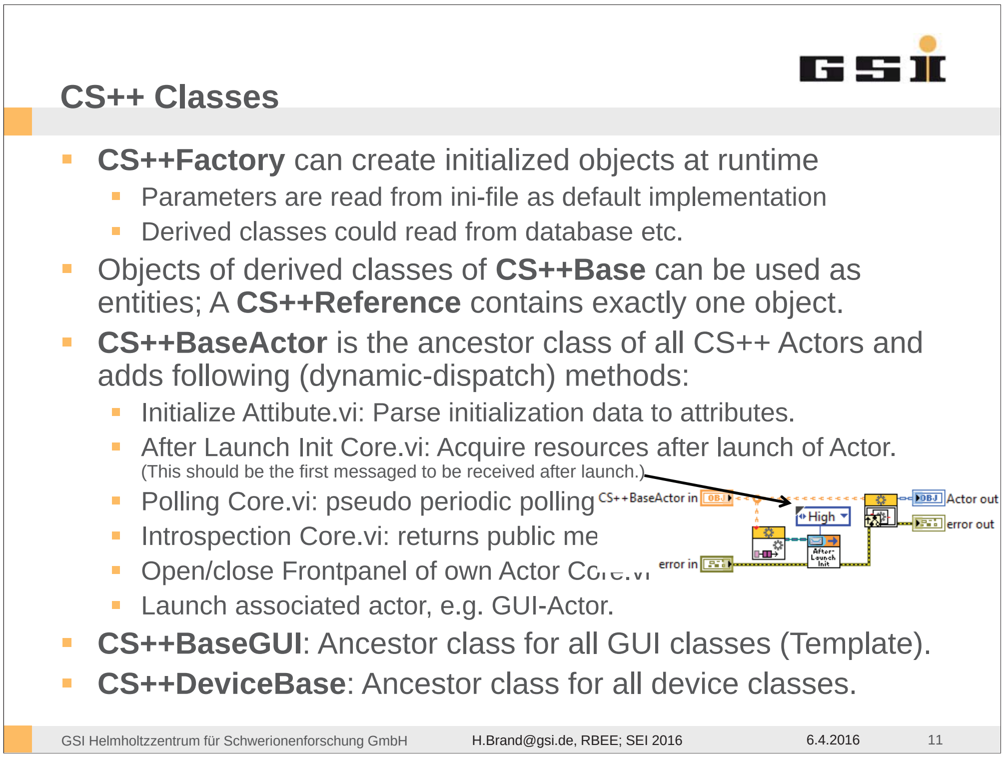
Actor.lvclass

Initialize Device.vi (4815)

Open connection to device and initialize.

CS++ Requirements

- Similar feature set as *CS* Framework based on LVOOP & Dataflow
- CS++ Actor classes should be usable by wire
  - Option for deterministic dataflow
    - To be used in Timed Loop on LV-RealTime or
    - Providing Sequence-Steps for an Sequencer
- Simple Configuration Database
  - Default ini-files; extendable for relational database
- Abstract Network Layer
  - Default implementation is Shared Variable
  - DataSocket for heterogenious LV-Systems with Linux/Mac
  - DIM support for smooth migration from *CS* Framework
- Focus
  - Easy Implementation (just LabVIEW), enforcement of design rules
  - Easy commissioning & reconfiguration and
  - Stable runtime behaviour



CS++ Classes

- **CS++Factory** can create initialized objects at runtime
  - Parameters are read from ini-file as default implementation
  - Derived classes could read from database etc.
- Objects of derived classes of **CS++Base** can be used as entities; A **CS++Reference** contains exactly one object.
- **CS++BaseActor** is the ancestor class of all CS++ Actors and adds following (dynamic-dispatch) methods:
  - Initialize Attibute.vi: Parse initialization data to attributes.
  - After Launch Init Core.vi: Acquire resources after launch of Actor. (This should be the first messaged to be received after launch.)
  - Polling Core.vi: pseudo periodic polling
  - Introspection Core.vi: returns public me
  - Open/close Frontpanel of own Actor Core.vi
  - Launch associated actor, e.g. GUI-Actor.
- **CS++BaseGUI**: Ancestor class for all GUI classes (Template).
- **CS++DeviceBase**: Ancestor class for all device classes.

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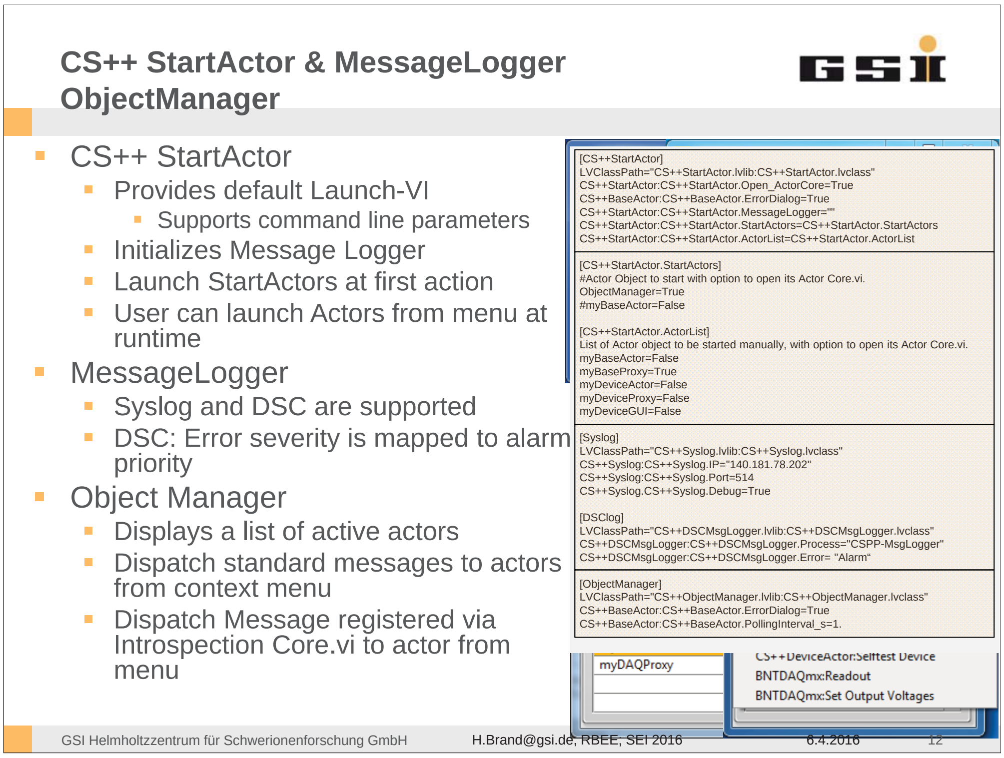

CS++ StartActor & MessageLogger ObjectManager

- CS++ StartActor
  - Provides default Launch-VI
    - Supports command line parameters
  - Initializes Message Logger
  - Launch StartActors at first action
  - User can launch Actors from menu at runtime
- MessageLogger
  - Syslog and DSC are supported
  - DSC: Error severity is mapped to alarm priority
- Object Manager
  - Displays a list of active actors
  - Dispatch standard messages to actors from context menu
  - Dispatch Message registered via Introspection Core.vi to actor from menu

```
[CS++StartActor]
LVClassPath="CS++StartActor.lvlib:CS++StartActor.lvclass"
CS++StartActor:CS++StartActor.Open_ActorCore=True
CS++BaseActor:CS++BaseActor.ErrorDialog=True
CS++StartActor:CS++StartActor.MessageLogger=""
CS++StartActor:CS++StartActor.StartActors=CS++StartActor.StartActors
CS++StartActor:CS++StartActor.ActorList=CS++StartActor.ActorList

[CS++StartActor.StartActors]
#Actor Object to start with option to open its Actor Core.vi.
ObjectManager=True
#myBaseActor=False

[CS++StartActor.ActorList]
List of Actor object to be started manually, with option to open its Actor Core.vi.
myBaseActor=False
myBaseProxy=True
myDeviceActor=False
myDeviceProxy=False
myDeviceGUI=False

[Syslog]
LVClassPath="CS++Syslog.lvlib:CS++Syslog.lvclass"
CS++Syslog:CS++Syslog.IP="140.181.78.202"
CS++Syslog:CS++Syslog.Port=514
CS++Syslog.CS++Syslog.Debug=True

[DSClog]
LVClassPath="CS++DSCMsgLogger.lvlib:CS++DSCMsgLogger.lvclass"
CS++DSCMsgLogger:CS++DSCMsgLogger.Process="CSPP-MsgLogger"
CS++DSCMsgLogger:CS++DSCMsgLogger.Error= "Alarm"

[ObjectManager]
LVClassPath="CS++ObjectManager.lvlib:CS++ObjectManager.lvclass"
CS++BaseActor:CS++BaseActor.ErrorDialog=True
CS++BaseActor:CS++BaseActor.PollingInterval_s=1.
```

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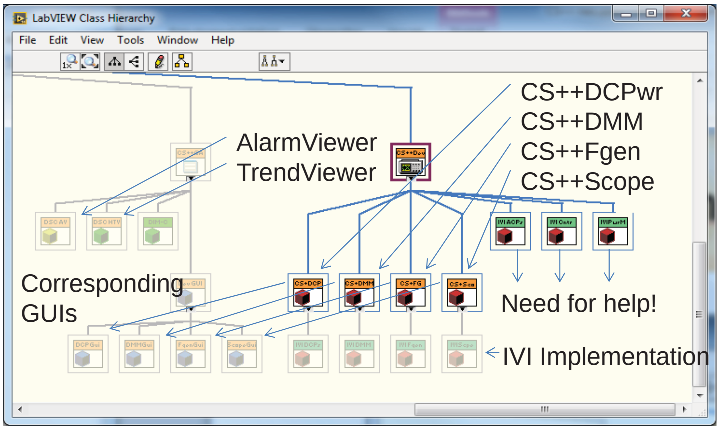
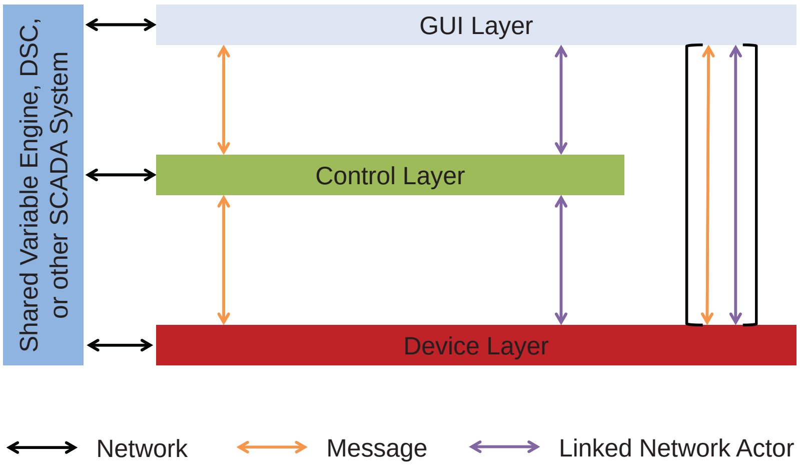
CS++ Device Classes

- CS++DCPwr, CS++DMM, CS++Fgen, CS++Scope & GUI
  - IVI Implementation available
- CS++Motor, CS++MCS & GUI
  - Concrete implementation examples are available.



CS++ Architecture & Communication



Shared Variable Engine, DSC, or other SCADA System

GUI Layer

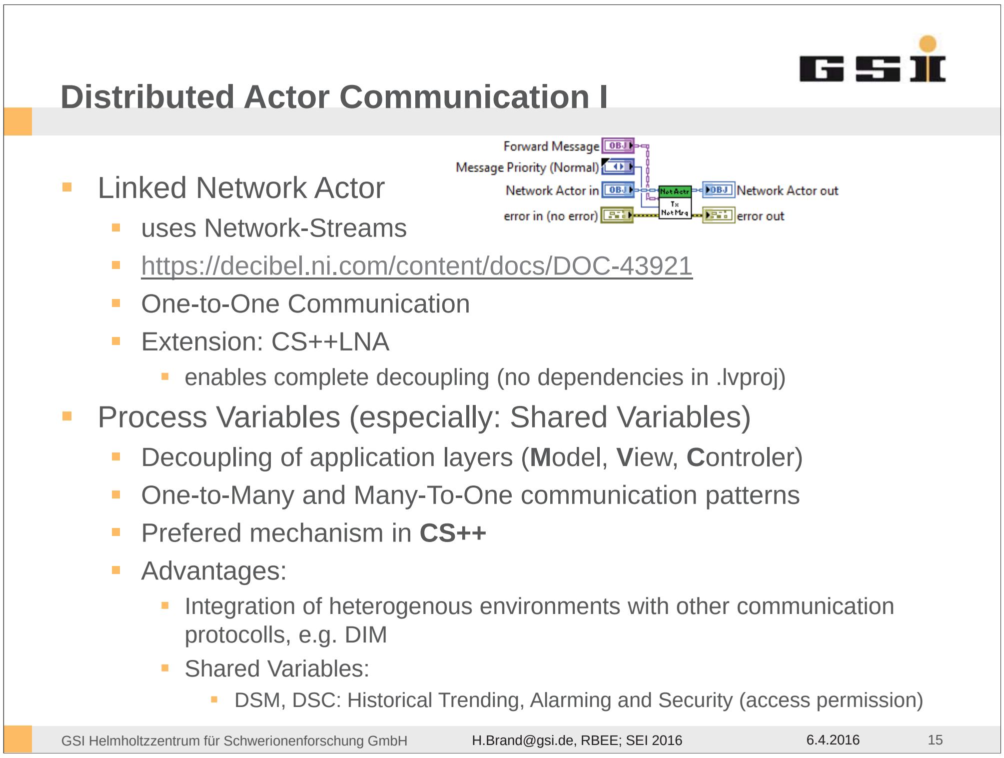
Control Layer

Device Layer

Network

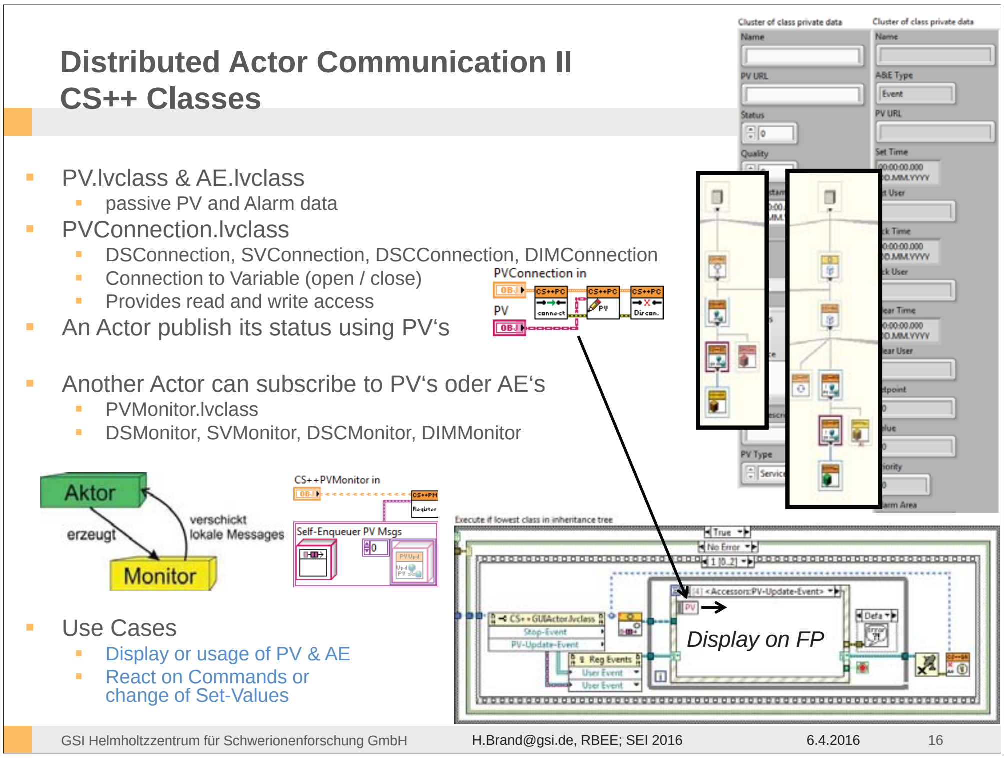
Message

Linked Network Actor



Distributed Actor Communication I

- Linked Network Actor
  - uses Network-Streams
  - https://decibel.ni.com/content/docs/DOC-43921
  - One-to-One Communication
  - Extension: CS++LNA
    - enables complete decoupling (no dependencies in .lvproj)
- Process Variables (especially: Shared Variables)
  - Decoupling of application layers (**M**odel, **V**iew, **C**ontroler)
  - One-to-Many and Many-To-One communication patterns
  - Prefered mechanism in **CS++**
  - Advantages:
    - Integration of heterogenous environments with other communication protocolls, e.g. DIM
    - Shared Variables:
      - DSM, DSC: Historical Trending, Alarming and Security (access permission)



Distributed Actor Communication II
CS++ Classes

- PV.lvclass & AE.lvclass
  - passive PV and Alarm data
- PVConnection.lvclass
  - DSConnection, SVConnection, DSCConnection, DIMConnection
  - Connection to Variable (open / close)
  - Provides read and write access
- An Actor publish its status using PV's
- Another Actor can subscribe to PV's oder AE's
  - PVMonitor.lvclass
  - DSMonitor, SVMonitor, DSCMonitor, DIMMonitor
- Use Cases
  - Display or usage of PV & AE
  - React on Commands or change of Set-Values

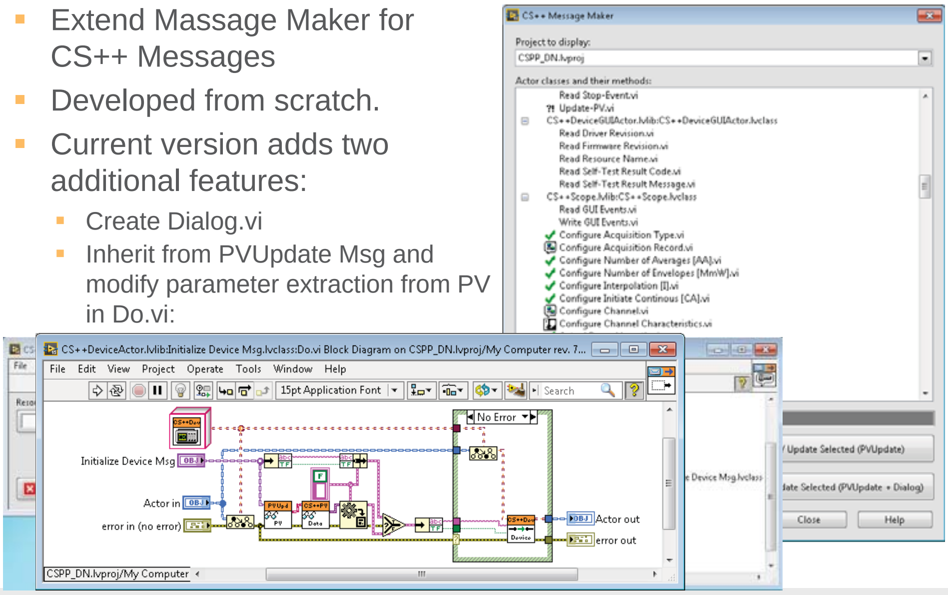
CS++ Configuration

```
[PV_Protocols]
ni.var.psp=DSCConnection

[DSCConnection]
LVClassPath="CS++DSCConnection.lvlib:DSCConnection.lvclass"

#_p:Polling, _e:Events
[PV_Monitors]
ni.var.psp_p=DSCMonitor
ni.var.psp_e=DSCMonitor

[DSCMonitor]
LVClassPath="CS++DSCMonitor.lvlib:CS++DSCMonitor.lvclass"
```

```
[myBaseActor]
LVClassPath="CS++BaseActor.lvlib:CS++BaseActor.lvclass"
CS++BaseActor:CS++BaseActor.DefaultGUI=""
CS++BaseActor:CS++BaseActor.LaunchDefaultGUI=False
CS++BaseActor:CS++BaseActor.ErrorDialog=True
CS++BaseActor:CS++BaseActor.PollingInterval_s=-1.

[myBaseActor.URLs]
PollingMode="ni.var.psp://localhost/CSPP_Core_SV/myBaseActor_PollingMode?.1"
PollingTime="ni.var.psp://localhost/CSPP_Core_SV/myBaseActor_PollingTime?.1"
PollingInterval="ni.var.psp://localhost/CSPP_Core_SV/myBaseActor_PollingInterval?.1"

[myBaseProxy]
LVClassPath="CS++PVProxy.lvlib:CS++PVProxy.lvclass"
CS++BaseActor:CS++BaseActor.DefaultGUI=""
CS++BaseActor:CS++BaseActor.LaunchDefaultGUI=False
CS++BaseActor:CS++BaseActor.ErrorDialog=True
CS++BaseActor:CS++BaseActor.PollingInterval_s=-1.
CS++PVProxy:CS++PVProxy.WorkerActor="myBaseActor"
CS++PVProxy:CS++PVProxy.DelayedActivation=True

[myBaseProxy.URLs]
Activate="ni.var.psp://localhost/CSPP_Core_SV/myBaseProxy_Activate?.1"
WorkerActor="ni.var.psp://localhost04/CSPP_Core_SV/myBaseProxy_WorkerActor|1024?.1"
Polling_Interval_Msg="ni.var.psp://localhost/CSPP_Core_SV/myBaseActor_PollingInterval?.1"
Polling_Start_Stop_Msg="ni.var.psp://localhost4/CSPP_Core_SV/myBaseActor_PollingStartStop?.1"
```

CS++ Message Maker

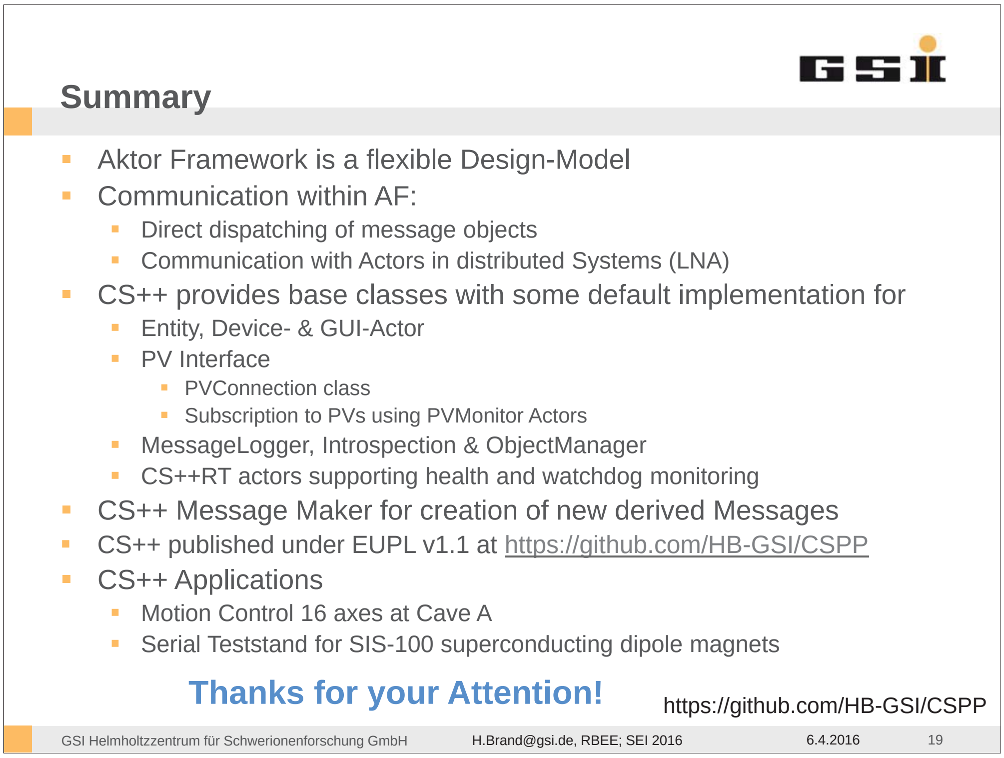
- Extend Massage Maker for CS++ Messages
- Developed from scratch.
- Current version adds two additional features:
  - Create Dialog.vi
  - Inherit from PVUpdate Msg and modify parameter extraction from PV in Do.vi:



CS++ Message Maker

Project to display: CSPP_DN.lvproj

CS++DeviceActor.lvlib:Initialize Device Msg.lvclass:Do.vi Block Diagram on CSPP_DN.lvproj/My Computer rev. 7...

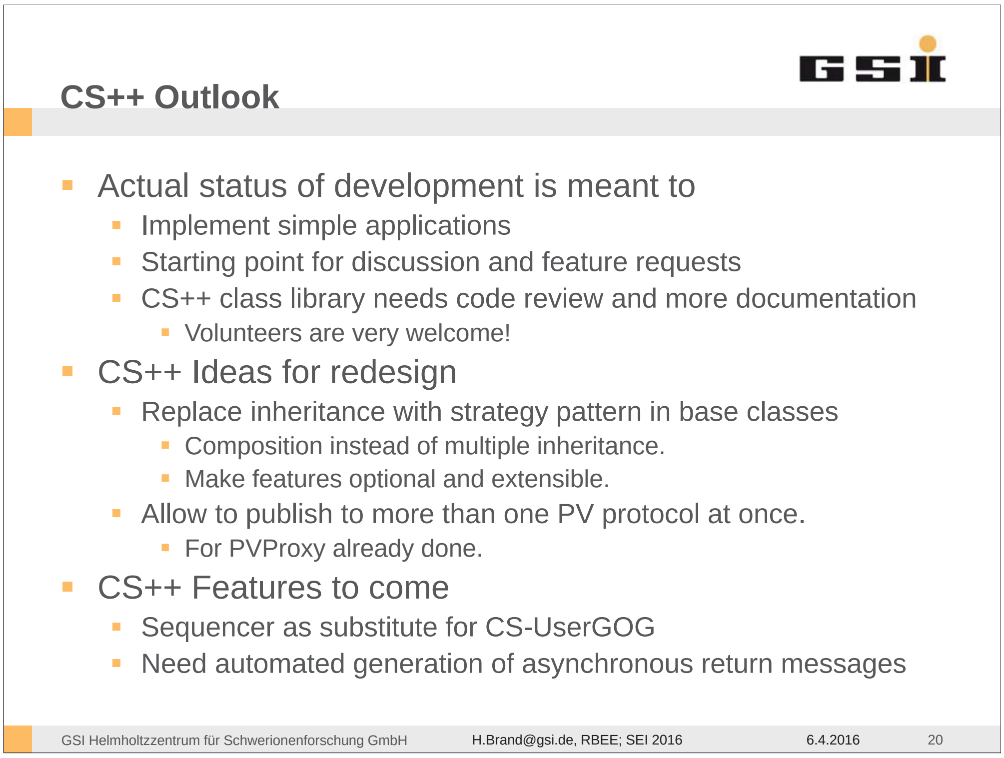


Summary

- Aktor Framework is a flexible Design-Model
- Communication within AF:
  - Direct dispatching of message objects
  - Communication with Actors in distributed Systems (LNA)
- CS++ provides base classes with some default implementation for
  - Entity, Device- & GUI-Actor
  - PV Interface
    - PVConnection class
    - Subscription to PVs using PVMonitor Actors
  - MessageLogger, Introspection & ObjectManager
  - CS++RT actors supporting health and watchdog monitoring
- CS++ Message Maker for creation of new derived Messages
- CS++ published under EUPL v1.1 at https://github.com/HB-GSI/CSPP
- CS++ Applications
  - Motion Control 16 axes at Cave A
  - Serial Teststand for SIS-100 superconducting dipole magnets

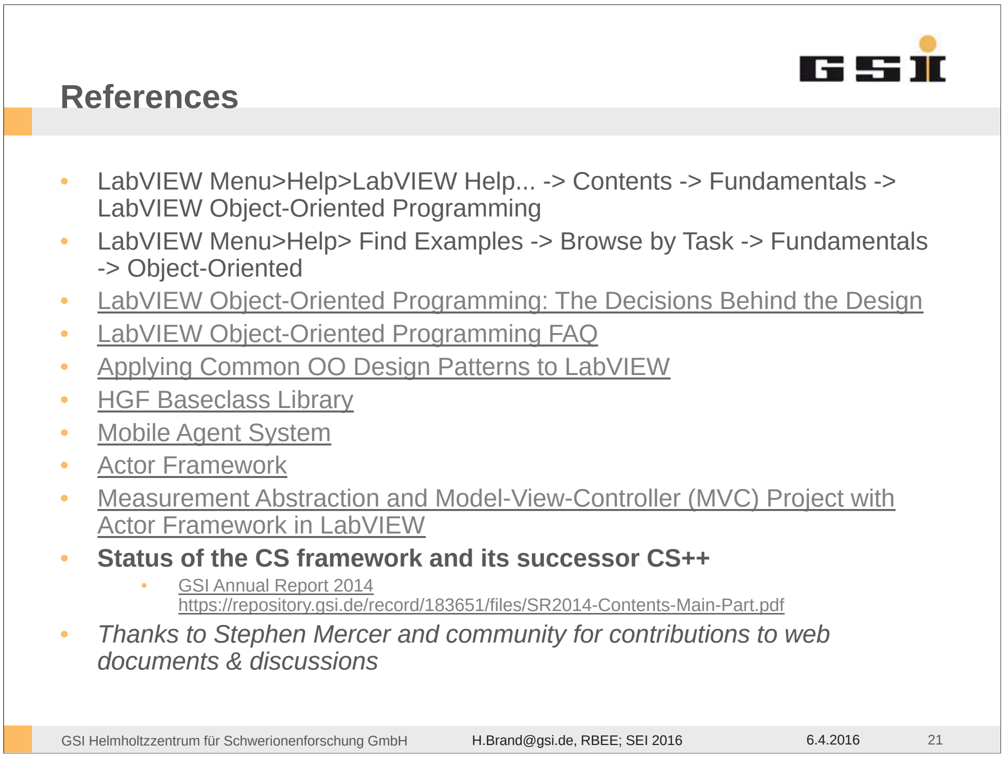
Thanks for your Attention!

https://github.com/HB-GSI/CSPP



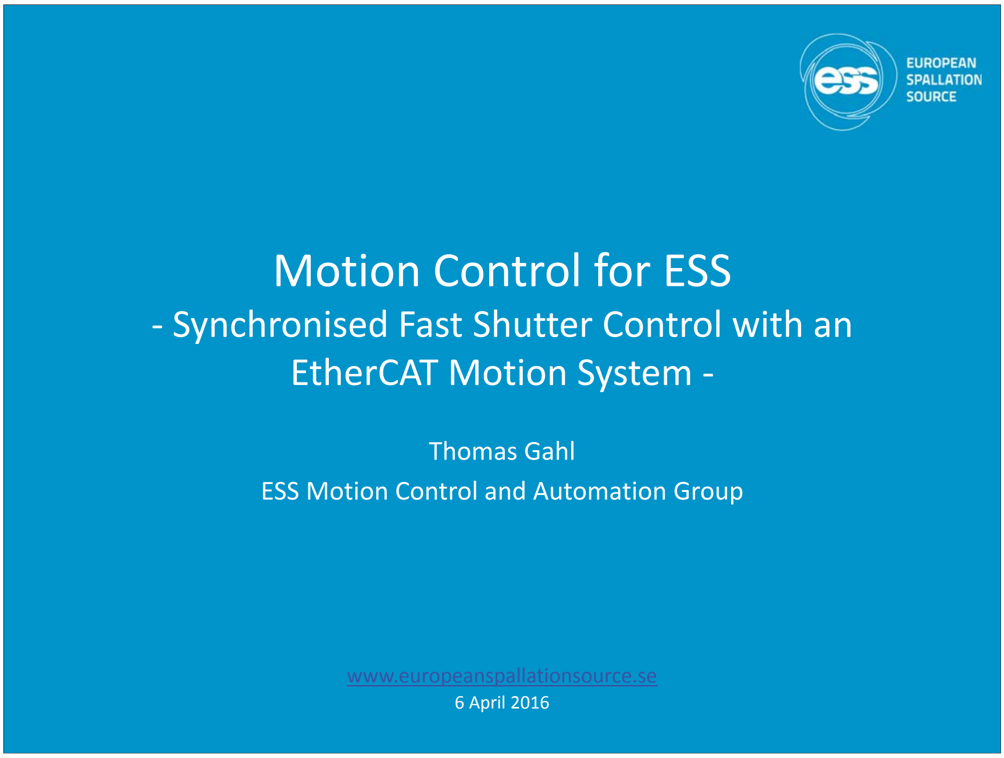
CS++ Outlook

- Actual status of development is meant to
  - Implement simple applications
  - Starting point for discussion and feature requests
  - CS++ class library needs code review and more documentation
    - Volunteers are very welcome!
- CS++ Ideas for redesign
  - Replace inheritance with strategy pattern in base classes
    - Composition instead of multiple inheritance.
    - Make features optional and extensible.
  - Allow to publish to more than one PV protocol at once.
    - For PVProxy already done.
- CS++ Features to come
  - Sequencer as substitute for CS-UserGOG
  - Need automated generation of asynchronous return messages



References

- LabVIEW Menu>Help>LabVIEW Help... -> Contents -> Fundamentals -> LabVIEW Object-Oriented Programming
- LabVIEW Menu>Help> Find Examples -> Browse by Task -> Fundamentals -> Object-Oriented
- LabVIEW Object-Oriented Programming: The Decisions Behind the Design
- LabVIEW Object-Oriented Programming FAQ
- Applying Common OO Design Patterns to LabVIEW
- HGF Baseclass Library
- Mobile Agent System
- Actor Framework
- Measurement Abstraction and Model-View-Controller (MVC) Project with Actor Framework in LabVIEW
- **Status of the CS framework and its successor CS++**
  - GSI Annual Report 2014 https://repository.gsi.de/record/183651/files/SR2014-Contents-Main-Part.pdf
- *Thanks to Stephen Mercer and community for contributions to web documents & discussions*



EUROPEAN SPALLATION SOURCE

Motion Control for ESS

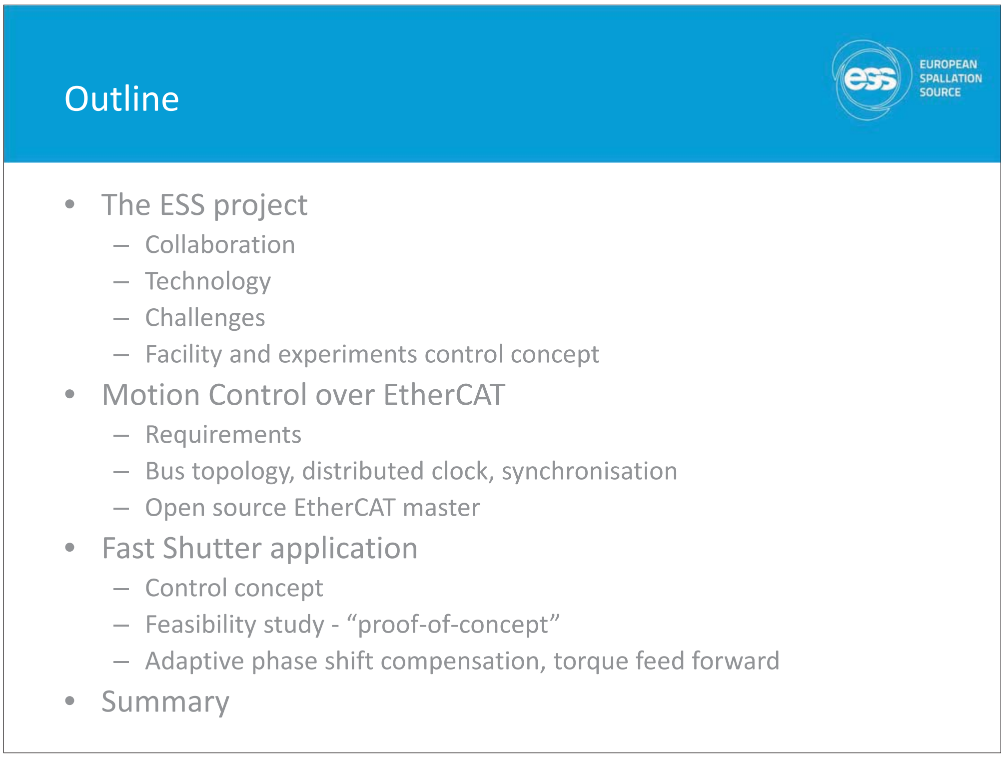
- Synchronised Fast Shutter Control with an EtherCAT Motion System -

Thomas Gahl

ESS Motion Control and Automation Group

www.europeanspallationsource.se

6 April 2016



Outline

EUROPEAN SPALLATION SOURCE

- The ESS project
  - Collaboration
  - Technology
  - Challenges
  - Facility and experiments control concept
- Motion Control over EtherCAT
  - Requirements
  - Bus topology, distributed clock, synchronisation
  - Open source EtherCAT master
- Fast Shutter application
  - Control concept
  - Feasibility study - “proof-of-concept”
  - Adaptive phase shift compensation, torque feed forward
- Summary

ESS – a collaborative project

European Spallation Source -
ESS, Lund, Sweden

Aarhus University
CEA Saclay, Paris
CNRS Orsay, Paris
ESS Bilbao
INFN, Catania
Lund University
Uppsala University
Accelerator Science and Technology Centre, Daresbury and Oxford
CERN, Geneva
Cockcroft Institute, Daresbury
DESY, Hamburg
KIT, Karlsruhe
Fermi National Laboratory, Chicago
John Adams Institute for Accelerator Science, London and Oxford
Laval University, Canada
Maribor University, Slovenia

National Centre for Nuclear Research, Poland
Oslo University
Rostock University
Spallation Neutron Source, Oak Ridge
Stockholm University
Technical University of Darmstadt
Nuclear Physics Institute Of The ASCR
Czech Technical University, Prague
Aarhus University
University Of Copenhagen
University Of Southern Danmark
Technical University Of Danmark - DTU
Institut Laue-Langevin - ILL
Laboratoire Léon Brillouin - LLB
Wigner Institute, Budapest
Helmholtz-Zentrum, Geesthacht
Technical University, Munich
Forschungszentrum, Jülich
Elettra-Sincrotrone Trieste
Università Di Perugia
Consiglio Nazionale Delle Ricerche
Delft University Of Technology
Institute For Energy Technology, IFE
Linköping University
Mid Sweden University
École Polytechnique Fédérale De Lausanne - EPFL
Paul Scherrer Institute - PSI

ESS – 17 European partner countries

European Spallation Source -
ESS, Lund, Sweden

National Centre for Nuclear Research, Poland
Oslo University
Rostock University
Spallation Neutron Source, Oak Ridge
Stockholm University
Technical University of Darmstadt
Nuclear Physics Institute Of The ASCR
Czech Technical University, Prague
Aarhus University
University Of Copenhagen
University Of Southern Danmark
Technical University Of Danmark - DTU
Institut Laue-Langevin - ILL
Laboratoire Léon Brillouin - LLB
Wigner Institute, Budapest
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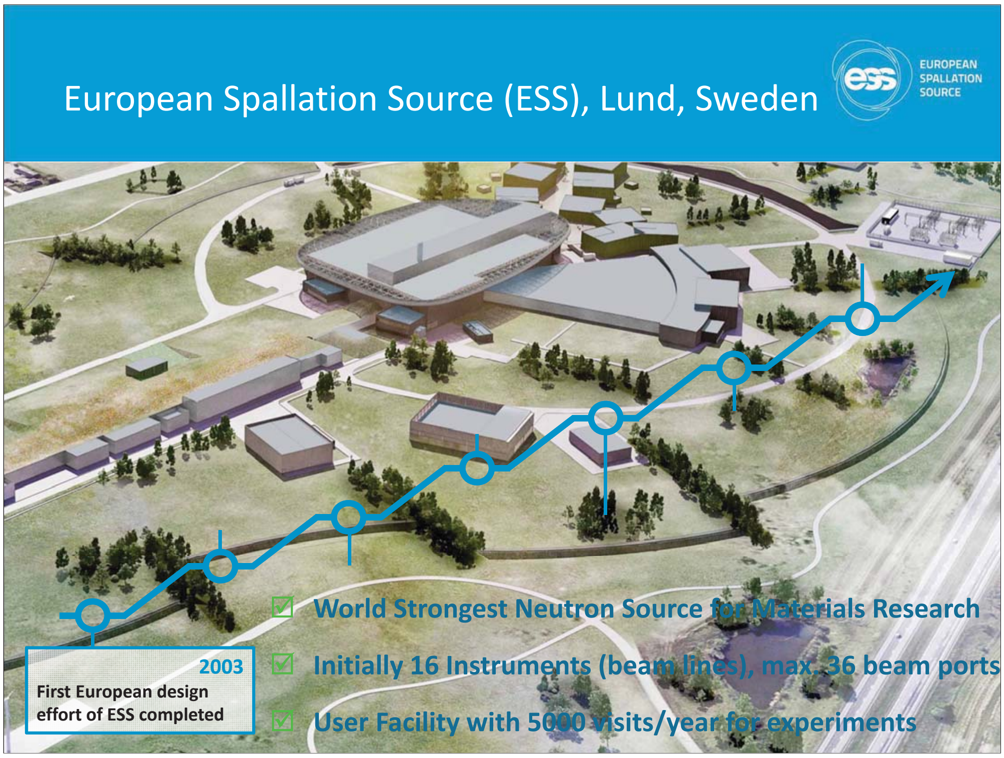
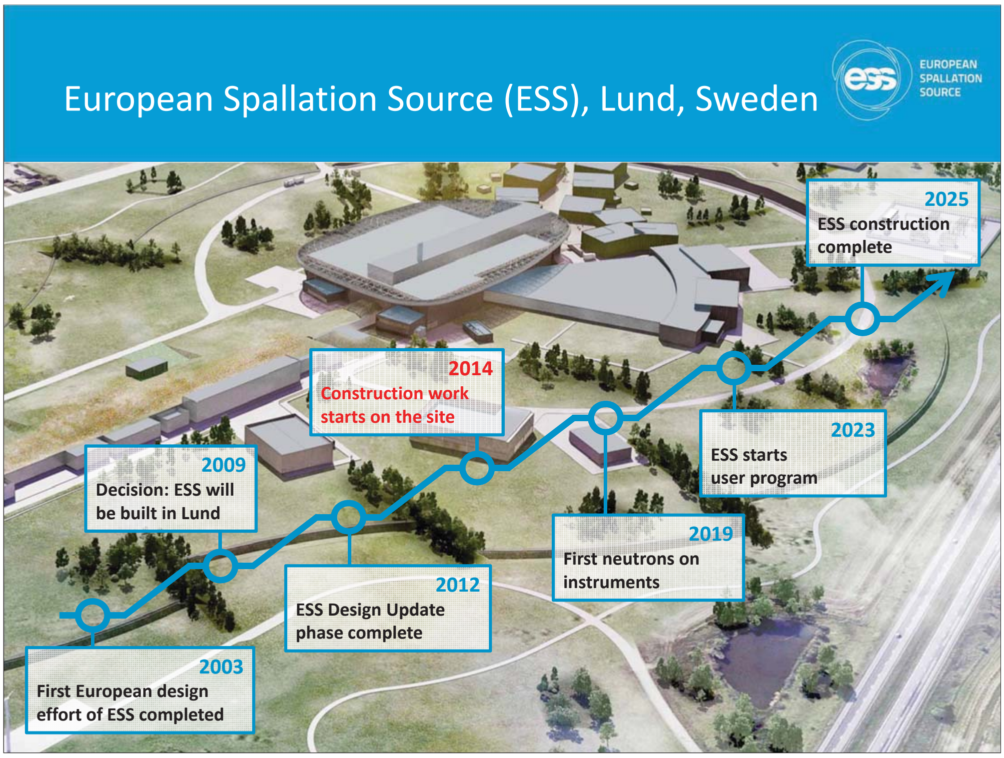


European Spallation Source (ESS), Lund, Sweden

2003
First European design effort of ESS completed

- ☑ World Strongest Neutron Source for Materials Research
- ☑ Initially 16 Instruments (beam lines), max. 36 beam ports
- ☑ User Facility with 5000 visits/year for experiments



European Spallation Source (ESS), Lund, Sweden

2003
First European design effort of ESS completed

2009
Decision: ESS will be built in Lund

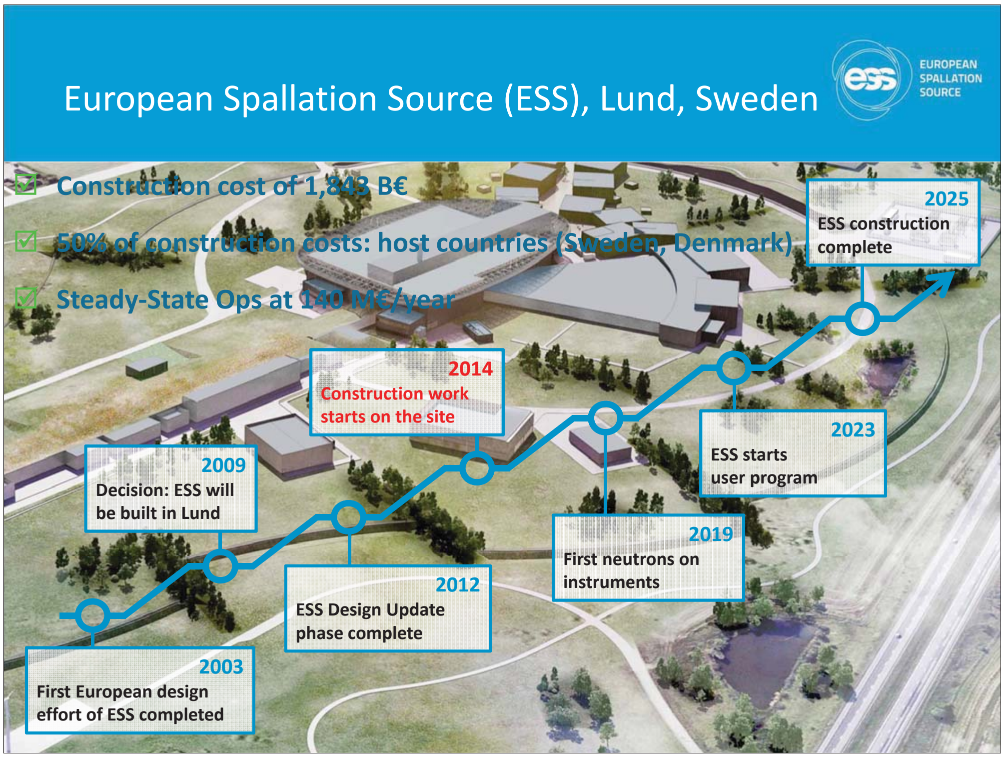
2012
ESS Design Update phase complete

2014
Construction work starts on the site

2019
First neutrons on instruments

2023
ESS starts user program

2025
ESS construction complete



European Spallation Source (ESS), Lund, Sweden

EUROPEAN SPALLATION SOURCE

- ☑ Construction cost of 1,843 B€
- ☑ 50% of construction costs: host countries (Sweden, Denmark)
- ☑ Steady-State Ops at 140 M€/year

2003 First European design effort of ESS completed

2009 Decision: ESS will be built in Lund

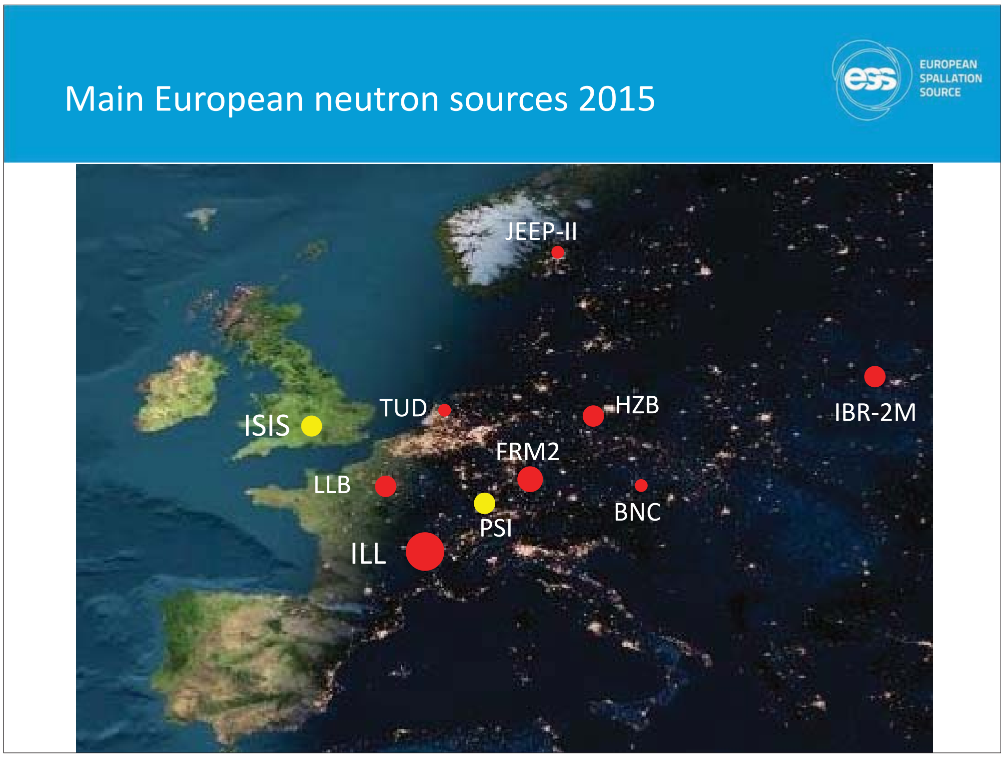
2012 ESS Design Update phase complete

2014 Construction work starts on the site

2019 First neutrons on instruments

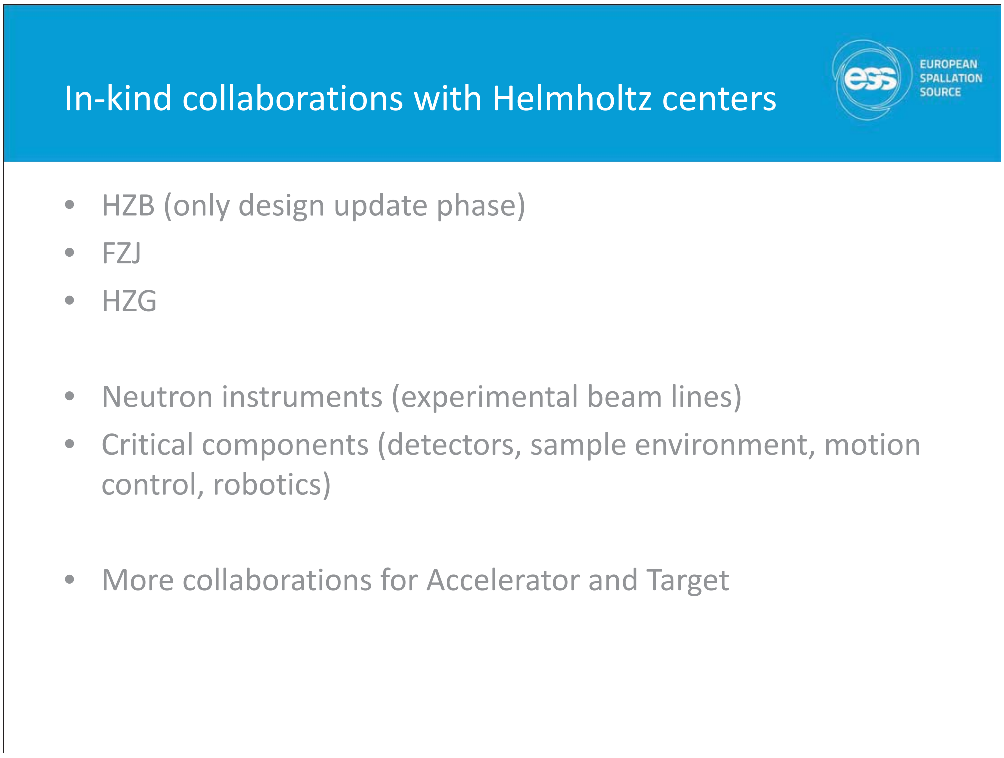
2023 ESS starts user program

2025 ESS construction complete



Main European neutron sources 2015

EUROPEAN SPALLATION SOURCE

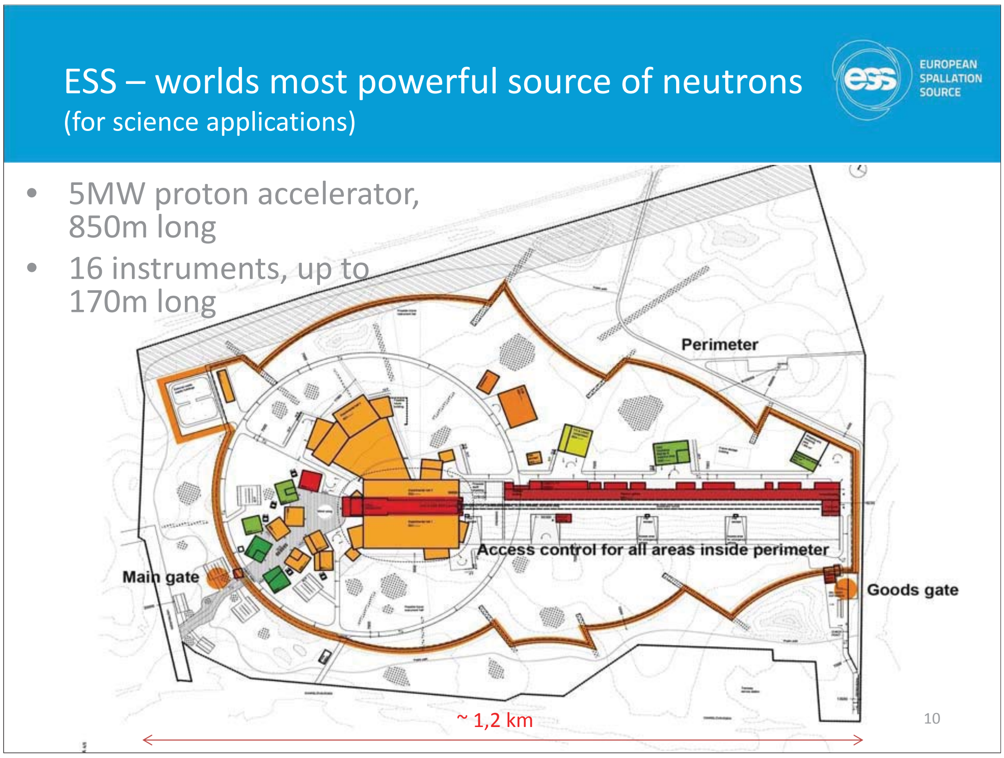


In-kind collaborations with Helmholtz centers

- HZB (only design update phase)
- FZJ
- HZG

- Neutron instruments (experimental beam lines)
- Critical components (detectors, sample environment, motion control, robotics)

- More collaborations for Accelerator and Target

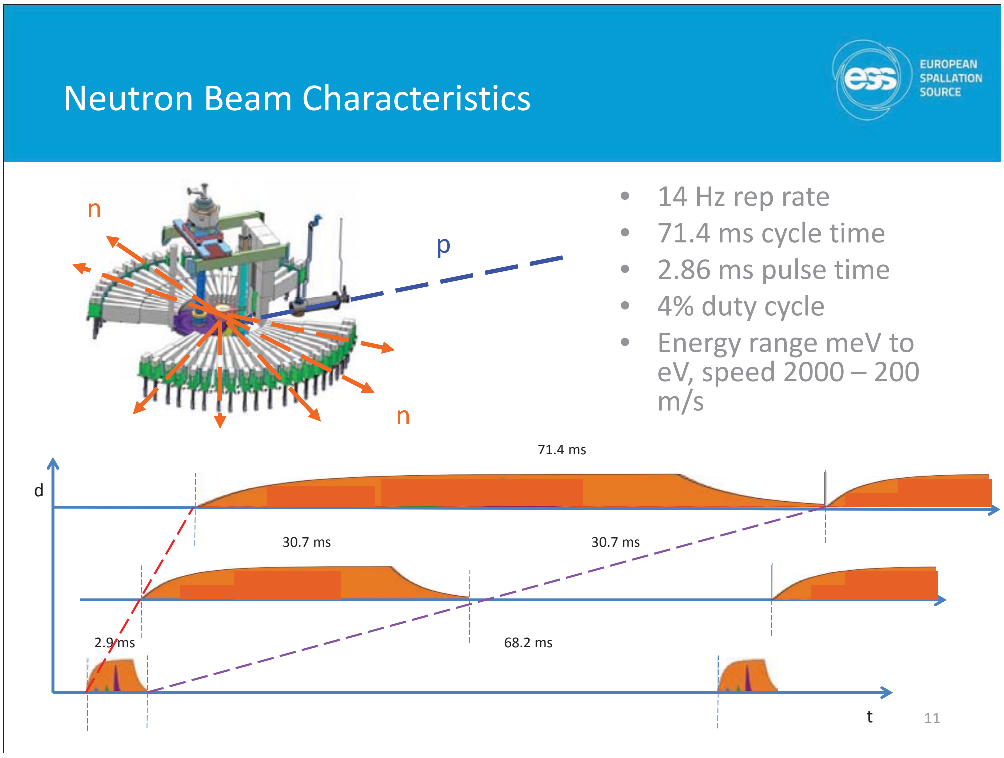


ESS – worlds most powerful source of neutrons

(for science applications)

- 5MW proton accelerator, 850m long
- 16 instruments, up to 170m long

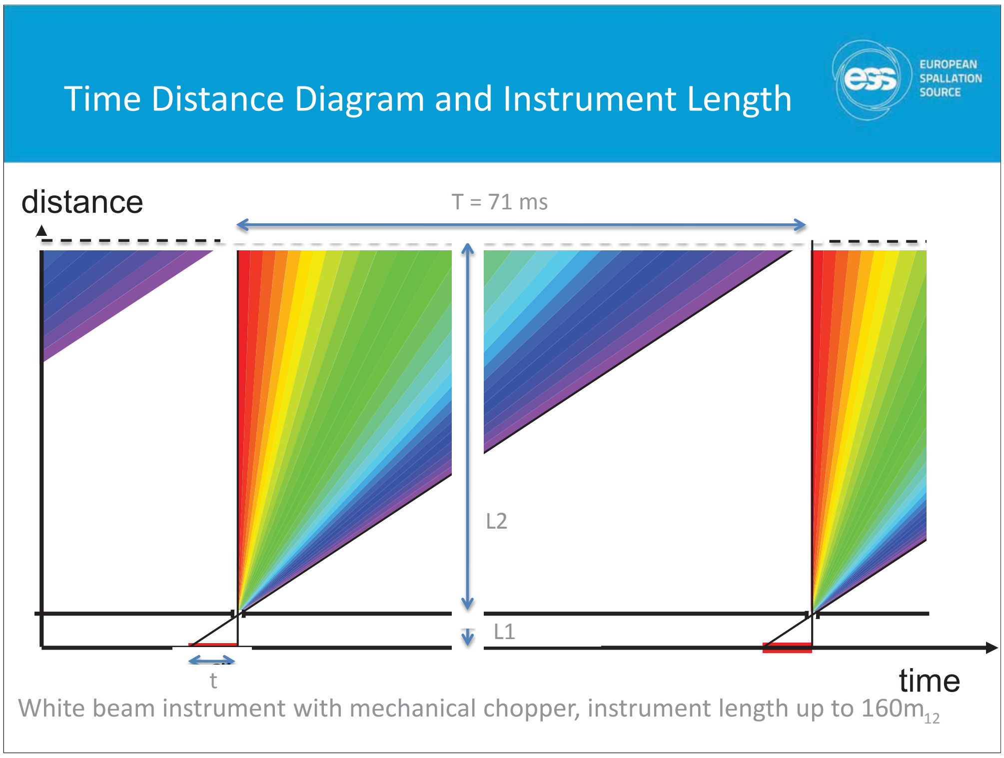
10



Neutron Beam Characteristics

EUROPEAN SPALLATION SOURCE

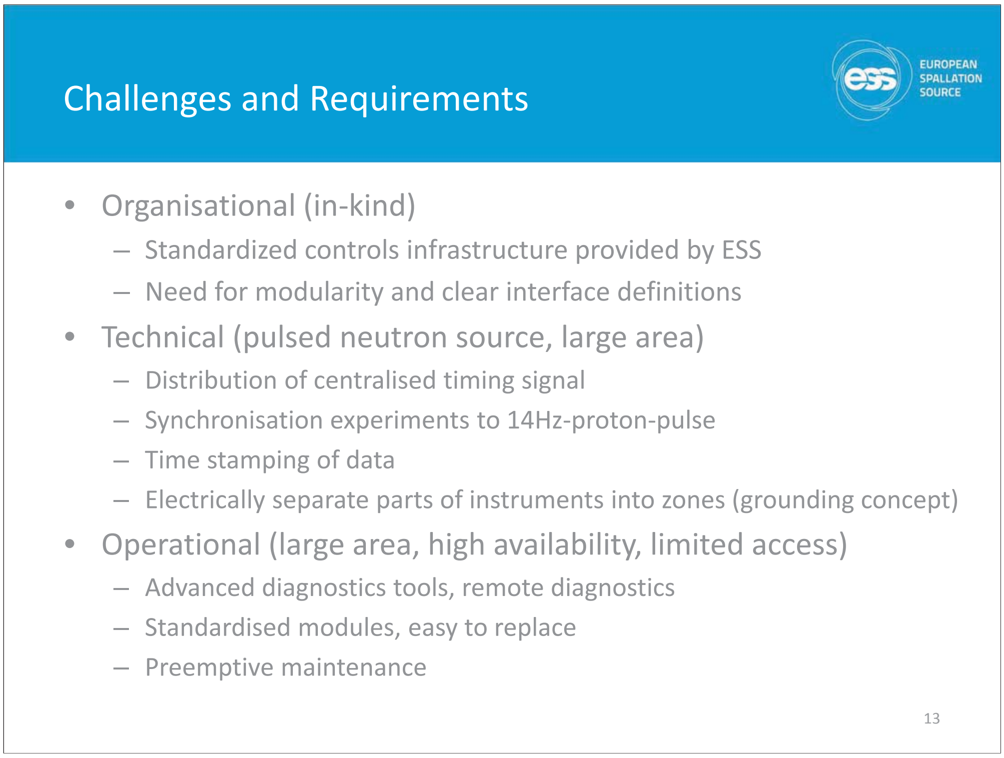
- 14 Hz rep rate
- 71.4 ms cycle time
- 2.86 ms pulse time
- 4% duty cycle
- Energy range meV to eV, speed 2000 – 200 m/s



Time Distance Diagram and Instrument Length

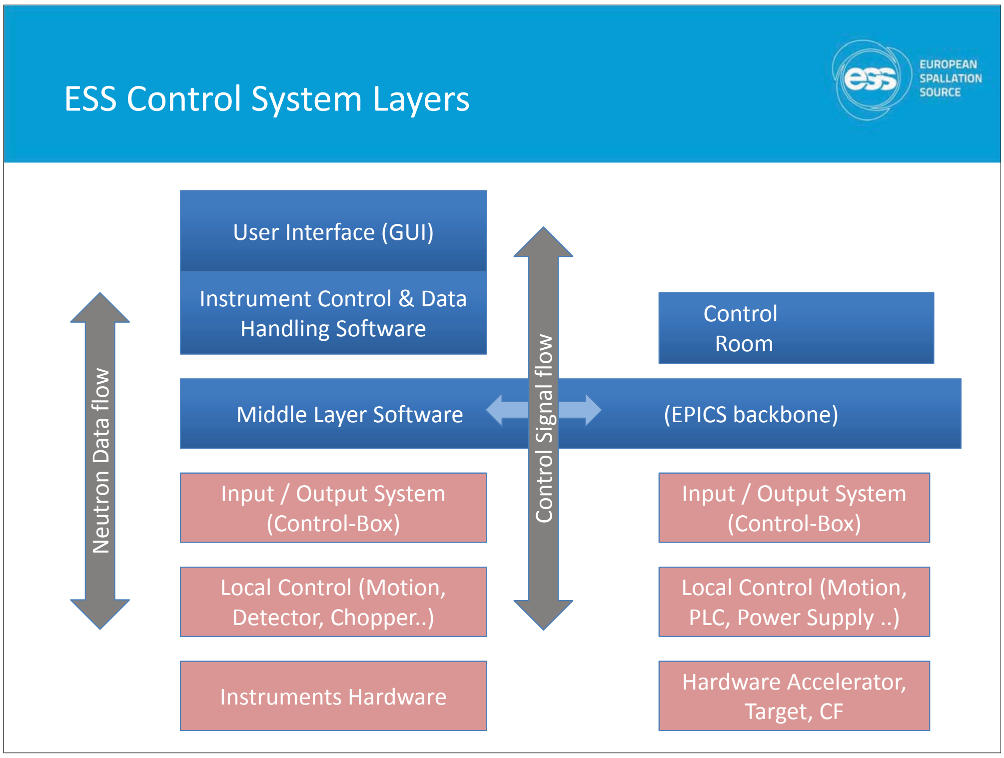
EUROPEAN SPALLATION SOURCE

White beam instrument with mechanical chopper, instrument length up to 160m



Challenges and Requirements

- Organisational (in-kind)
  - Standardized controls infrastructure provided by ESS
  - Need for modularity and clear interface definitions
- Technical (pulsed neutron source, large area)
  - Distribution of centralised timing signal
  - Synchronisation experiments to 14Hz-proton-pulse
  - Time stamping of data
  - Electrically separate parts of instruments into zones (grounding concept)
- Operational (large area, high availability, limited access)
  - Advanced diagnostics tools, remote diagnostics
  - Standardised modules, easy to replace
  - Preemptive maintenance



ESS Control System Layers

User Interface (GUI)

Instrument Control & Data Handling Software

Control Room

Middle Layer Software

(EPICS backbone)

Input / Output System (Control-Box)

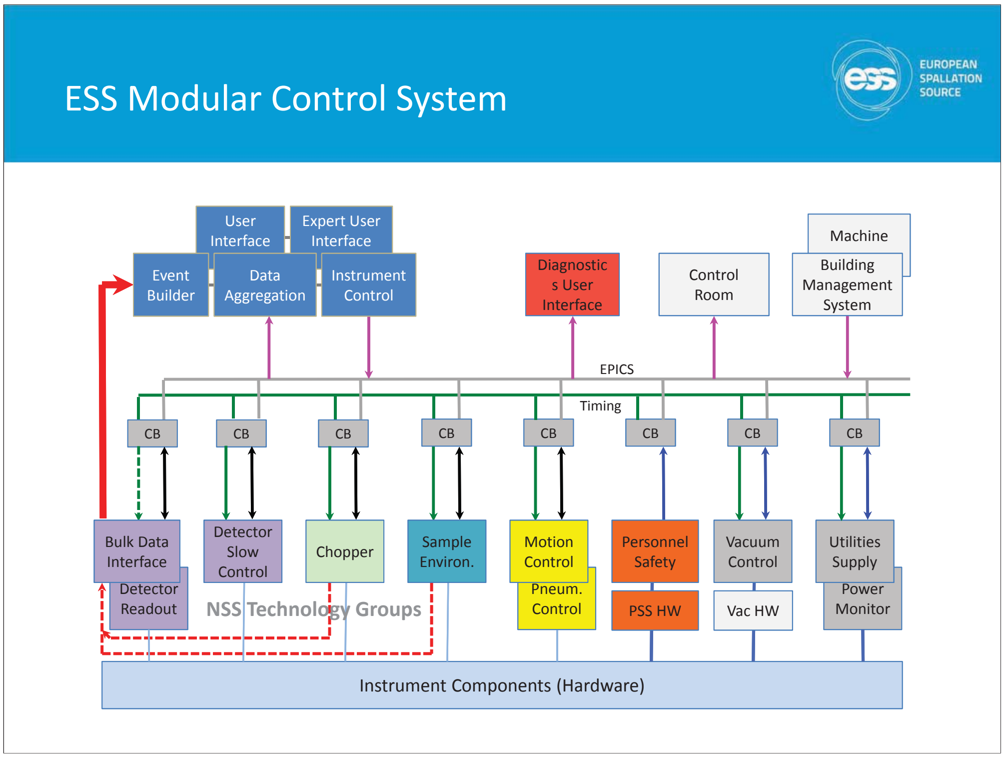
Input / Output System (Control-Box)

Local Control (Motion, Detector, Chopper..)

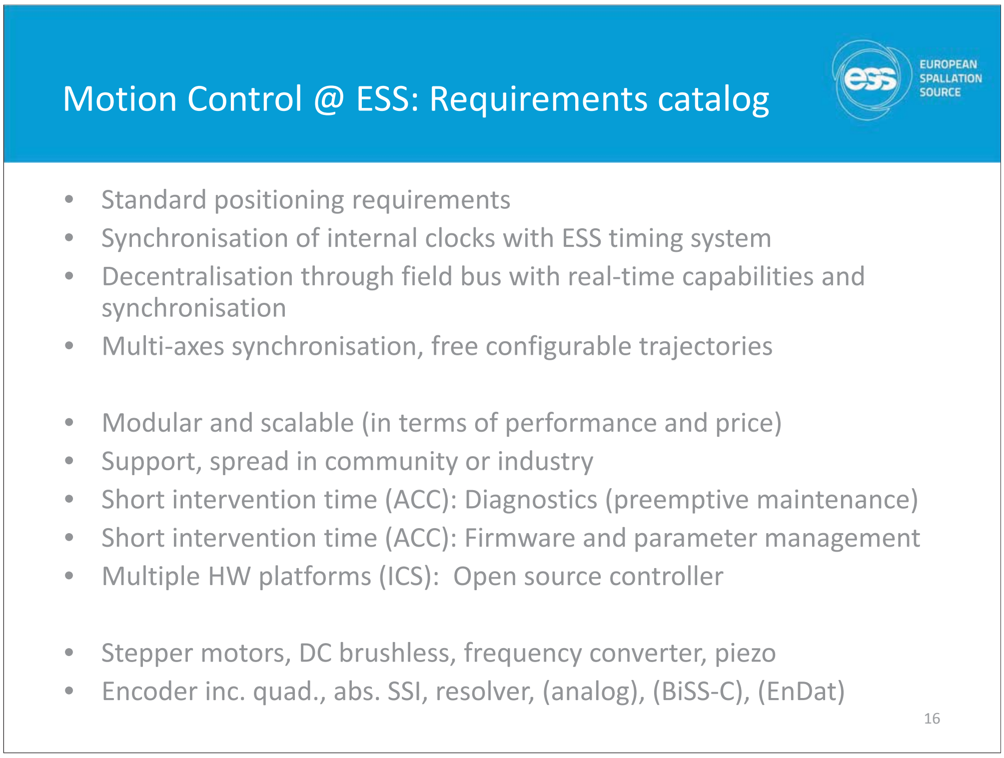
Local Control (Motion, PLC, Power Supply ..)

Instruments Hardware

Hardware Accelerator, Target, CF



ESS Modular Control System

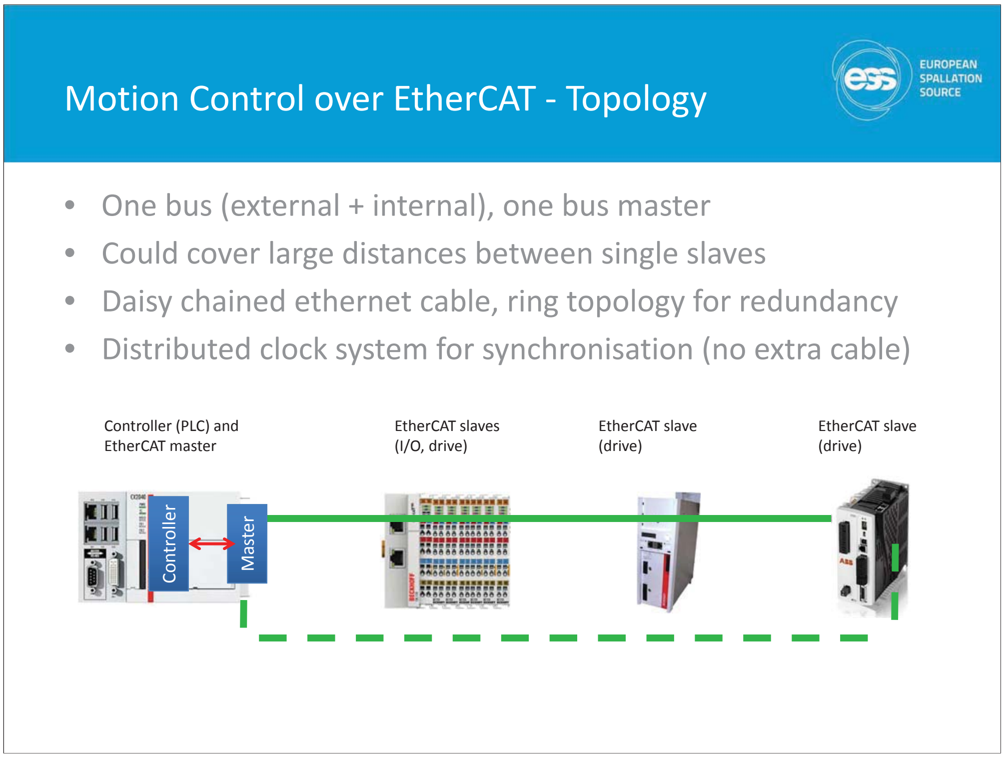


Motion Control @ ESS: Requirements catalog

- Standard positioning requirements
- Synchronisation of internal clocks with ESS timing system
- Decentralisation through field bus with real-time capabilities and synchronisation
- Multi-axes synchronisation, free configurable trajectories

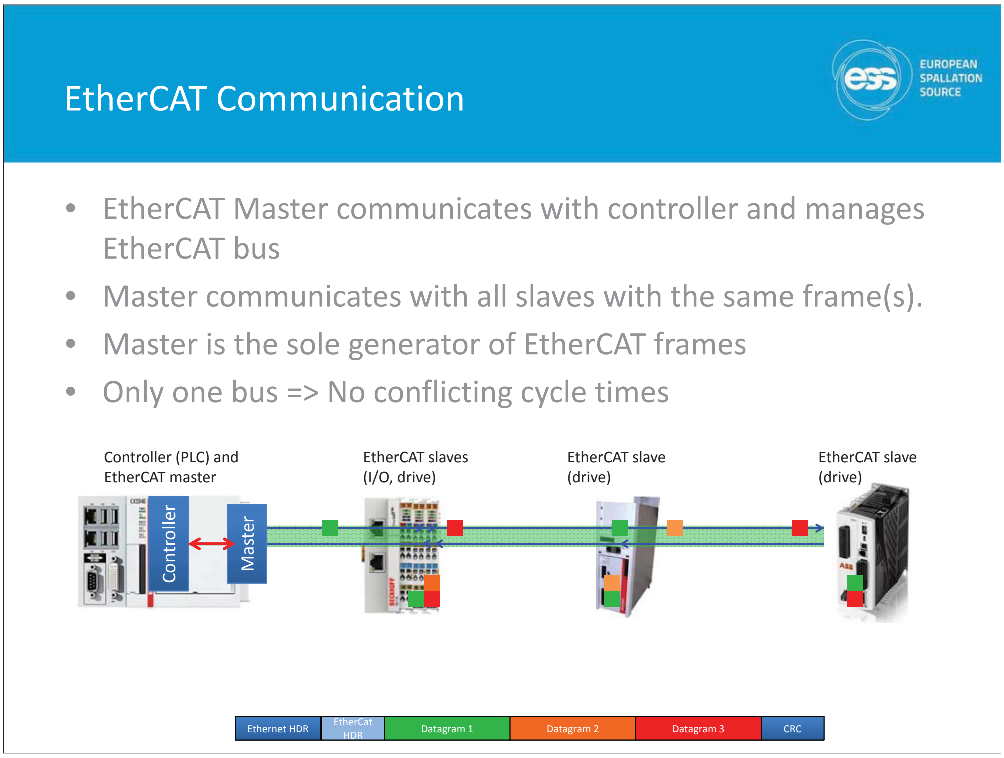
- Modular and scalable (in terms of performance and price)
- Support, spread in community or industry
- Short intervention time (ACC): Diagnostics (preemptive maintenance)
- Short intervention time (ACC): Firmware and parameter management
- Multiple HW platforms (ICS): Open source controller

- Stepper motors, DC brushless, frequency converter, piezo
- Encoder inc. quad., abs. SSI, resolver, (analog), (BiSS-C), (EnDat)



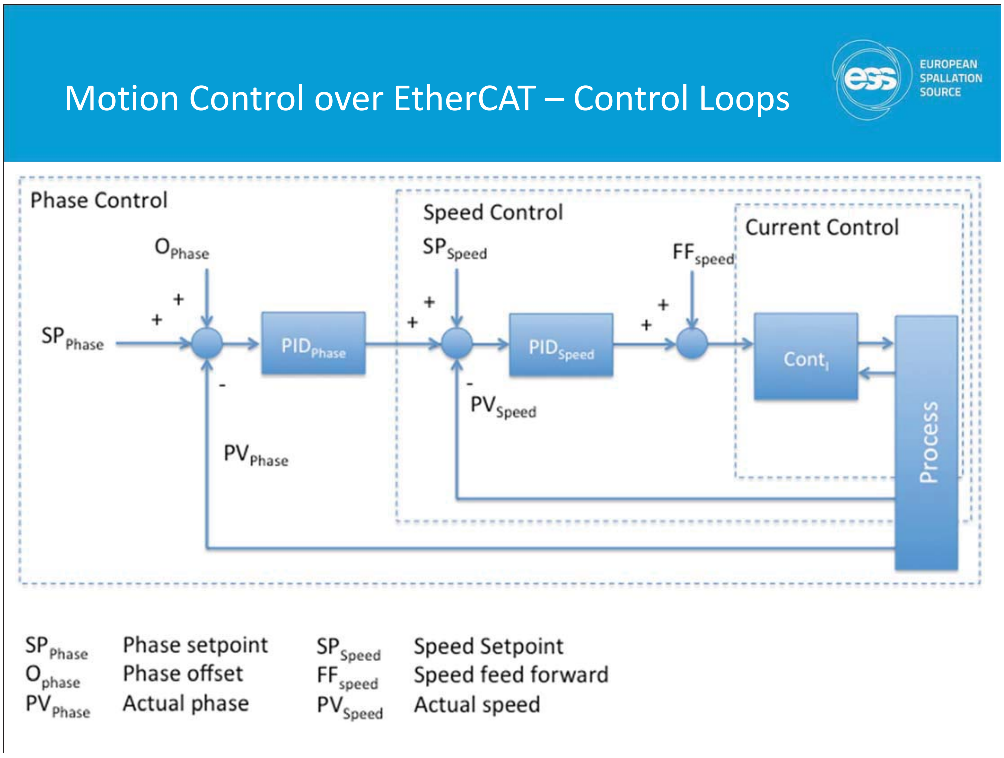
Motion Control over EtherCAT - Topology

- One bus (external + internal), one bus master
- Could cover large distances between single slaves
- Daisy chained ethernet cable, ring topology for redundancy
- Distributed clock system for synchronisation (no extra cable)



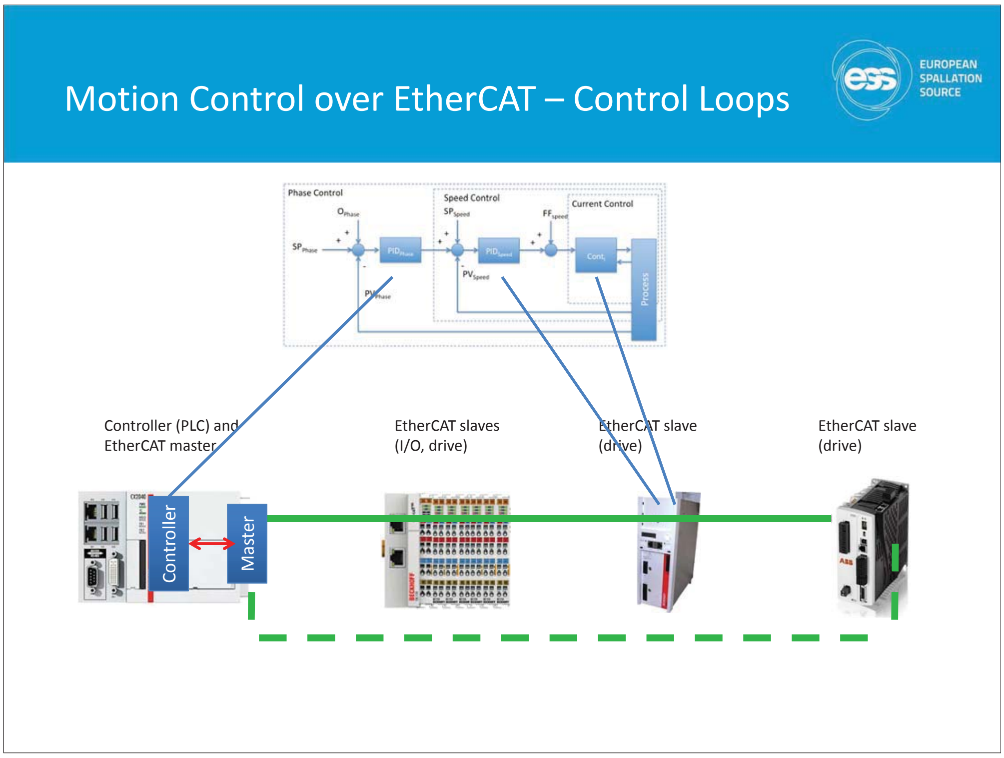
EtherCAT Communication

- EtherCAT Master communicates with controller and manages EtherCAT bus
- Master communicates with all slaves with the same frame(s).
- Master is the sole generator of EtherCAT frames
- Only one bus => No conflicting cycle times



Motion Control over EtherCAT – Control Loops

SP_{Phase}	Phase setpoint	SP_{Speed}	Speed Setpoint
O_{phase}	Phase offset	FF_{speed}	Speed feed forward
PV_{Phase}	Actual phase	PV_{Speed}	Actual speed



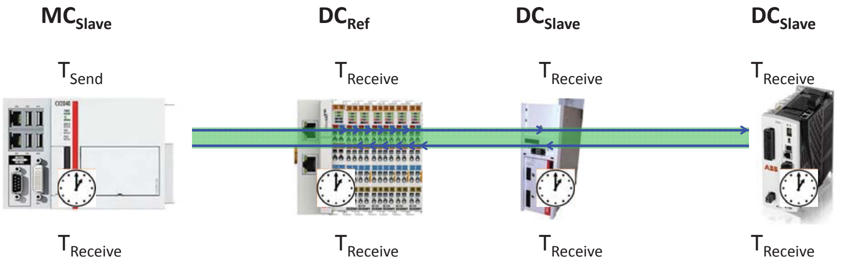
Motion Control over EtherCAT – Control Loops

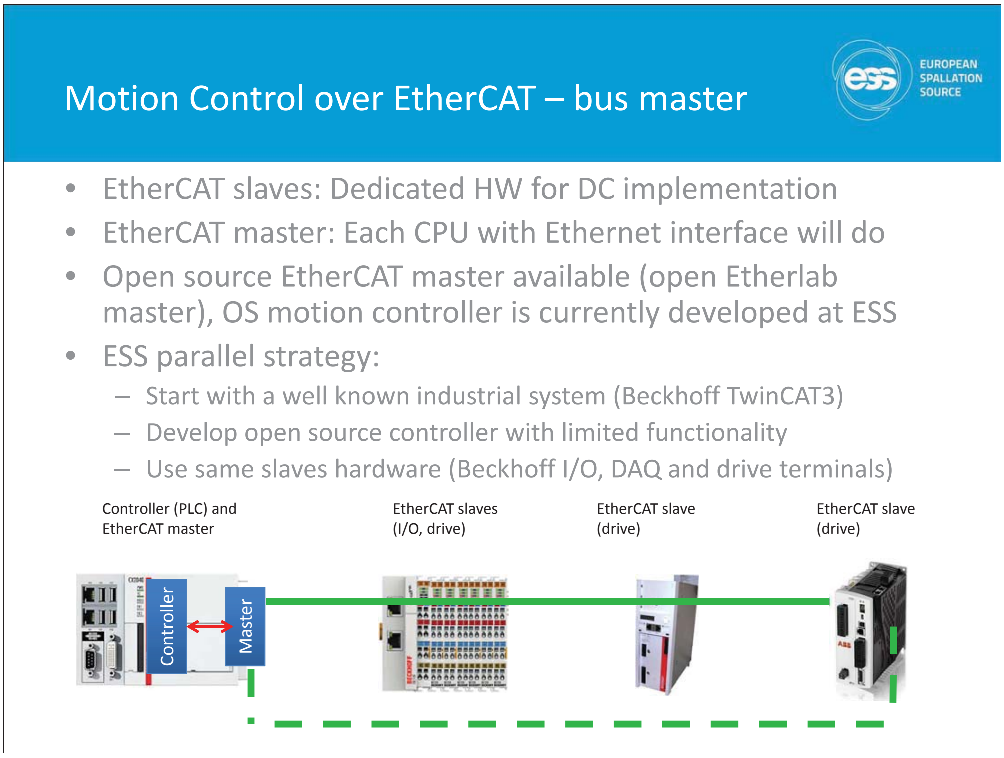
Motion Control over EtherCAT – distributed clocks

- EtherCAT supports use of distributed clocks (DC) in slaves
- DC is not obligatory
- DC is a 64bit nanosecond counter (will overflow after 584 years)
- DC is implemented in ASIC or FPGA in the EtherCAT Slave Controller (ESC) hardware
- Clock in master (MC) to generate frames
- The EtherCAT master is performing synchronization of the DCs and MC.

Internal synchronization of DC

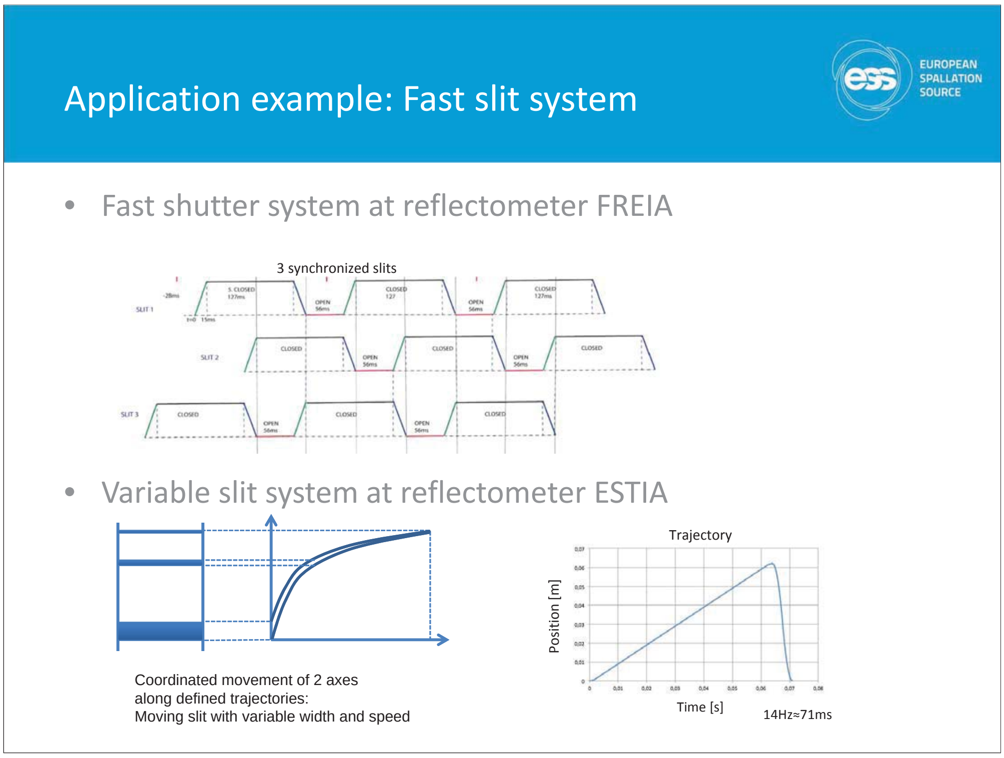
- One DC is selected as reference clock
- EtherCAT master sends synchronization frames to slaves:
  - Delays in network are measured and calculated in master
  - Absolute time of slaves is set by a cyclic procedure (startup procedure approx. 10s)
  - DC slaves and MC are synchronized to DC$_{ref}$ by cyclic synchronization frames (approx. 1Hz). Synch precision < 100 ns, typ. 20 ns





Motion Control over EtherCAT – bus master

- EtherCAT slaves: Dedicated HW for DC implementation
- EtherCAT master: Each CPU with Ethernet interface will do
- Open source EtherCAT master available (open Etherlab master), OS motion controller is currently developed at ESS
- ESS parallel strategy:
  - Start with a well known industrial system (Beckhoff TwinCAT3)
  - Develop open source controller with limited functionality
  - Use same slaves hardware (Beckhoff I/O, DAQ and drive terminals)

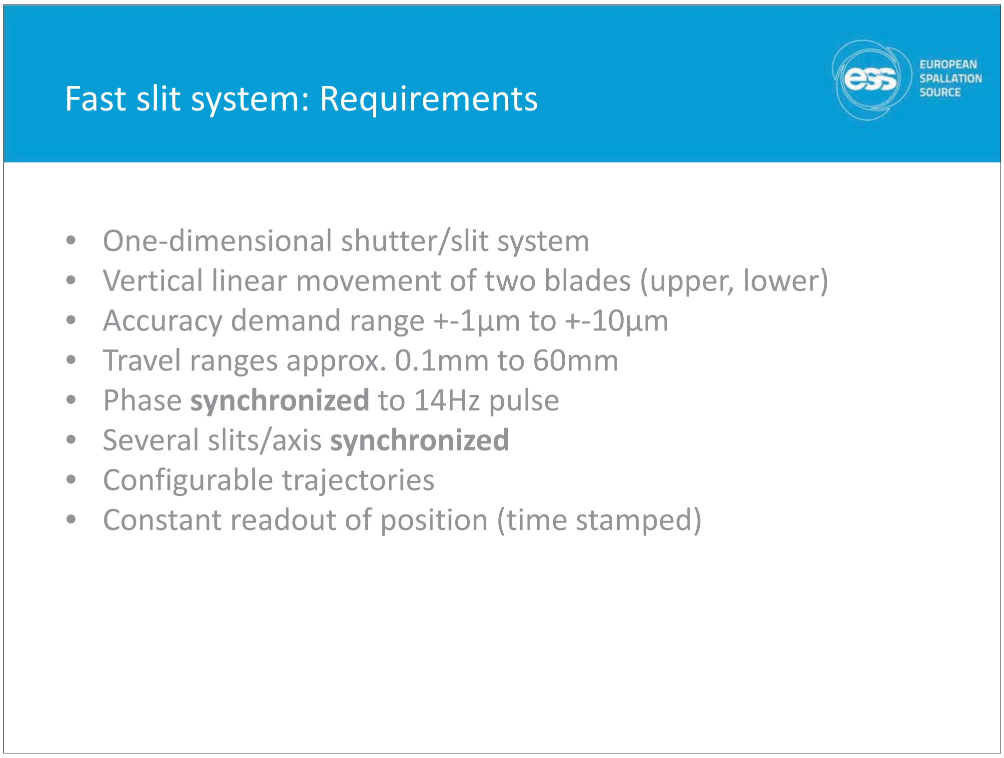


Application example: Fast slit system

- Fast shutter system at reflectometer FREIA

- Variable slit system at reflectometer ESTIA

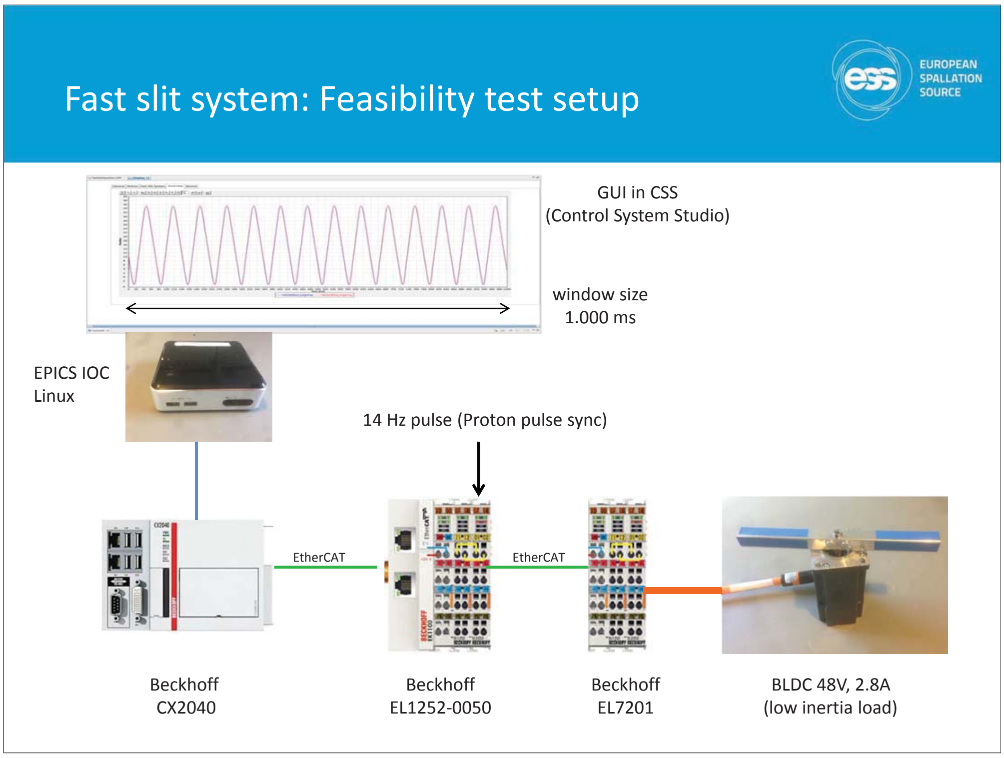
Coordinated movement of 2 axes along defined trajectories:
Moving slit with variable width and speed



Fast slit system: Requirements

EUROPEAN SPALLATION SOURCE

- One-dimensional shutter/slit system
- Vertical linear movement of two blades (upper, lower)
- Accuracy demand range +-1µm to +-10µm
- Travel ranges approx. 0.1mm to 60mm
- Phase **synchronized** to 14Hz pulse
- Several slits/axis **synchronized**
- Configurable trajectories
- Constant readout of position (time stamped)



Fast slit system: Feasibility test setup

EUROPEAN SPALLATION SOURCE

GUI in CSS
(Control System Studio)

window size
1.000 ms

EPICS IOC
Linux

14 Hz pulse (Proton pulse sync)

EtherCAT

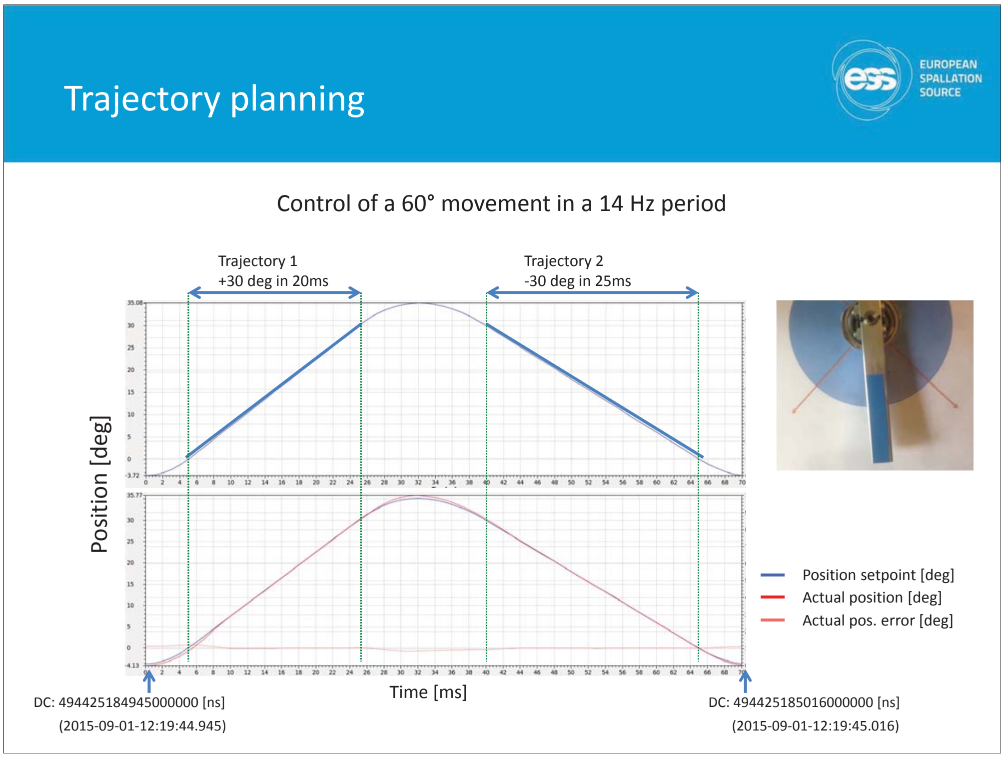
EtherCAT

Beckhoff
CX2040

Beckhoff
EL1252-0050

Beckhoff
EL7201

BLDC 48V, 2.8A
(low inertia load)

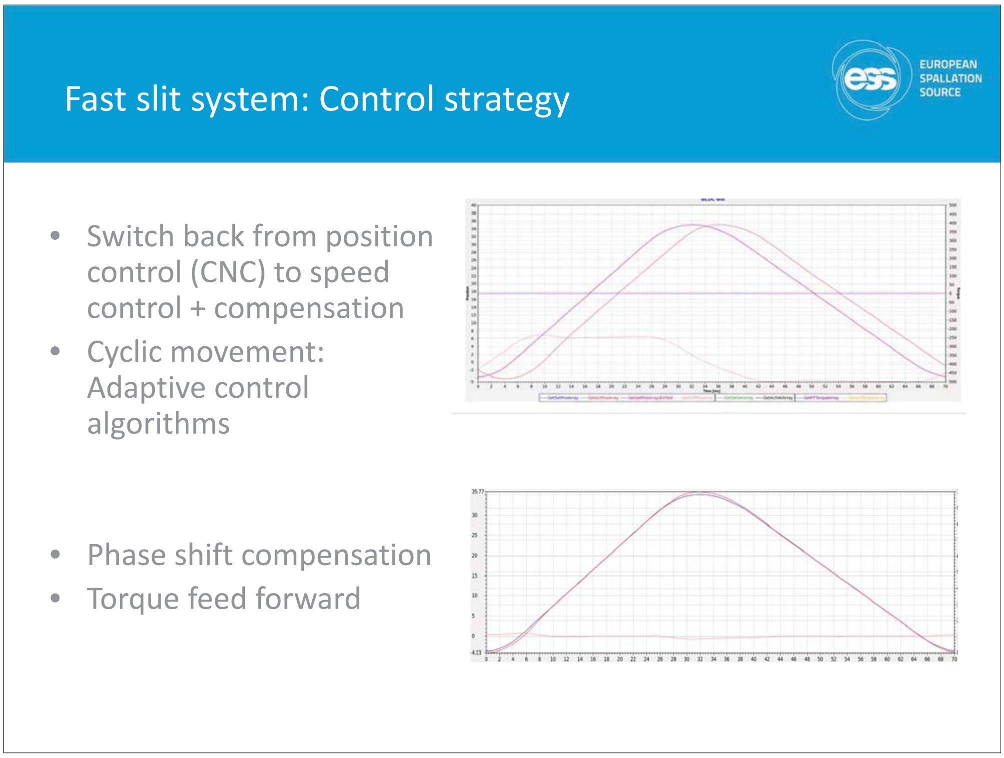


Trajectory planning

Control of a 60° movement in a 14 Hz period

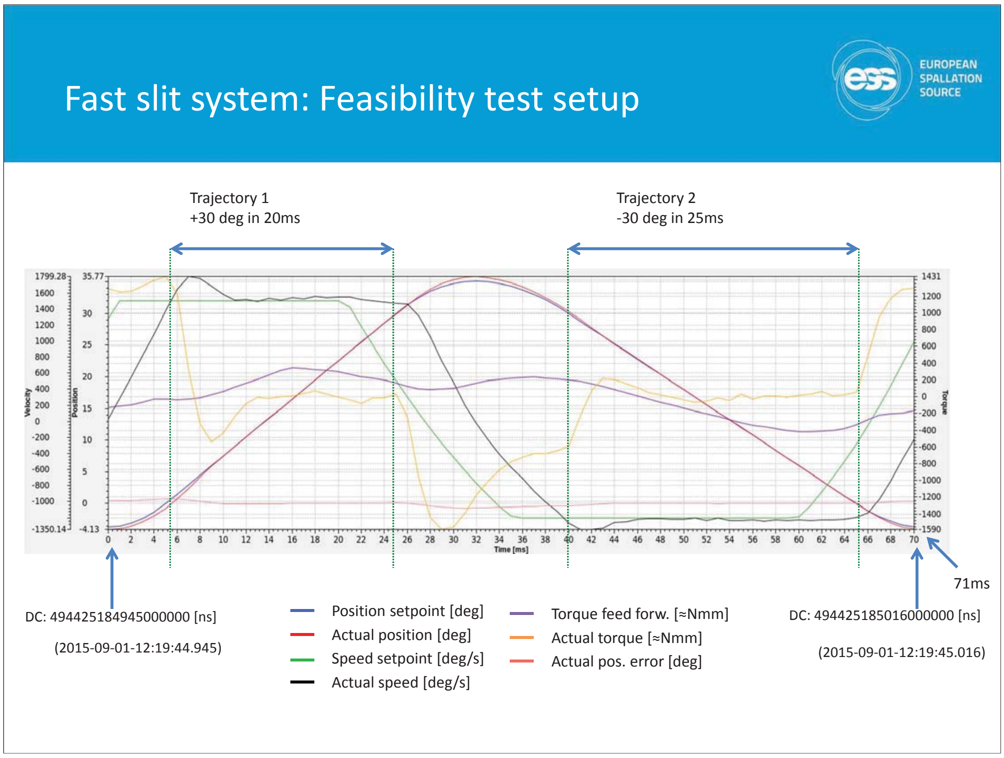
DC: 494425184945000000 [ns]
(2015-09-01-12:19:44.945)

DC: 494425185016000000 [ns]
(2015-09-01-12:19:45.016)



Fast slit system: Control strategy

- Switch back from position control (CNC) to speed control + compensation
- Cyclic movement: Adaptive control algorithms
- Phase shift compensation
- Torque feed forward



Fast slit system: Feasibility test setup

Trajectory 1
+30 deg in 20ms

Trajectory 2
-30 deg in 25ms

71ms

DC: 494425184945000000 [ns]

(2015-09-01-12:19:44.945)

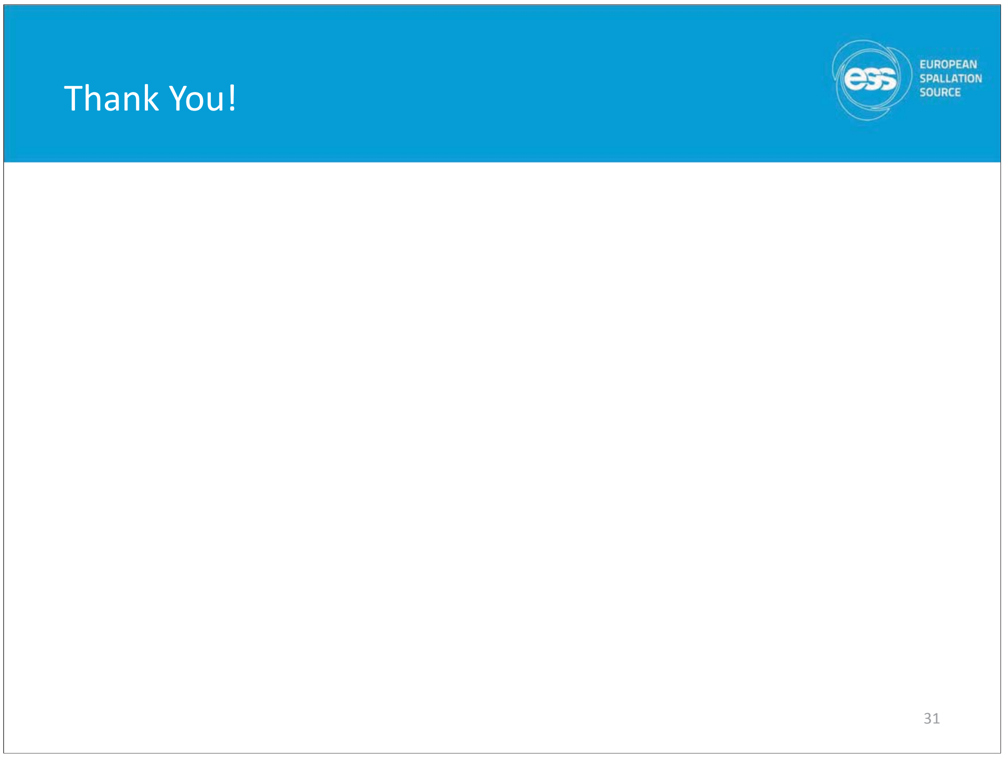
DC: 494425185016000000 [ns]

(2015-09-01-12:19:45.016)

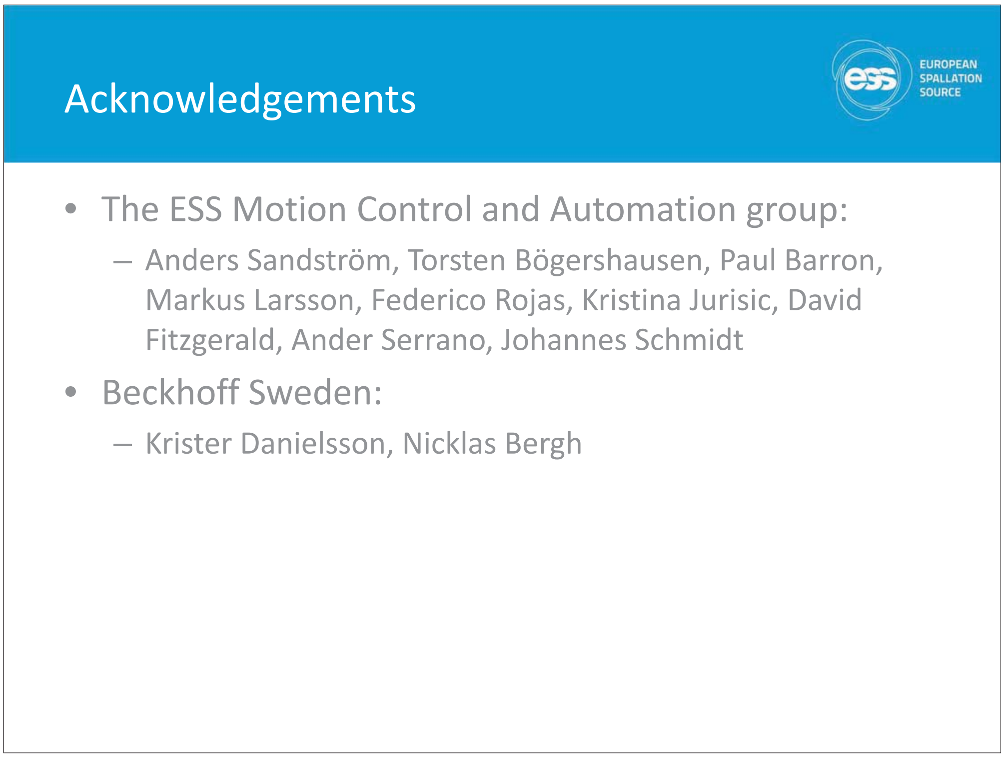
- Position setpoint [deg]
- Actual position [deg]
- Speed setpoint [deg/s]
- Actual speed [deg/s]
- Torque feed forw. [≈Nmm]
- Actual torque [≈Nmm]
- Actual pos. error [deg]

Summary

- The ESS project
  - Collaboration of 17 European countries, 70% in-kind contributions
  - Construction work started, first neutrons in 2019, user op. 2023
  - Pulsed 14Hz neutron spallation source with linear H+ accelerator
  - Modular control concept with EPICS + Timing system as backbone
- Motion Control over EtherCAT
  - Requirements: Distributed and synchronised system, scalable, time stamping, open source bus system, second source
  - EtherCAT looks like the best solution
  - Open source EtherCAT master for long term perspective
- Fast shutter/slit application
  - System to be used at two reflectometers
  - Control concept designed
  - Feasibility study for rotary movement- “proof-of-concept”



Thank You!

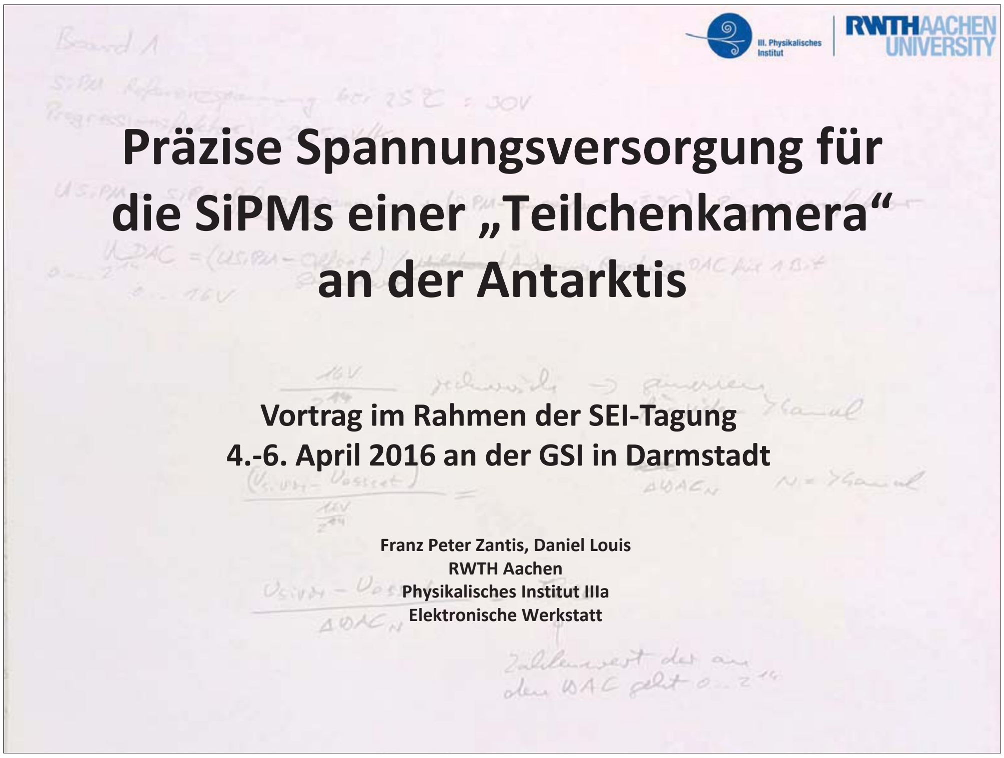


Acknowledgements

- The ESS Motion Control and Automation group:
  - Anders Sandström, Torsten Bögershausen, Paul Barron, Markus Larsson, Federico Rojas, Kristina Jurisic, David Fitzgerald, Ander Serrano, Johannes Schmidt
- Beckhoff Sweden:
  - Krister Danielsson, Nicklas Bergh

References

[1] EtherCAT Technology Group (www.ethercat.org)
[2] Beckhoff Automation GmbH (www.beckhoff.com)
[3] EtherLab (www.etherlab.org)
[4] SOEM (http://sourceforge.net/projects/soem.berlios)
[5] Gunnar Prytz, ABB AS Corporate Research Center: *“A performance analysis of EtherCAT and PROFINET IRT”*
[6] Gianluca Cena, Ivan Cibrario Bertolotti, Stefano Scanzio, Adriano Valenzano, IEIIT–CNR: *“On the Accuracy of the Distributed Clock Mechanism in EtherCAT”*
[7] *Stewart Pullen, ESS:* “Scope of work. Prototype Development of Fast Slit-Shutter Technology”



Präzise Spannungsversorgung für die SiPMs einer „Teilchenkamera“ an der Antarktis

Vortrag im Rahmen der SEI-Tagung
4.-6. April 2016 an der GSI in Darmstadt

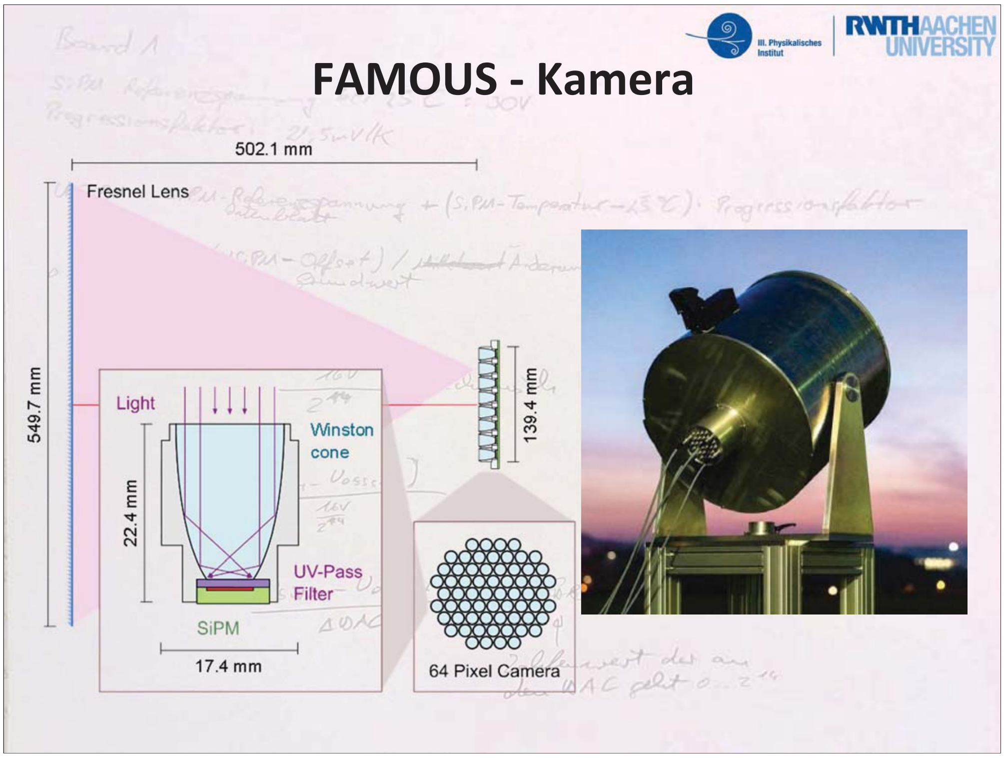
Franz Peter Zantis, Daniel Louis
RWTH Aachen
Physikalisches Institut IIIa
Elektronische Werkstatt

Motivation

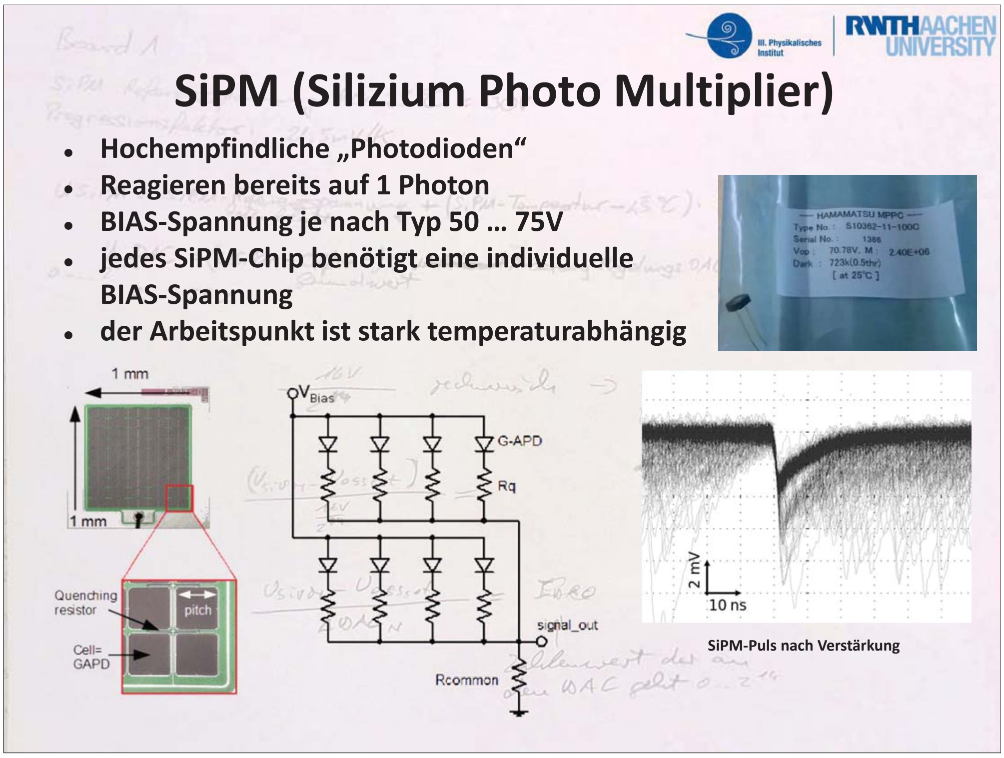
Die Physiker betreiben an einer Station in der Antarktis einen Teilchendetektor „IceCube“.

Wegen der günstigen Randbedingungen (kein Störlicht, klarer Himmer, etc.) soll an dieser Station auch eine „Teilchenkamera“ aus dem Projekt „FAMOUS“1 aufgestellt werden, die mit SiPMs (Silizium Photo Multiplier) bestückt ist.
Die Kamera ist seit Dezember 2015 in Betrieb.

1„First Auger Multi-pixel-photon-counter-camera for the Observation of Ultra-high-energy-cosmic-ray air Showers”



FAMOUS - Kamera

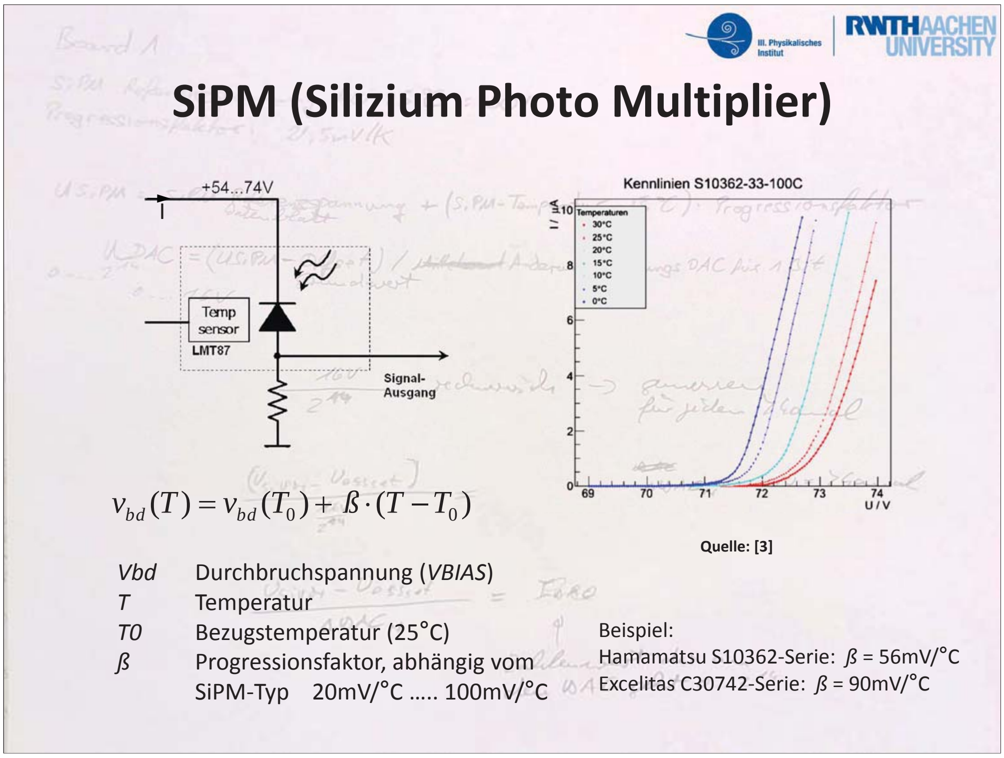


SiPM (Silizium Photo Multiplier)

- **Hochempfindliche „Photodioden“**
- **Reagieren bereits auf 1 Photon**
- **BIAS-Spannung je nach Typ 50 … 75V**
- **jedes SiPM-Chip benötigt eine individuelle BIAS-Spannung**
- **der Arbeitspunkt ist stark temperaturabhängig**

— HAMAMATSU MPPC —
Type No. : S10362-11-100C
Serial No. : 1386
Vop : 70.78V, M : 2.40E+06
Dark : 723k(0.5thr)
[at 25°C]

SiPM-Puls nach Verstärkung



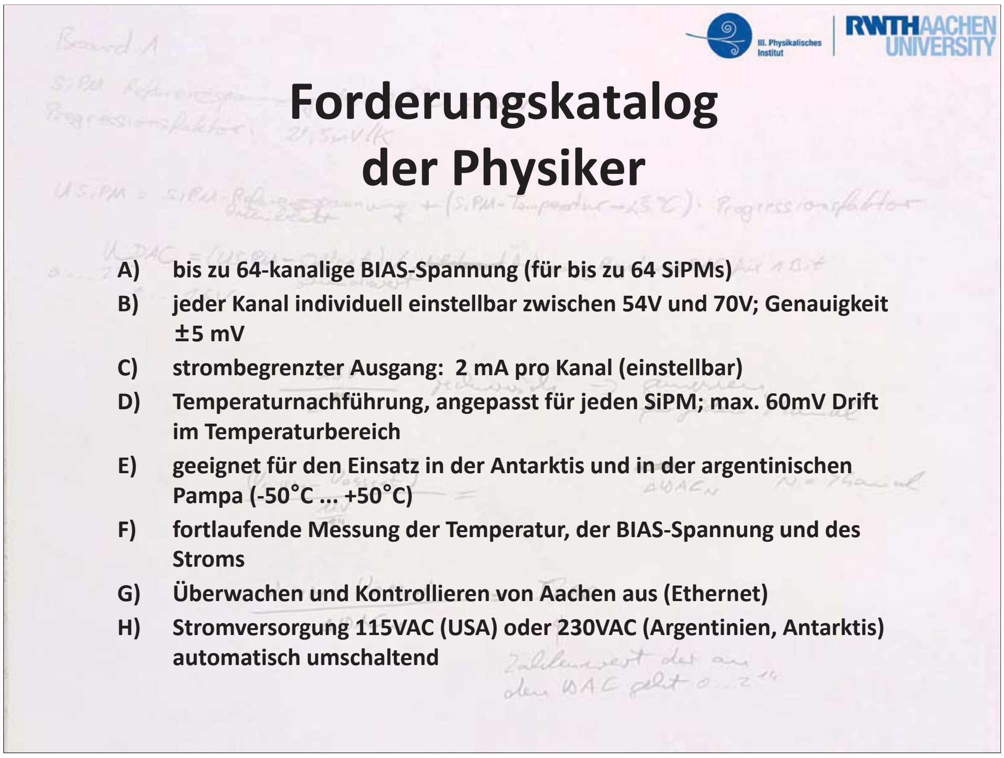
SiPM (Silizium Photo Multiplier)

$$v_{bd}(T) = v_{bd}(T_0) + ß \cdot (T - T_0)$$

Quelle: [3]

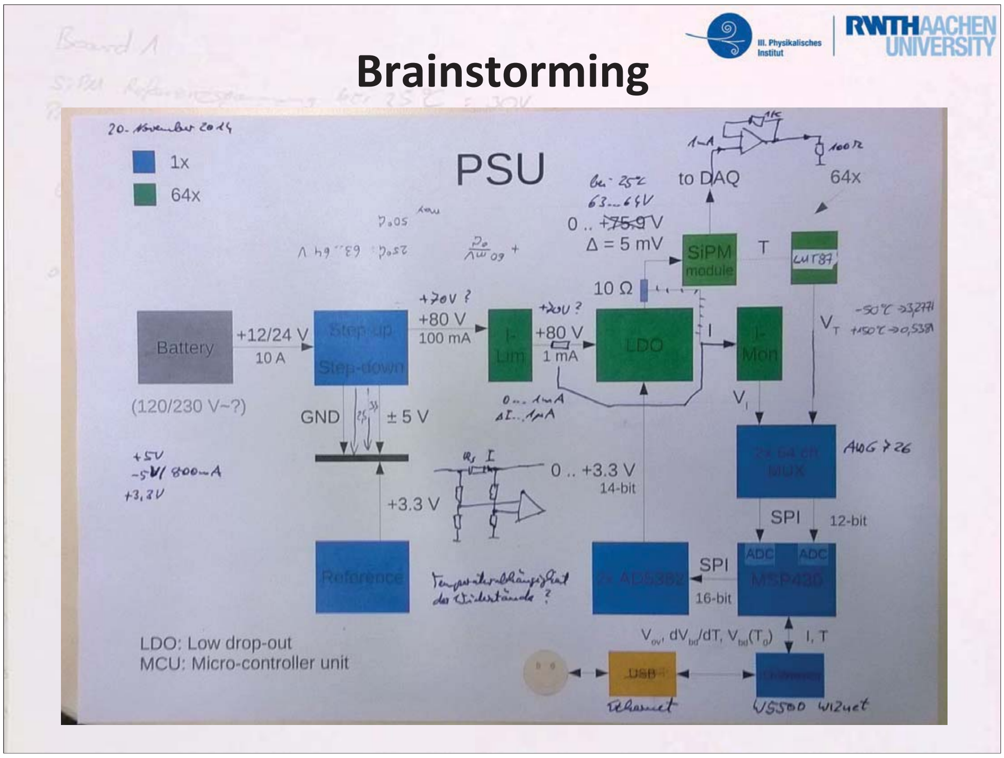
Vbd	Durchbruchspannung (*VBIAS*)
T	Temperatur
T0	Bezugstemperatur (25°C)
ß	Progressionsfaktor, abhängig vom SiPM-Typ 20mV/°C ..... 100mV/°C

Beispiel:
Hamamatsu S10362-Serie: *ß* = 56mV/°C
Excelitas C30742-Serie: *ß* = 90mV/°C

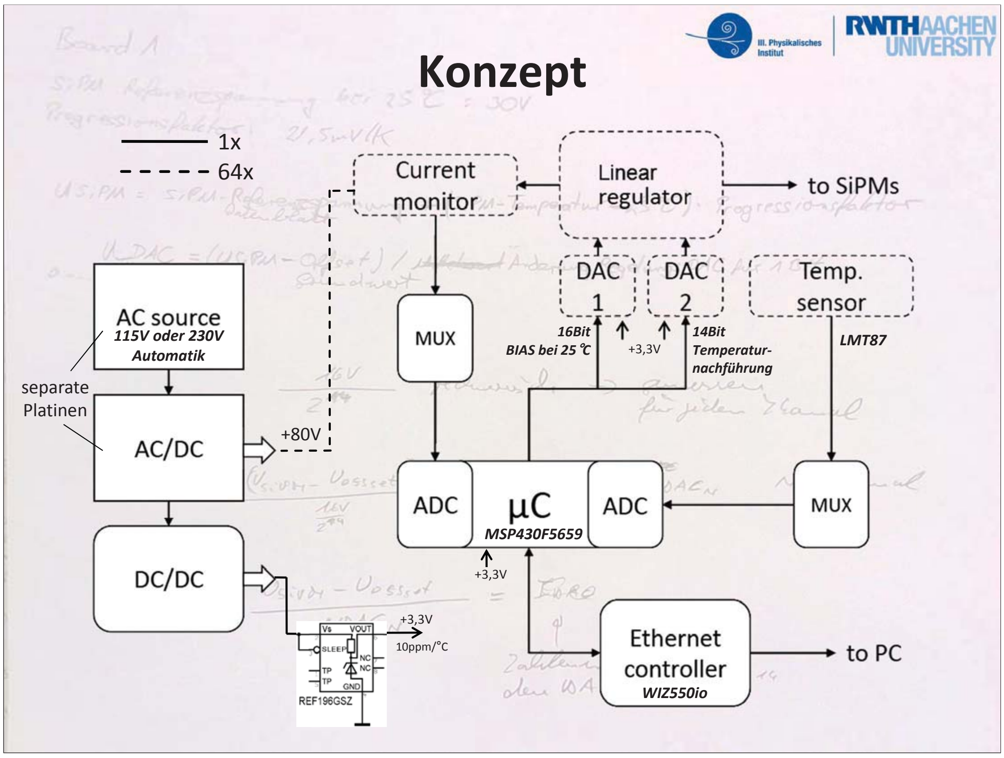


Forderungskatalog der Physiker

- **A) bis zu 64-kanalige BIAS-Spannung (für bis zu 64 SiPMs)**
- **B) jeder Kanal individuell einstellbar zwischen 54V und 70V; Genauigkeit ±5 mV**
- **C) strombegrenzter Ausgang: 2 mA pro Kanal (einstellbar)**
- **D) Temperaturnachführung, angepasst für jeden SiPM; max. 60mV Drift im Temperaturbereich**
- **E) geeignet für den Einsatz in der Antarktis und in der argentinischen Pampa (-50°C ... +50°C)**
- **F) fortlaufende Messung der Temperatur, der BIAS-Spannung und des Stroms**
- **G) Überwachen und Kontrollieren von Aachen aus (Ethernet)**
- **H) Stromversorgung 115VAC (USA) oder 230VAC (Argentinien, Antarktis) automatisch umschaltend**

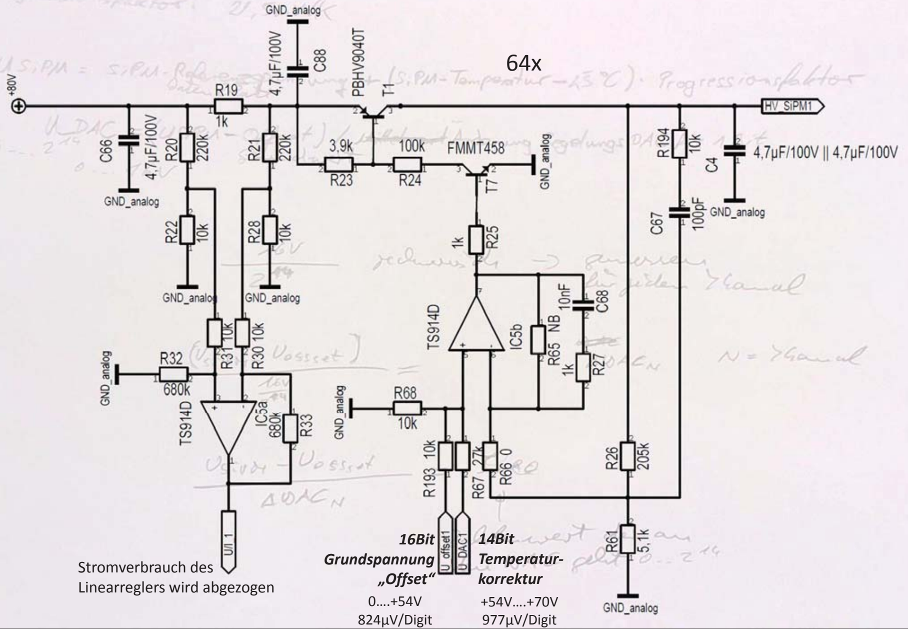


Brainstorming



Konzept

Linearregler/Stellglied und Strommonitor



Stromverbrauch des
Linearreglers wird abgezogen

16Bit Grundspannung „Offset“
0….+54V
824µV/Digit

14Bit Temperatur-korrektur
+54V….+70V
977µV/Digit

Maßnahmen zur Erreichung der Genauigkeit in der Hardware

Grund-genauigkeit

- **alle relevanten Widerstände mit ±0,1% und ±25ppm/°C**
- **Versorgung von µC/ADU und DAC über Spannungsreferenzen mit 10ppm/°C**

Genauigkeit der Temperatur-nachführung

- **Temperatursensoren LMT87 mit einer Genauigkeit von ±0,3°C für jeden SiPM**

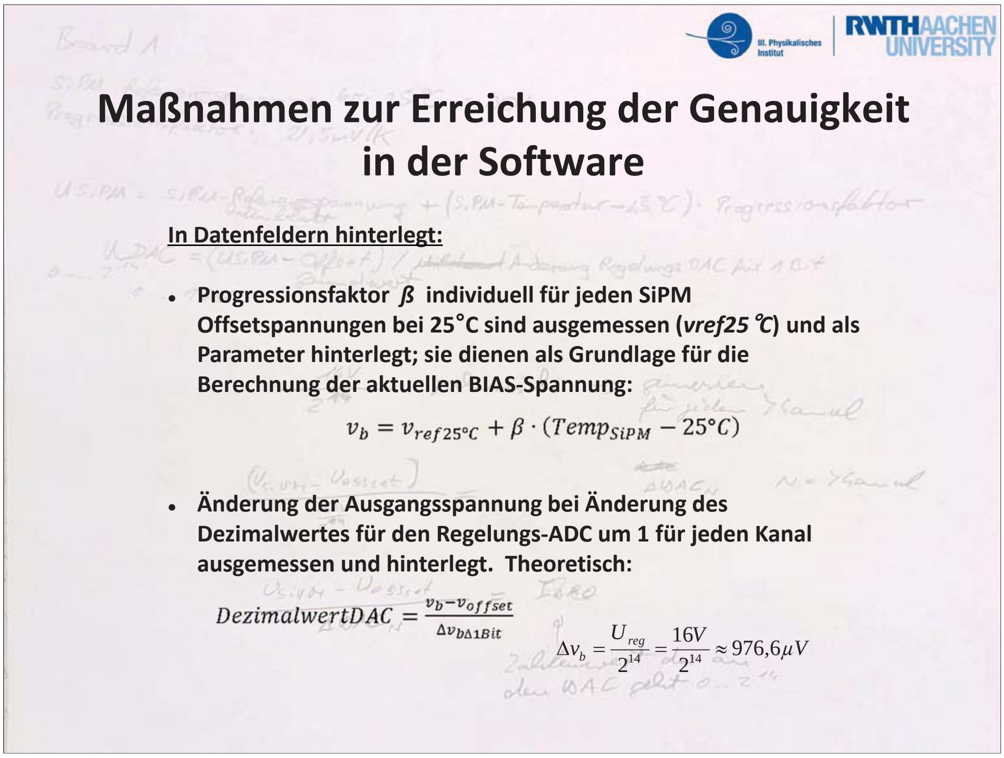
$$V_{TEMP}[mV] = 2230{,}8mV - \left[13{,}582\,\frac{mV}{°C}\cdot(T-30°C)\right] - \left[0{,}00433\,\frac{mV}{°C^2}\cdot(T-30°C)^2\right]$$

UTEMP = f(T) ist insgesamt sehr linear; der quadratische Anteil ist nur klein

$$\frac{T}{°C} = \frac{13{,}582 - \sqrt{(-13{,}582)^2 + 4\cdot 0{,}00433\cdot(2230{,}8 - V_{TEMP}[mV])}}{2\cdot(-0{,}00433)} + 30$$

nach Erfassung mit dem 12-Bit-ADC des µC (*Uref = 3,3V*):

$$\frac{T}{°C} = -0{,}0604 \cdot Dezimalwert_{ADC} + 197{,}81$$



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Maßnahmen zur Erreichung der Genauigkeit in der Software

In Datenfeldern hinterlegt:

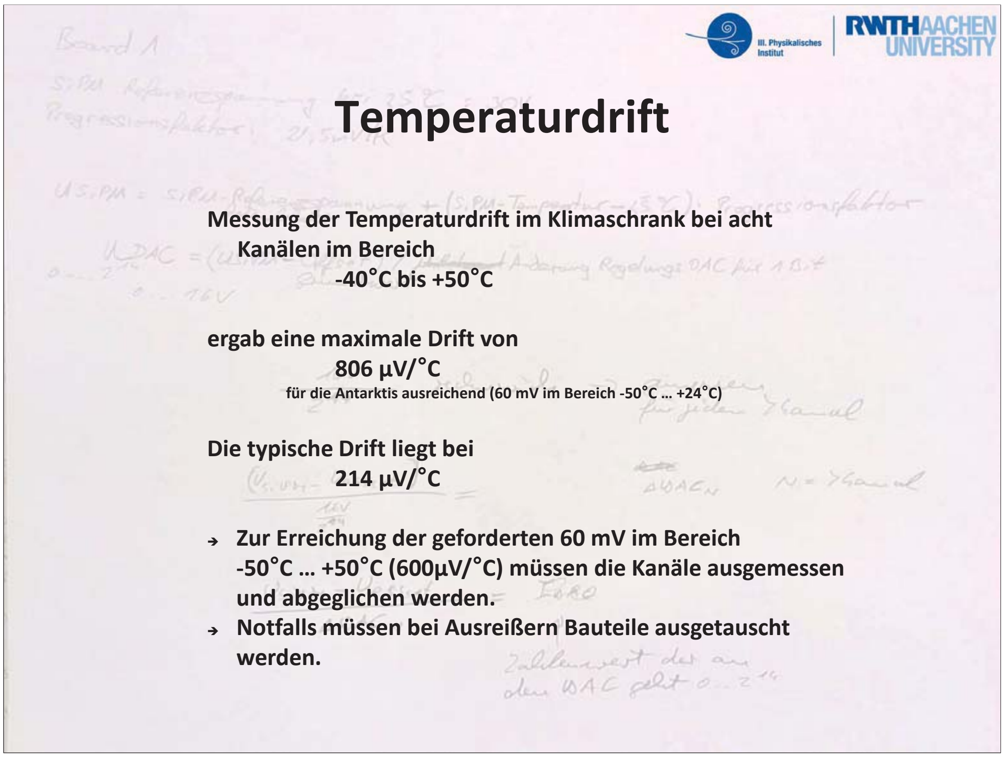
- **Progressionsfaktor *ß* individuell für jeden SiPM Offsetspannungen bei 25°C sind ausgemessen (*vref25 ℃*) und als Parameter hinterlegt; sie dienen als Grundlage für die Berechnung der aktuellen BIAS-Spannung:**

$$v_b = v_{ref25°C} + \beta \cdot (Temp_{SiPM} - 25°C)$$

- **Änderung der Ausgangsspannung bei Änderung des Dezimalwertes für den Regelungs-ADC um 1 für jeden Kanal ausgemessen und hinterlegt. Theoretisch:**

$$DezimalwertDAC = \frac{v_b - v_{offset}}{\Delta v_{b\Delta 1Bit}}$$

$$\Delta v_b = \frac{U_{reg}}{2^{14}} = \frac{16V}{2^{14}} \approx 976{,}6\mu V$$



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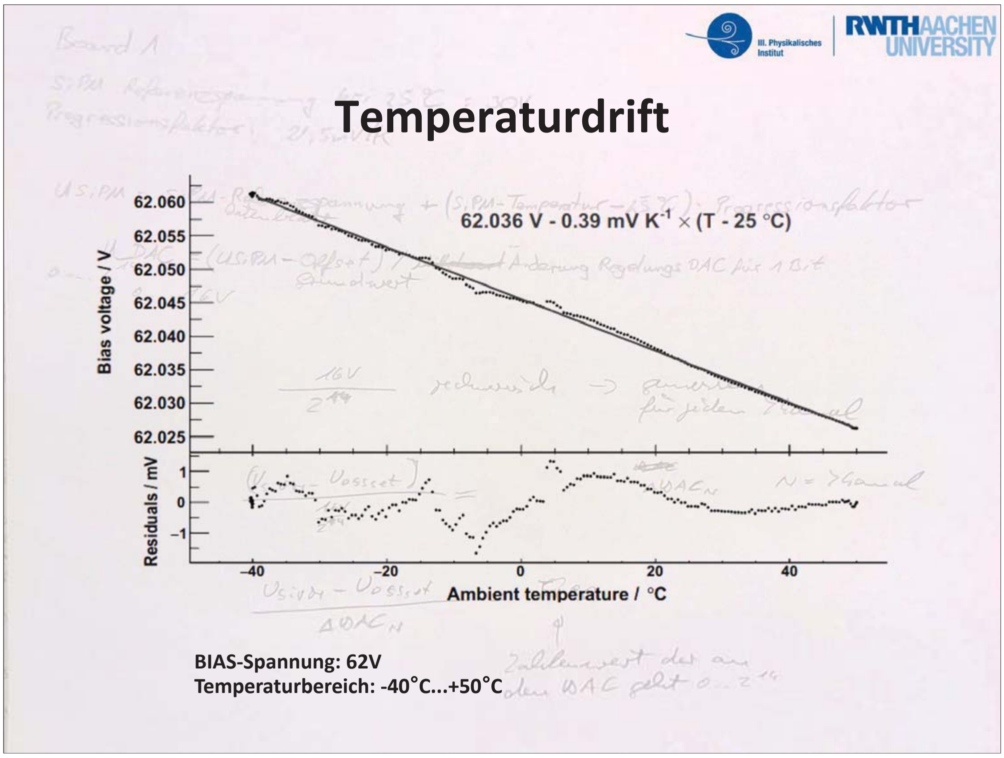
Temperaturdrift

Messung der Temperaturdrift im Klimaschrank bei acht Kanälen im Bereich
-40°C bis +50°C

ergab eine maximale Drift von
806 µV/°C
für die Antarktis ausreichend (60 mV im Bereich -50°C … +24°C)

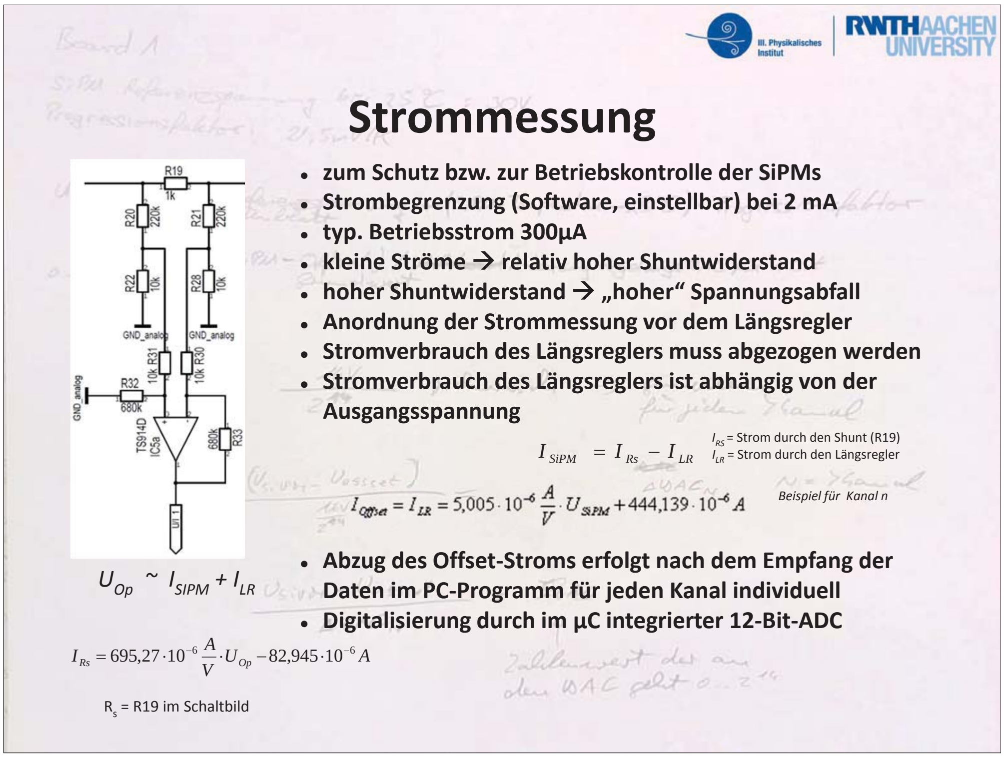
Die typische Drift liegt bei
214 µV/°C

- **→ Zur Erreichung der geforderten 60 mV im Bereich -50°C … +50°C (600µV/°C) müssen die Kanäle ausgemessen und abgeglichen werden.**
- **→ Notfalls müssen bei Ausreißern Bauteile ausgetauscht werden.**



Temperaturdrift

BIAS-Spannung: 62V
Temperaturbereich: -40°C...+50°C



Strommessung

- **zum Schutz bzw. zur Betriebskontrolle der SiPMs**
- **Strombegrenzung (Software, einstellbar) bei 2 mA**
- **typ. Betriebsstrom 300µA**
- **kleine Ströme → relativ hoher Shuntwiderstand**
- **hoher Shuntwiderstand → „hoher“ Spannungsabfall**
- **Anordnung der Strommessung vor dem Längsregler**
- **Stromverbrauch des Längsreglers muss abgezogen werden**
- **Stromverbrauch des Längsreglers ist abhängig von der Ausgangsspannung**

$$I_{SiPM} = I_{Rs} - I_{LR}$$

I_{RS} = Strom durch den Shunt (R19)
I_{LR} = Strom durch den Längsregler

$$I_{Offset} = I_{LR} = 5{,}005 \cdot 10^{-6} \frac{A}{V} \cdot U_{SiPM} + 444{,}139 \cdot 10^{-6} A$$

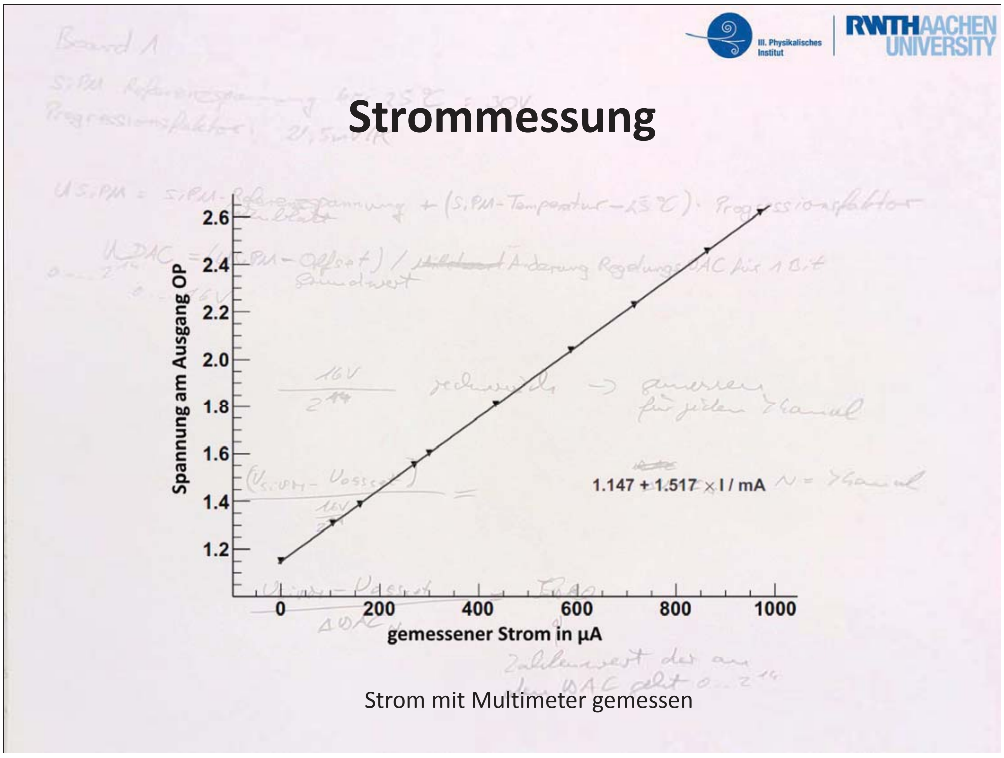
Beispiel für Kanal n

$$U_{Op} \sim I_{SIPM} + I_{LR}$$

- **Abzug des Offset-Stroms erfolgt nach dem Empfang der Daten im PC-Programm für jeden Kanal individuell**
- **Digitalisierung durch im µC integrierter 12-Bit-ADC**

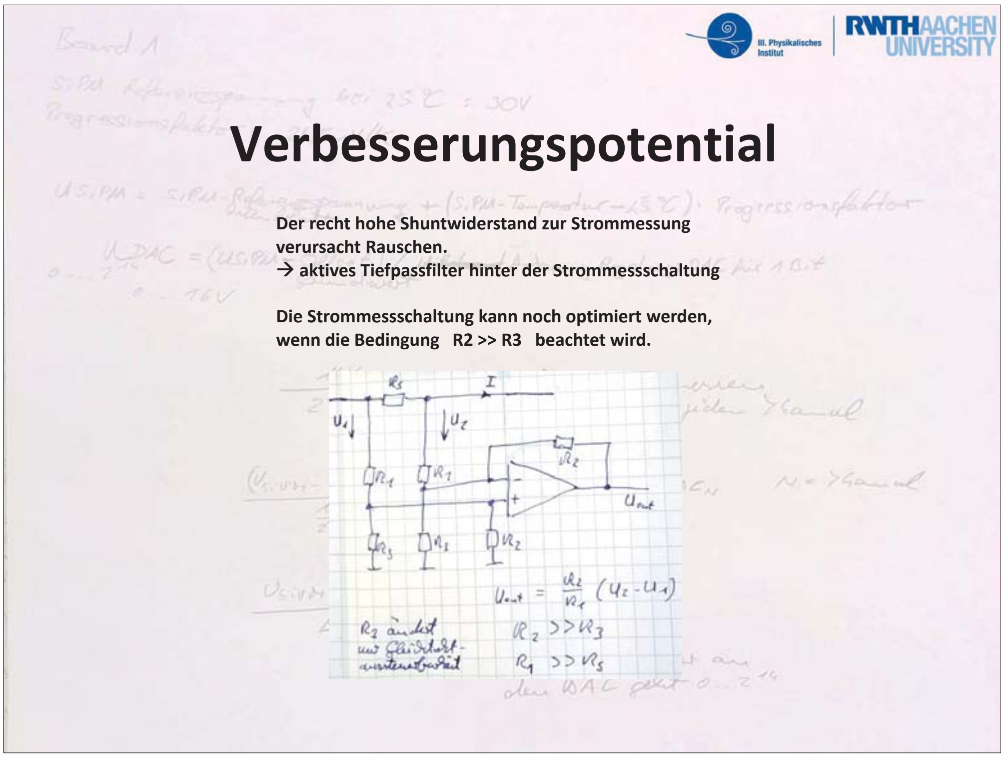
$$I_{Rs} = 695{,}27 \cdot 10^{-6} \frac{A}{V} \cdot U_{Op} - 82{,}945 \cdot 10^{-6} A$$

R_s = R19 im Schaltbild



Strommessung

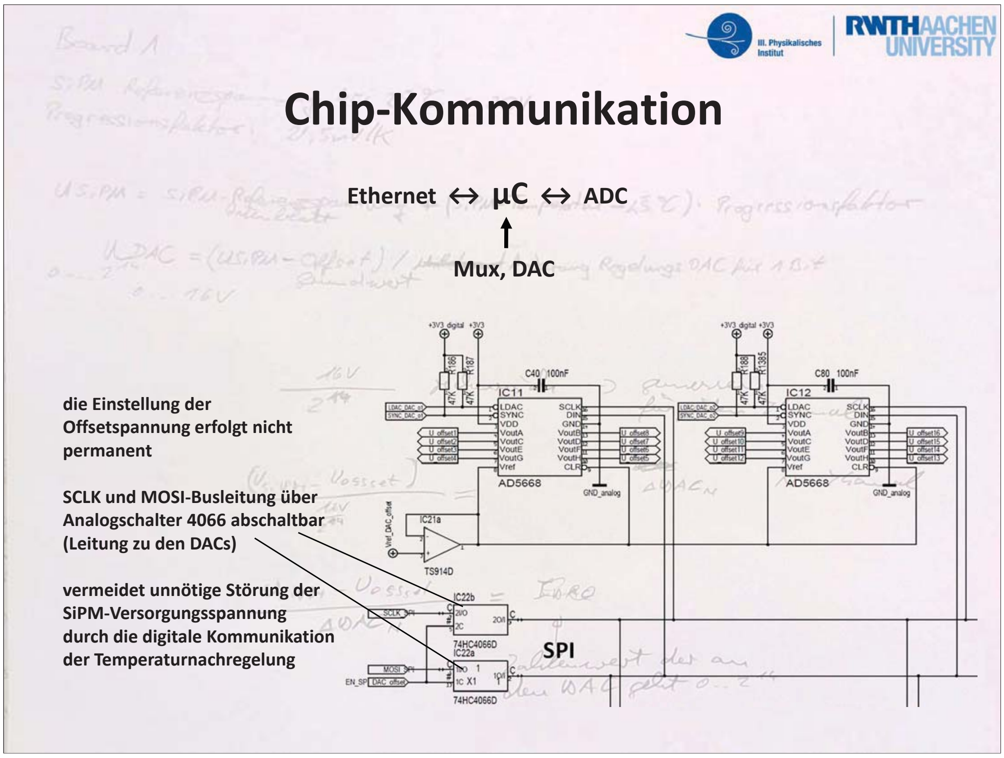
Strom mit Multimeter gemessen



Verbesserungspotential

Der recht hohe Shuntwiderstand zur Strommessung verursacht Rauschen.
→ aktives Tiefpassfilter hinter der Strommessschaltung

Die Strommessschaltung kann noch optimiert werden, wenn die Bedingung R2 >> R3 beachtet wird.



Chip-Kommunikation

Ethernet ↔ µC ↔ ADC

↑

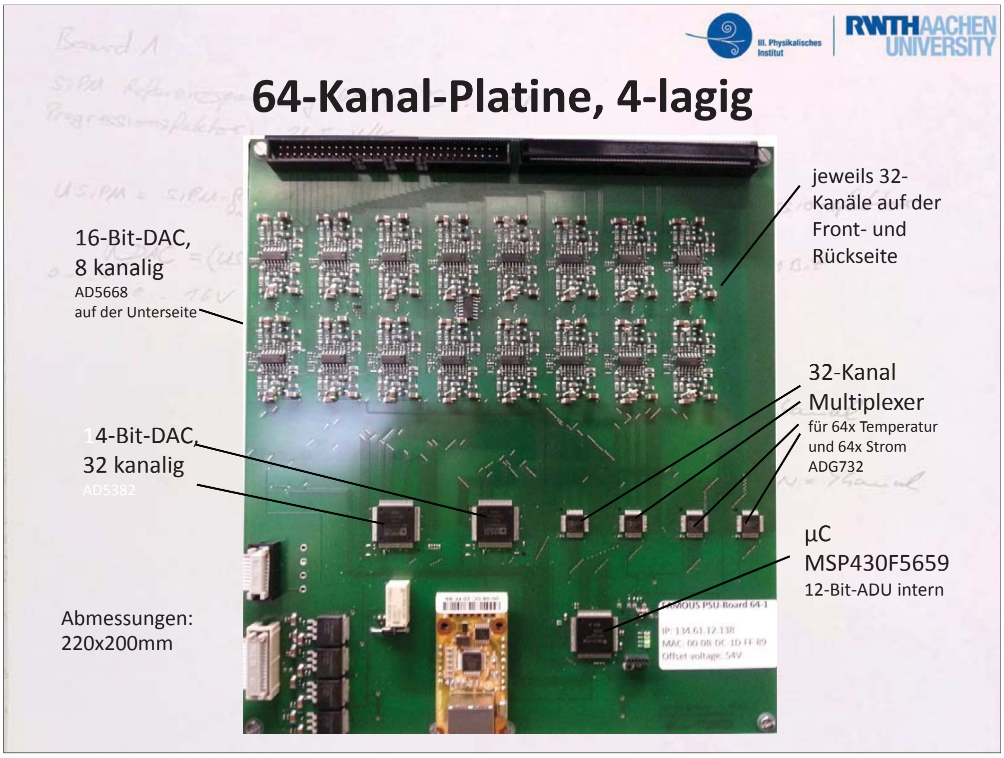
Mux, DAC

die Einstellung der Offsetspannung erfolgt nicht permanent

SCLK und MOSI-Busleitung über Analogschalter 4066 abschaltbar (Leitung zu den DACs)

vermeidet unnötige Störung der SiPM-Versorgungsspannung durch die digitale Kommunikation der Temperaturnachregelung

SPI



64-Kanal-Platine, 4-lagig

16-Bit-DAC,
8 kanalig
AD5668
auf der Unterseite

14-Bit-DAC,
32 kanalig
AD5382

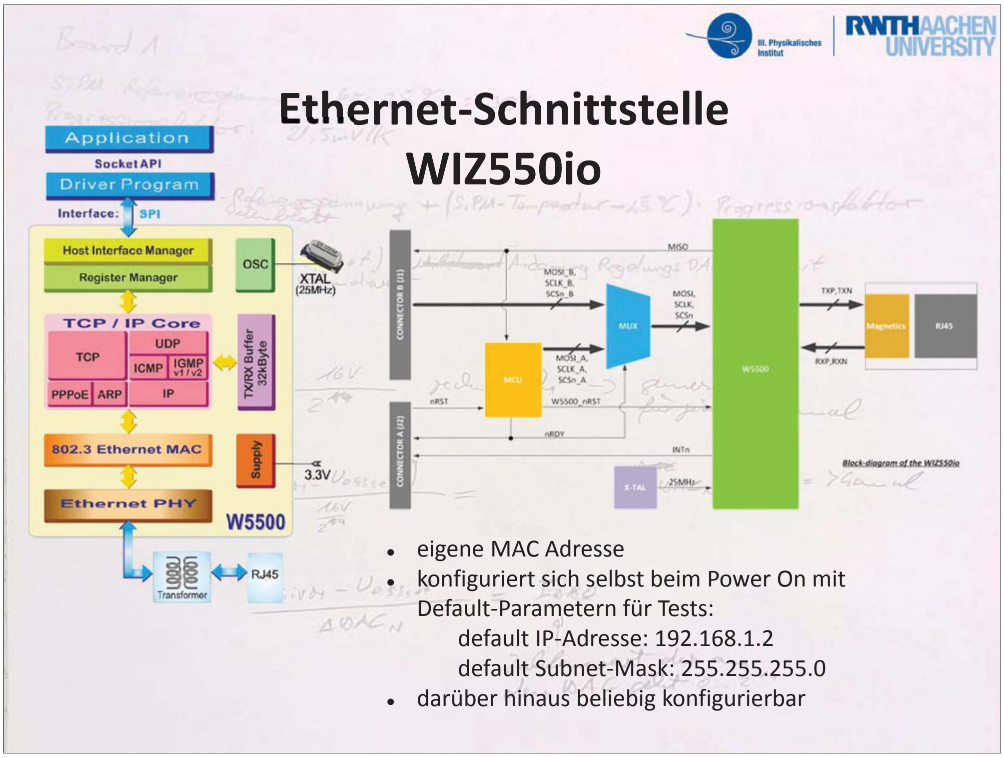
Abmessungen:
220x200mm

jeweils 32-Kanäle auf der Front- und Rückseite

32-Kanal Multiplexer
für 64x Temperatur und 64x Strom
ADG732

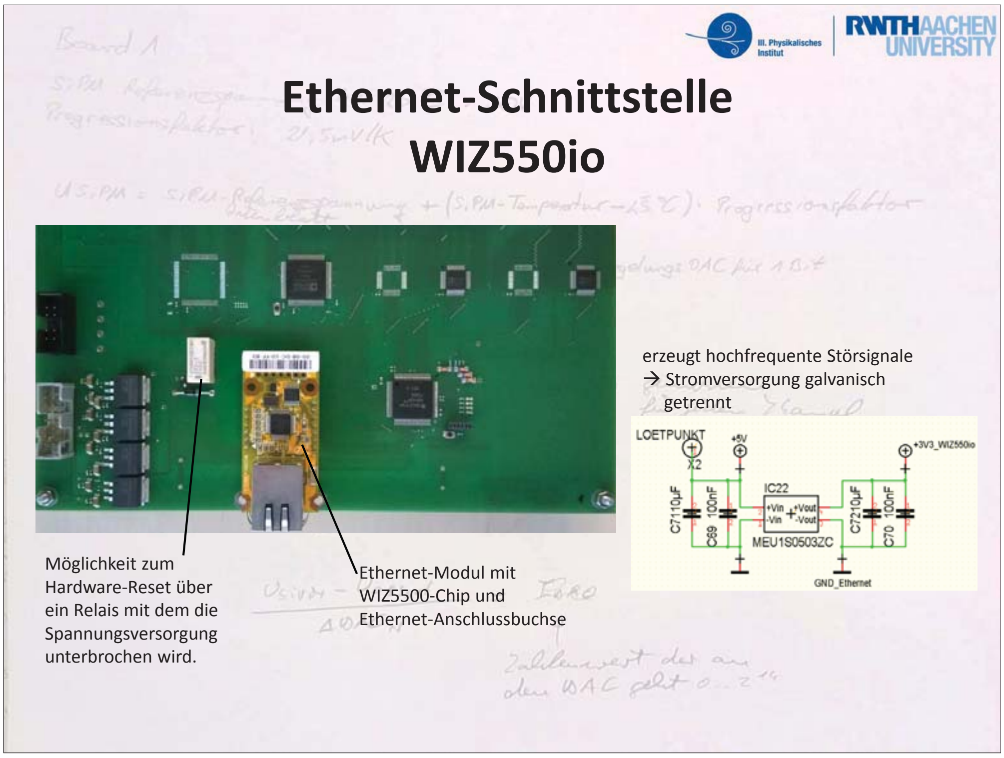
µC
MSP430F5659
12-Bit-ADU intern

FAMOUS PSU-Board 64-1
IP: 134.61.12.138
MAC: 00-08-DC-1D-FF-89
Offset voltage: 54V



Ethernet-Schnittstelle WIZ550io

- eigene MAC Adresse
- konfiguriert sich selbst beim Power On mit Default-Parametern für Tests:
  - default IP-Adresse: 192.168.1.2
  - default Subnet-Mask: 255.255.255.0
- darüber hinaus beliebig konfigurierbar

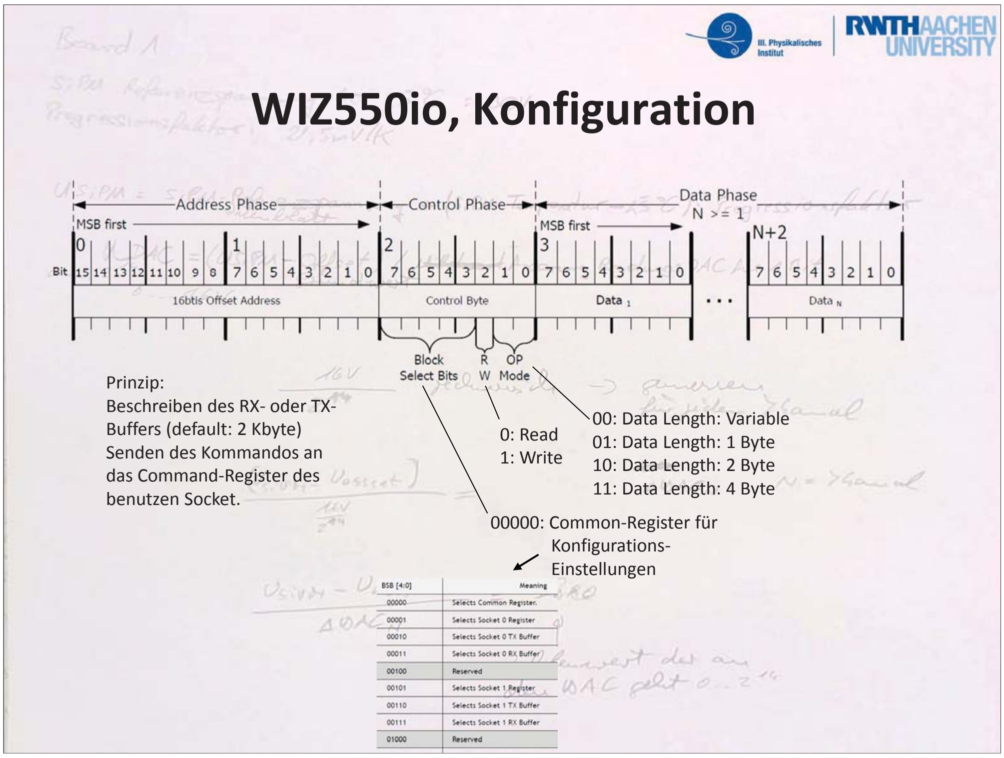


Ethernet-Schnittstelle WIZ550io

erzeugt hochfrequente Störsignale
→ Stromversorgung galvanisch getrennt

Möglichkeit zum Hardware-Reset über ein Relais mit dem die Spannungsversorgung unterbrochen wird.

Ethernet-Modul mit WIZ5500-Chip und Ethernet-Anschlussbuchse



WIZ550io, Konfiguration

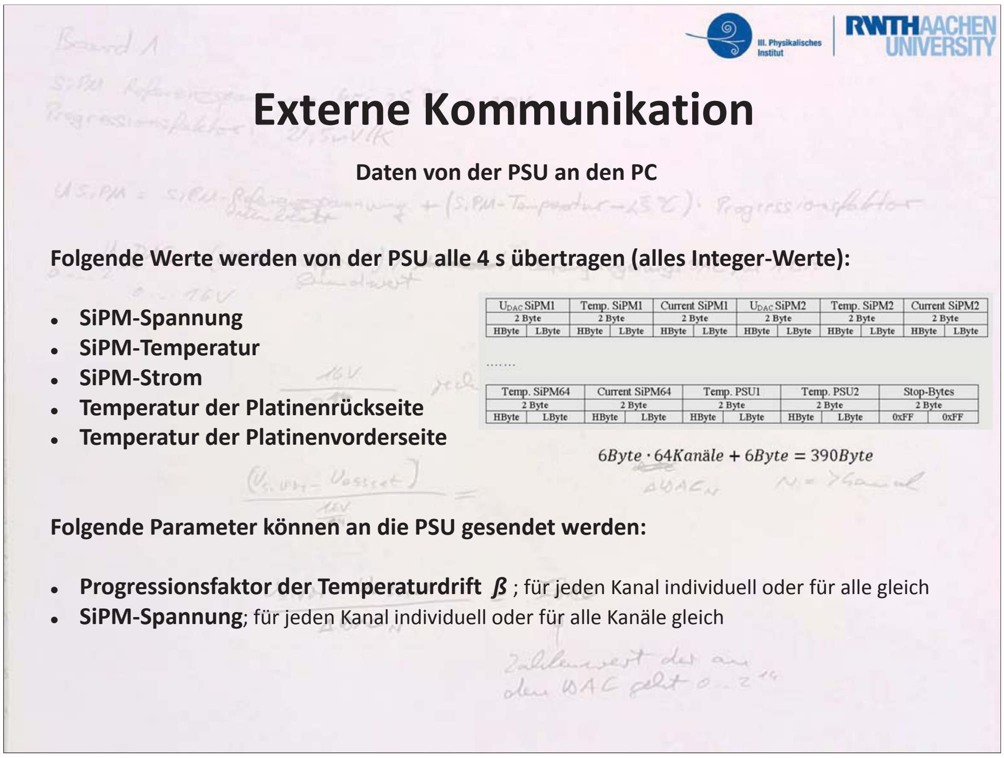
Prinzip:
Beschreiben des RX- oder TX-Buffers (default: 2 Kbyte)
Senden des Kommandos an das Command-Register des benutzen Socket.

0: Read
1: Write

00: Data Length: Variable
01: Data Length: 1 Byte
10: Data Length: 2 Byte
11: Data Length: 4 Byte

00000: Common-Register für Konfigurations-Einstellungen

BSB [4:0]	Meaning
00000	Selects Common Register.
00001	Selects Socket 0 Register
00010	Selects Socket 0 TX Buffer
00011	Selects Socket 0 RX Buffer
00100	Reserved
00101	Selects Socket 1 Register
00110	Selects Socket 1 TX Buffer
00111	Selects Socket 1 RX Buffer
01000	Reserved



Externe Kommunikation

Daten von der PSU an den PC

Folgende Werte werden von der PSU alle 4 s übertragen (alles Integer-Werte):

- **SiPM-Spannung**
- **SiPM-Temperatur**
- **SiPM-Strom**
- **Temperatur der Platinenrückseite**
- **Temperatur der Platinenvorderseite**

U_{DAC} SiPM1		Temp. SiPM1		Current SiPM1		U_{DAC} SiPM2		Temp. SiPM2		Current SiPM2	
2 Byte		2 Byte		2 Byte		2 Byte		2 Byte		2 Byte	
HByte	LByte	HByte	LByte	HByte	LByte	HByte	LByte	HByte	LByte	HByte	LByte

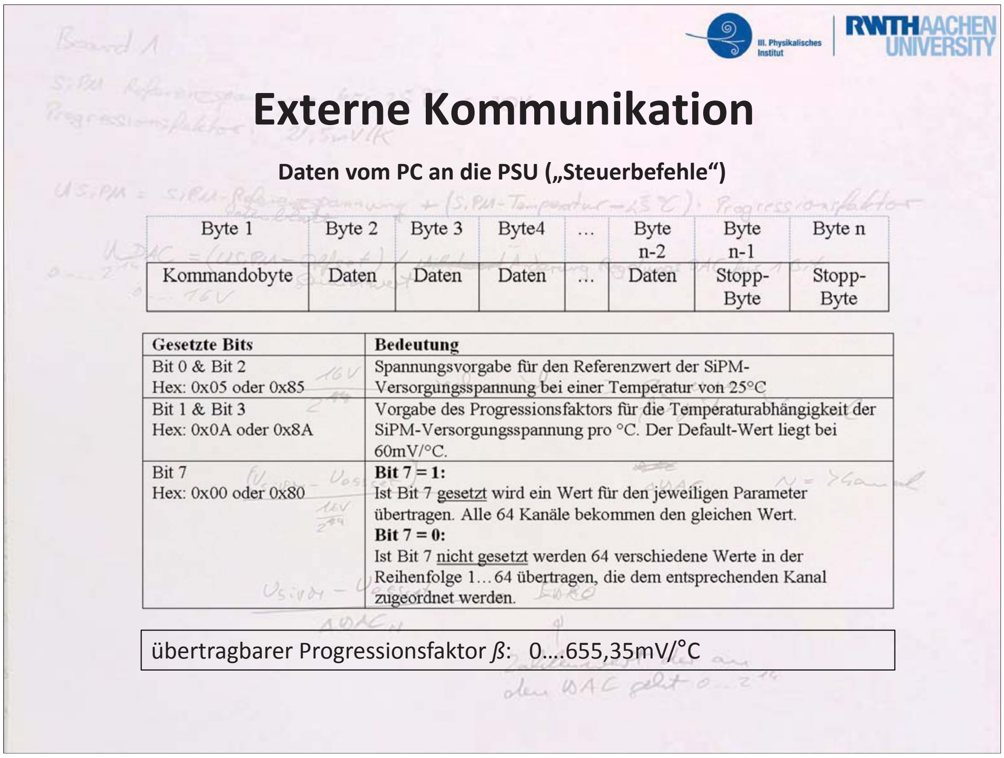
……..

Temp. SiPM64		Current SiPM64		Temp. PSU1		Temp. PSU2		Stop-Bytes	
2 Byte		2 Byte		2 Byte		2 Byte		2 Byte	
HByte	LByte	HByte	LByte	HByte	LByte	HByte	LByte	0xFF	0xFF

$$6Byte \cdot 64Kanäle + 6Byte = 390Byte$$

Folgende Parameter können an die PSU gesendet werden:

- **Progressionsfaktor der Temperaturdrift** ***ß*** ; für jeden Kanal individuell oder für alle gleich
- **SiPM-Spannung**; für jeden Kanal individuell oder für alle Kanäle gleich



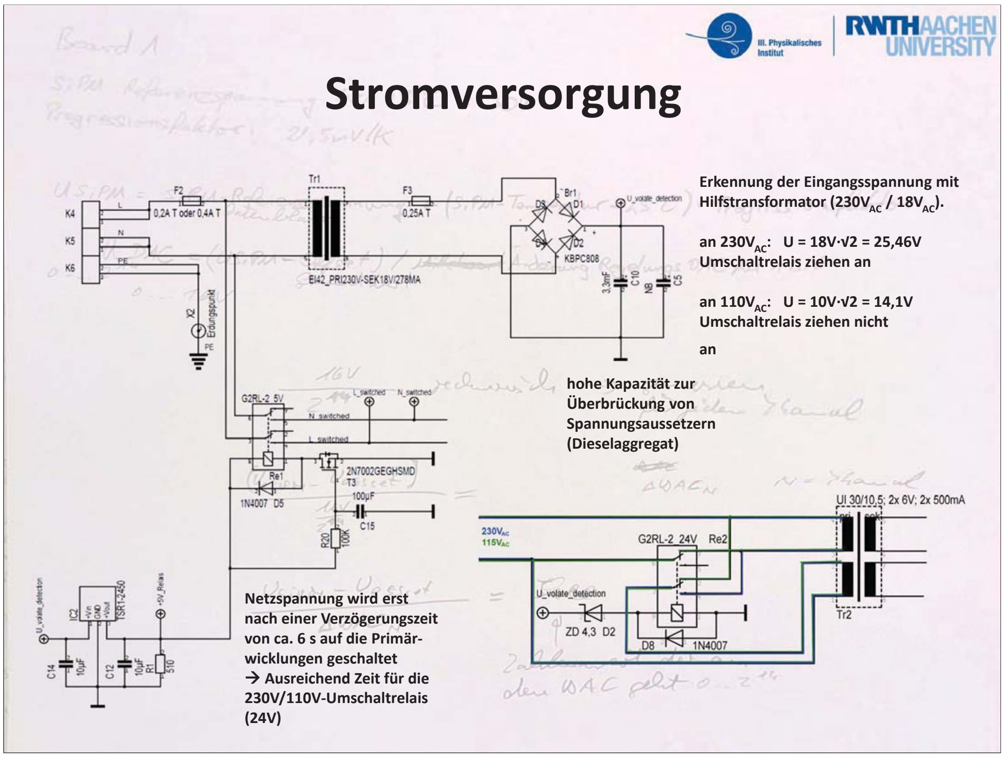
Externe Kommunikation

Daten vom PC an die PSU („Steuerbefehle“)

Byte 1	Byte 2	Byte 3	Byte4	…	Byte n-2	Byte n-1	Byte n
Kommandobyte	Daten	Daten	Daten	…	Daten	Stopp-Byte	Stopp-Byte

Gesetzte Bits	Bedeutung
Bit 0 & Bit 2 Hex: 0x05 oder 0x85	Spannungsvorgabe für den Referenzwert der SiPM-Versorgungsspannung bei einer Temperatur von 25°C
Bit 1 & Bit 3 Hex: 0x0A oder 0x8A	Vorgabe des Progressionsfaktors für die Temperaturabhängigkeit der SiPM-Versorgungsspannung pro °C. Der Default-Wert liegt bei 60mV/°C.
Bit 7 Hex: 0x00 oder 0x80	**Bit 7 = 1:** Ist Bit 7 gesetzt wird ein Wert für den jeweiligen Parameter übertragen. Alle 64 Kanäle bekommen den gleichen Wert. **Bit 7 = 0:** Ist Bit 7 nicht gesetzt werden 64 verschiedene Werte in der Reihenfolge 1…64 übertragen, die dem entsprechenden Kanal zugeordnet werden.

übertragbarer Progressionsfaktor *ß*: 0….655,35mV/°C



Stromversorgung

Erkennung der Eingangsspannung mit Hilfstransformator (230V_{AC} / 18V_{AC}).

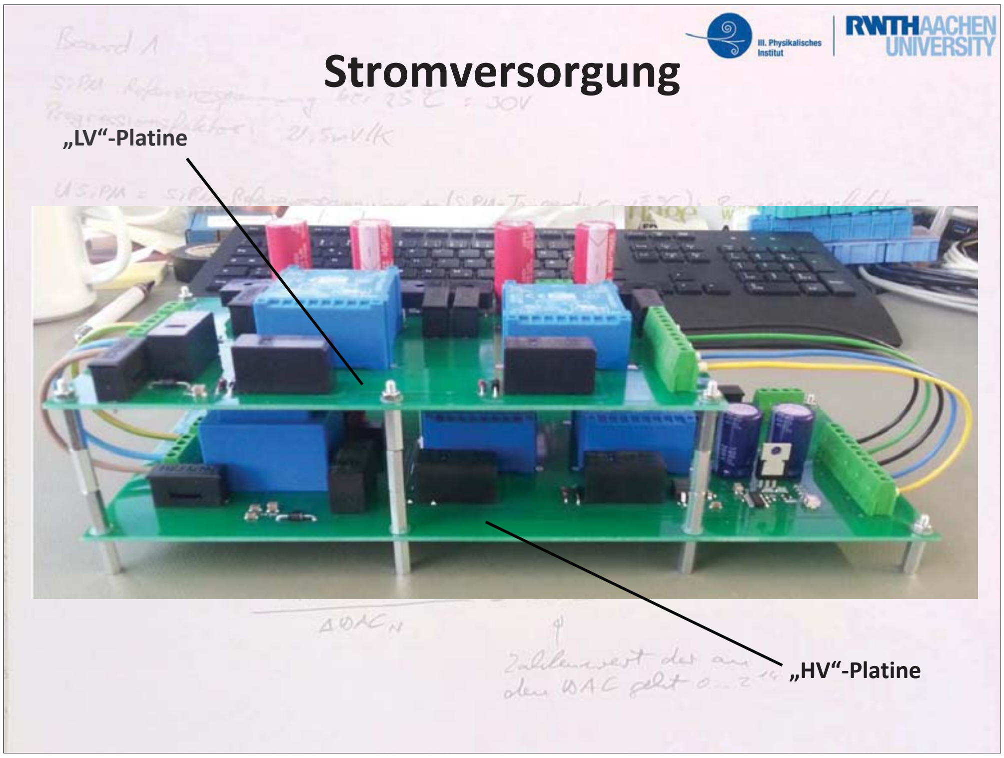
an 230V_{AC}: U = 18V·√2 = 25,46V
Umschaltrelais ziehen an

an 110V_{AC}: U = 10V·√2 = 14,1V
Umschaltrelais ziehen nicht

an

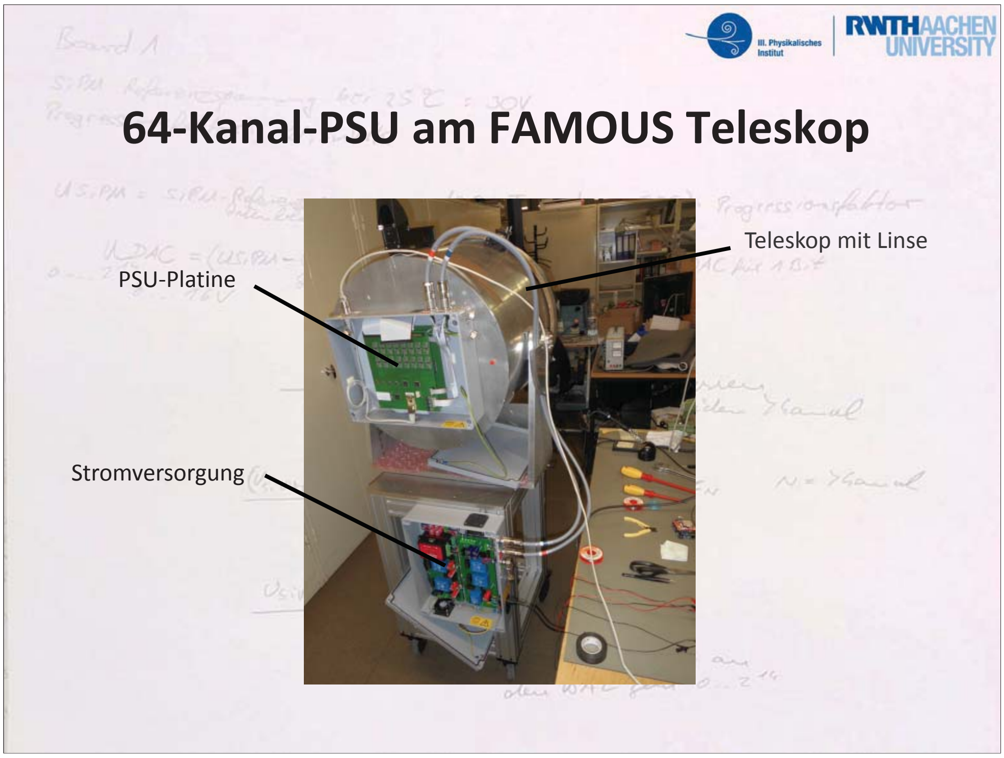
hohe Kapazität zur Überbrückung von Spannungsaussetzern (Dieselaggregat)

Netzspannung wird erst nach einer Verzögerungszeit von ca. 6 s auf die Primärwicklungen geschaltet
→ Ausreichend Zeit für die 230V/110V-Umschaltrelais (24V)



Stromversorgung

8-Kanal-PSU mit Stromversorgung eingebaut in einem Aluminiumbehälter für den Einsatz in der Antarktis

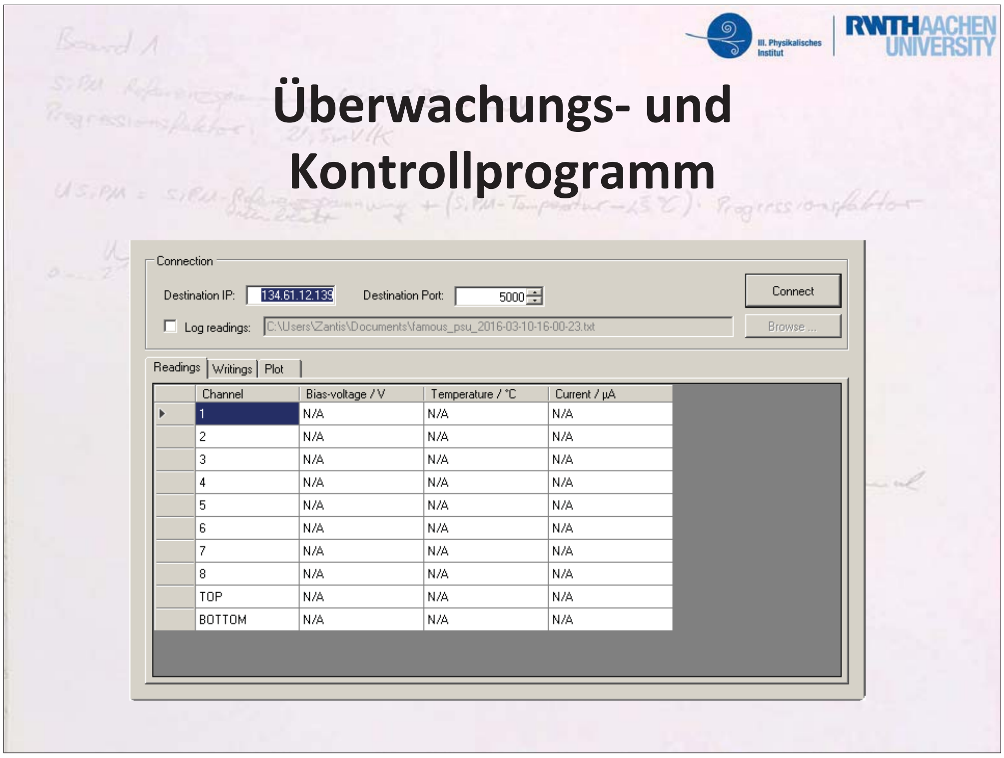


64-Kanal-PSU am FAMOUS Teleskop

PSU-Platine

Teleskop mit Linse

Stromversorgung



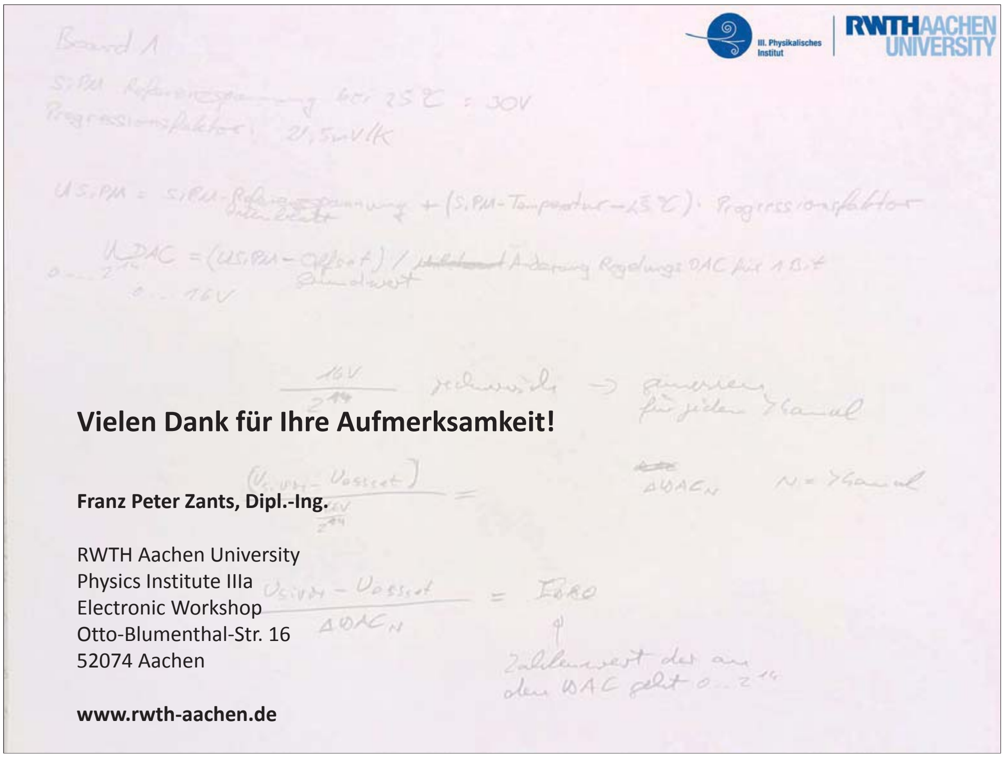
Überwachungs- und Kontrollprogramm

Connection

Destination IP: 134.61.12.139 Destination Port: 5000

☐ Log readings: C:\Users\Zantis\Documents\famous_psu_2016-03-10-16-00-23.txt

Channel	Bias-voltage / V	Temperature / °C	Current / µA
1	N/A	N/A	N/A
2	N/A	N/A	N/A
3	N/A	N/A	N/A
4	N/A	N/A	N/A
5	N/A	N/A	N/A
6	N/A	N/A	N/A
7	N/A	N/A	N/A
8	N/A	N/A	N/A
TOP	N/A	N/A	N/A
BOTTOM	N/A	N/A	N/A



Vielen Dank für Ihre Aufmerksamkeit!

Franz Peter Zants, Dipl.-Ing.

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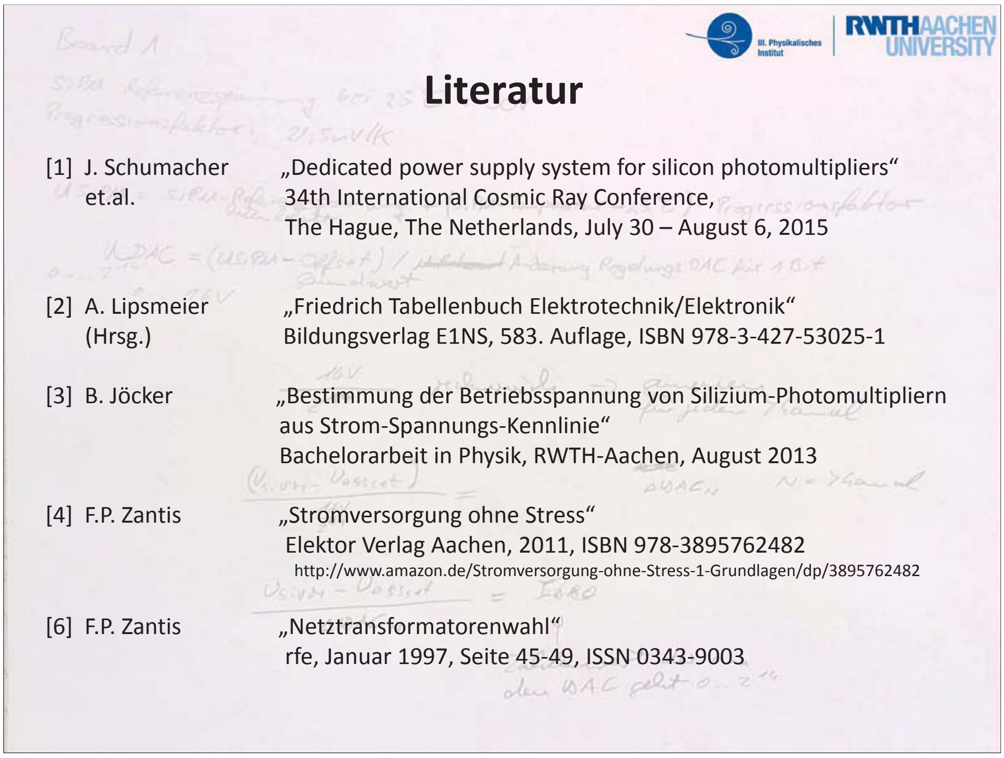

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[3] B. Jöcker „Bestimmung der Betriebsspannung von Silizium-Photomultipliern aus Strom-Spannungs-Kennlinie“ Bachelorarbeit in Physik, RWTH-Aachen, August 2013

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SEI-Tagung 2016

Entwicklung einer Multikanal-Auswertehardware für Delayline-Neutronendetektoren

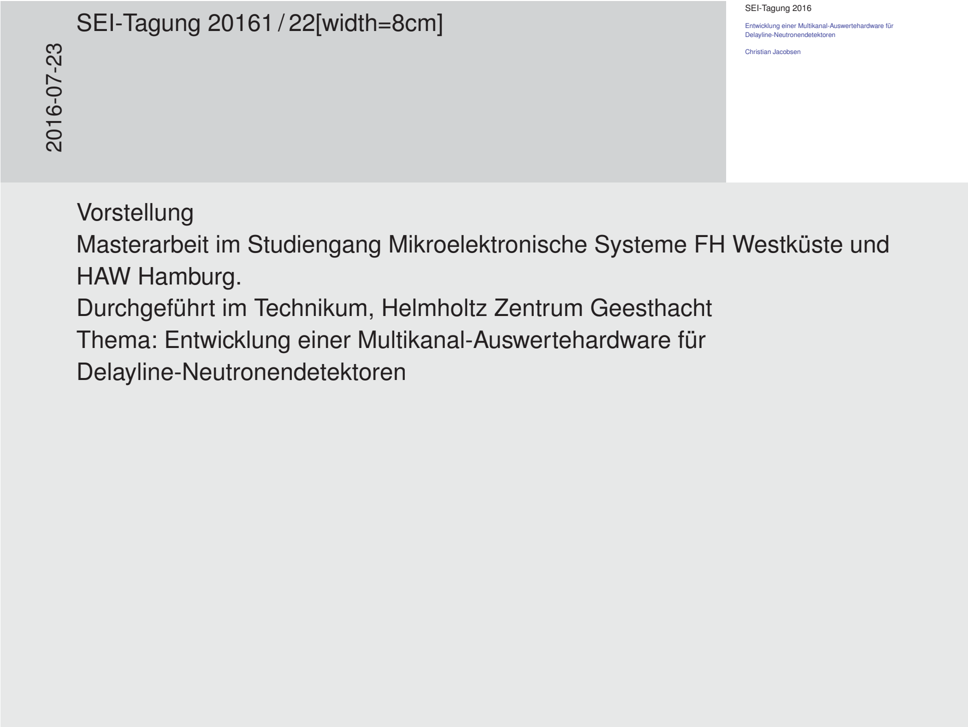
Christian Jacobsen

Darmstadt, 06. April 2016

Fachhochschule Westküste
Hochschule für Wirtschaft & Technik

Hochschule für Angewandte Wissenschaften Hamburg
Hamburg University of Applied Sciences

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung



SEI-Tagung 20161 / 22[width=8cm]

2016-07-23

SEI-Tagung 2016
Entwicklung einer Multikanal-Auswertehardware für Delayline-Neutronendetektoren
Christian Jacobsen

Vorstellung
Masterarbeit im Studiengang Mikroelektronische Systeme FH Westküste und HAW Hamburg.
Durchgeführt im Technikum, Helmholtz Zentrum Geesthacht
Thema: Entwicklung einer Multikanal-Auswertehardware für Delayline-Neutronendetektoren

Outline

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Einführung

Zeitmessung

Prozessorsystem

Ergebnisse

SEI-Tagung 20162 / 22[width=8cm]

2016-07-23

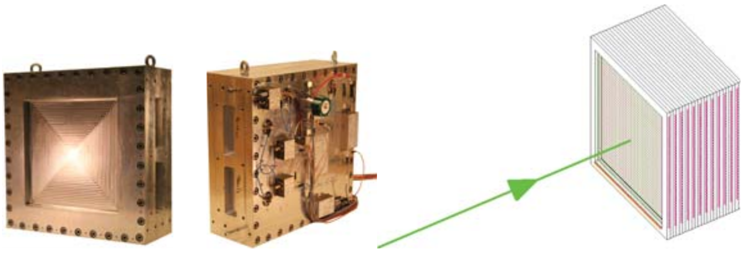
└Outline

Outline
Einführung
Zeitmessung
Prozessorsystem
Ergebnisse

Gliederung in vier Bereiche
- Darstellung eines Grundes für die Entwicklung
- Details zu der FPGA Hardware für die Zeitmessung
- Anbindung des FPGAs ein ein Prozessorsystem und Integration in Linux
- Vorstellung erster Ergebnisse

Benötigte Hardware zur Auslese

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung



Denex Testdetektor für Bor-Konverter

2016-07-23

SEI-Tagung 20163 / 22[width=8cm]
└Einführung
  └Detektoren
    └Benötigte Hardware zur Auslese

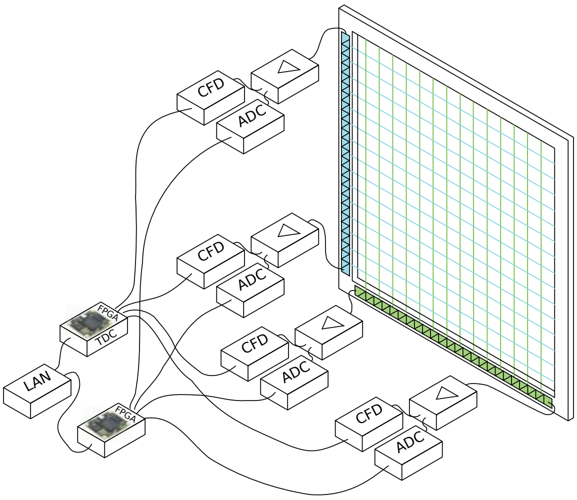
Benötigte Hardware zur Auslese

Denex Testdetektor für Bor-Konverter

Für die ESS Detektorgruppe werden werden Detektoren mit Feststoffkonverter entwickelt. Weiterhin wird ein Gas im Detektor benötigt, welches durch die Gasverstärkung ein ausreichend große Ionenwolke erzeugt. Damit bei dünnen Bor-Konverterschichten weiterhin eine vergleichbare Effizienz entsteht, müssen mehrere Konverter und Drahtebenen hintereinander verbaut werden.
- Die jeweiligen Drahtebenen werden über Delaylines zusammengefasst. Alle Ausgänge der Delaylines werden aus dem Gehäuse herausgeführt.
- Der Testdetektor ist für eine frontale und auch seitliche Bestrahlung, durch geeignete Fenster, ausgelegt.

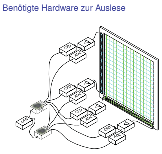
Benötigte Hardware zur Auslese

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

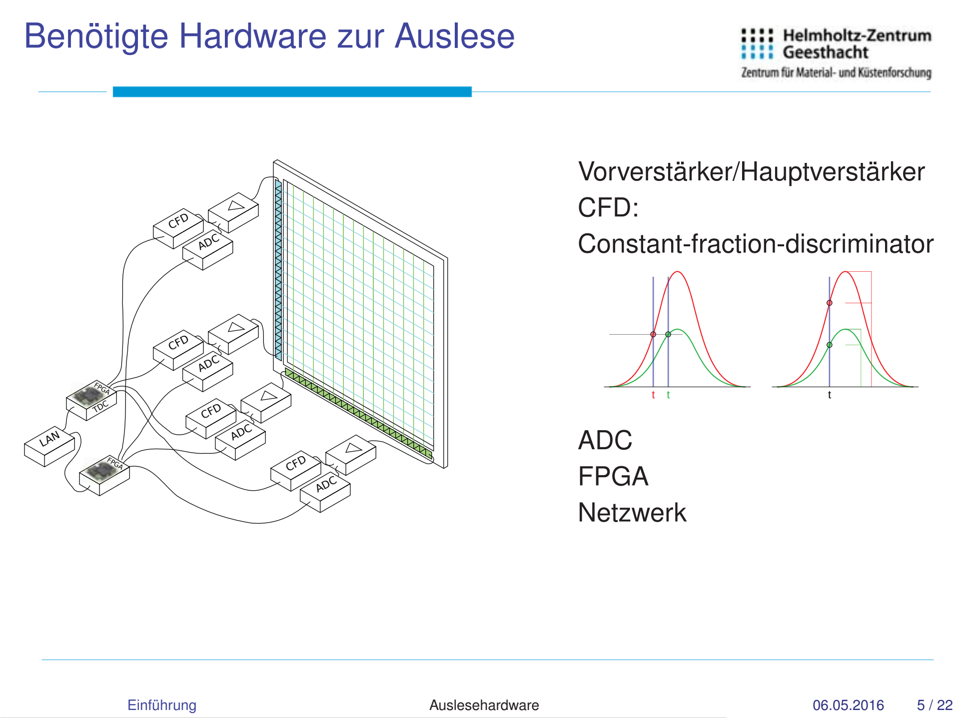


2016-07-23

SEI-Tagung 20164 / 22[width=8cm]
└─Einführung
  └─Auslesehardware
    └─Benötigte Hardware zur Auslese


Benötigte Hardware zur Auslese

- Jede Delayline liefert zwei Ausgangssignale, daher vier pro Ebene
- daher alles vierfach dargestellt
- Durch die Verwendung von Delaylines werden die Neutronenereignisse Zeitcodiert
- Alternativ wird häufig Charge-Division verwendet, bei der die Informationen über die Ereignisse in der Amplitude codiert sind.



Benötigte Hardware zur Auslese

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

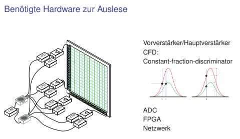
Vorverstärker/Hauptverstärker
CFD:
Constant-fraction-discriminator

ADC
FPGA
Netzwerk

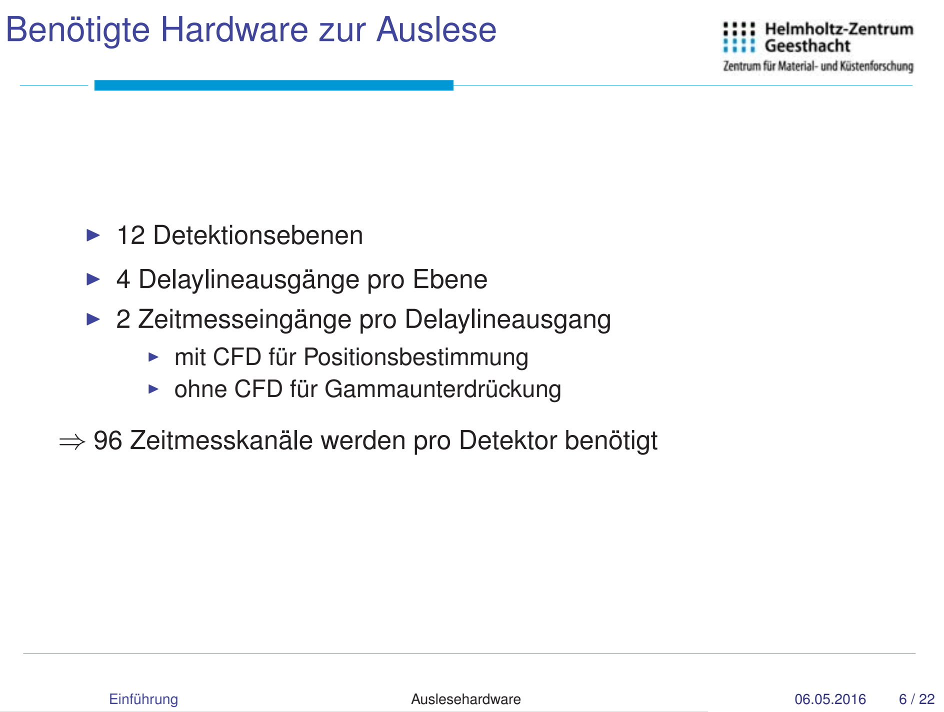
Einführung Auslesehardware 06.05.2016 5 / 22

2016-07-23

SEI-Tagung 20165 / 22[width=8cm]
└─Einführung
  └─Auslesehardware
    └─Benötigte Hardware zur Auslese



- für die Auswertung werden Vor-, Hauptverstärker benötigt
- Der CFD dient der Signalaufbereitung. Er sogt für einen Konstanten Abtastpunkt, unabhängig von der Amplitude
- Der CFD verändert aber die Signalform, die fallende Flanke wird verzögert -> zweiter Pfad ohne CFD um weiterhin Informationen über die Pulsbreite zu erhalten
- optional ist ein ADC für Monitoring vorgesehen, das geplantes ADC ist aber zu langsam für die vollständige Signalauswertung und bspw. zur Überwachung von Komparatorschwellen geeignet
- FPGA mit Zeit nach Digital Wandler für die Dekodierung der Zeitsignale
- Netzwerkinterface für Weiterverbreitung der Daten



Benötigte Hardware zur Auslese

Helmholtz-Zentrum Geesthacht
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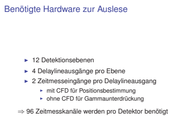
- 12 Detektionsebenen
- 4 Delaylineausgänge pro Ebene
- 2 Zeitmesseingänge pro Delaylineausgang
  - mit CFD für Positionsbestimmung
  - ohne CFD für Gammaunterdrückung

⇒ 96 Zeitmesskanäle werden pro Detektor benötigt

2016-07-23

SEI-Tagung 20166 / 22[width=8cm]
└─Einführung
  └─Auslesehardware
    └─Benötigte Hardware zur Auslese



Benötigte Hardware zur Auslese

- 12 Detektionsebenen
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- 2 Zeitmesseingänge pro Delaylineausgang
  - mit CFD für Positionsbestimmung
  - ohne CFD für Gammaunterdrückung

⇒ 96 Zeitmesskanäle werden pro Detektor benötigt

- Ein Detektor hat 12 Drahtebenen, mit jeweils X- und Y Kathode
- Jede Ebene hat vier Ausgänge
- Jeder Ausgang wird durch zwei TDC Kanäle verarbeitet, einem mit CFD und einmal ohne
- Insgesamt 96 Zeit-codierte Signale pro Detektor
- Erwartete Rate etwa 100.000 Ereignisse pro Sekunde pro Ebene

Zeitmesshardware

- Aufgrund der Zeitkodierung der Signale
  → Time-to-Digital-Converter (TDC)

Folgende Eigenschaften sollen dabei realisiert werden:

- Kontinuierliche Messung
- Eindeutige Kennzeichnung mit Kanal und Absolut-/Relativzeit
- Chronologische Sortierung der Zeitstempel
- mehrere TDC-Kanäle in einem FPGA

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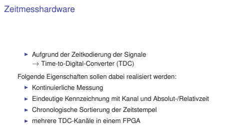
SEI-Tagung 20167 / 22[width=8cm]
└─Zeitmessung
  └─Voröberlegungen
    └─Zeitmesshardware



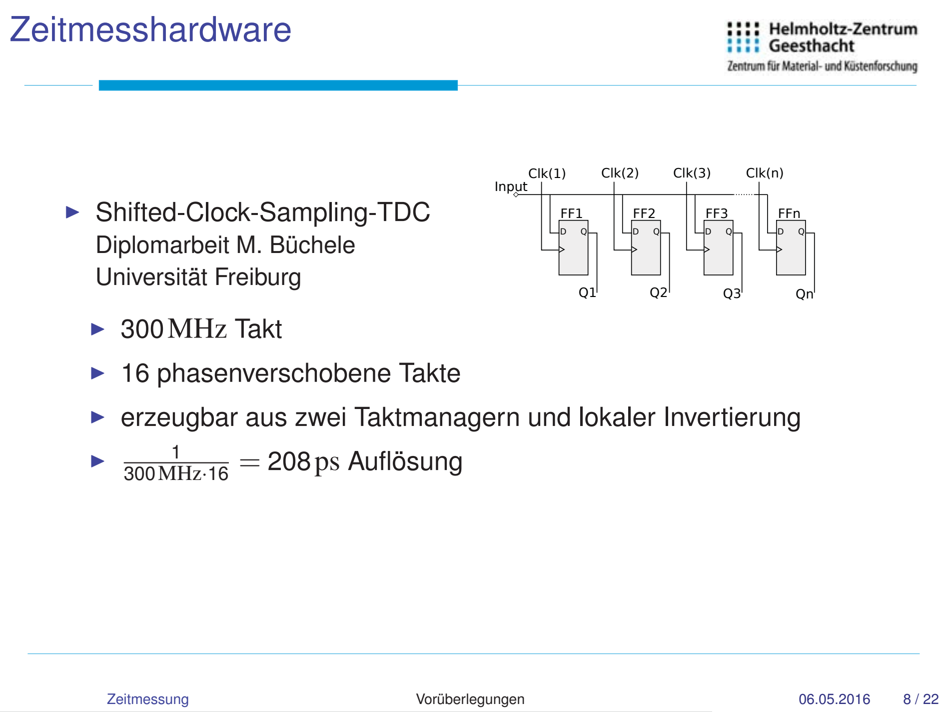
Zeitmesshardware

- Aufgrund der Zeitkodierung der Signale
  → Time-to-Digital-Converter (TDC)

Folgende Eigenschaften sollen dabei realisiert werden:

- Kontinuierliche Messung
- Eindeutige Kennzeichnung mit Kanal und Absolut-/Relativzeit
- Chronologische Sortierung der Zeitstempel
- mehrere TDC-Kanäle in einem FPGA

- Durch Delaylines ist das Signal Zeitcodiert
- Decodierung durch Time to Digital Converter auch TDC genant
- Eigenschaften die realisiert werden sollen: – eine über einen langen Zeitraum eindeutige Messung > mehrere Tage/Wochen
– alle Kanäle eines Detektors sollen eindeutig gekennzeichnet sein
– zeitlich chronologische Sortierung für eine einfache Weiterverarbeitung
– möglichst viele TDC Kanäle in einem FPGA
* Dies sind Voröberlegungen, nun folgt die konkrete Umsetzung



Zeitmesshardware

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- Shifted-Clock-Sampling-TDC
  Diplomarbeit M. Büchele
  Universität Freiburg
  - 300 MHz Takt
  - 16 phasenverschobene Takte
  - erzeugbar aus zwei Taktmanagern und lokaler Invertierung
  - $\frac{1}{300\,\mathrm{MHz}\cdot 16} = 208\,\mathrm{ps}$ Auflösung

Zeitmessung Voürberlegungen 06.05.2016 8 / 22

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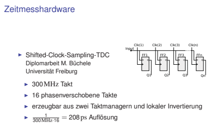
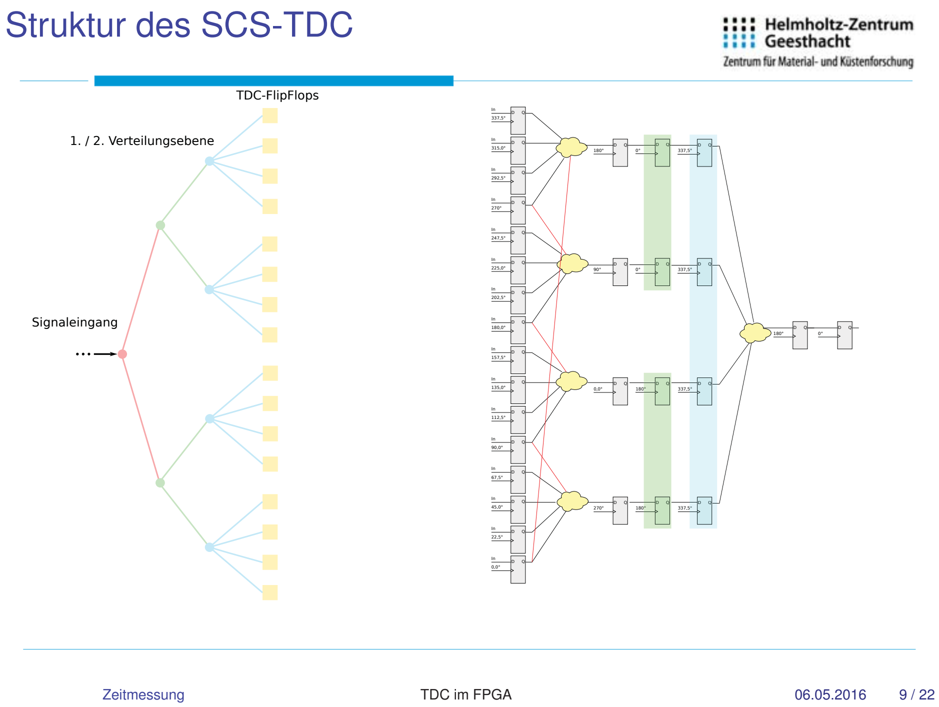
SEI-Tagung 20168 / 22[width=8cm]
└─Zeitmessung
  └─Voürberlegungen
    └─Zeitmesshardware



- Mehrere Konzepte stehen zur Auswahl für ein TDC
- Aufgrund von interessanten Eigenschaften ist die Wahl auf das Shifted Clock Sampling TDC gefallen
- Durch Phasenverschobene Takte wird ein deutlich höherer (virtuelle) Abtasttakt erzeugen
- 300*16 = 4,8GHz
- entspricht 208ps Abtastung
- Ein Taktmanager der 7er-Serie hat 6 Ausgänge, daher werde zwei Taktmanager mit jeweils vier Ausgängen verwendet, die andere Hälfte der benötigten Taktsignale wird durch lokale Invertierung erzeugt.
- Das Konzept funktioniert nur, wenn alle Flipflops das Messsignal gleichzeitig sehen

-> Routing vom FPGA Pin zum Flipflop ist entsprechend wichtig



Struktur des SCS-TDC

Zeitmessung TDC im FPGA 06.05.2016 9 / 22

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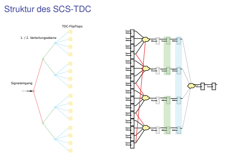
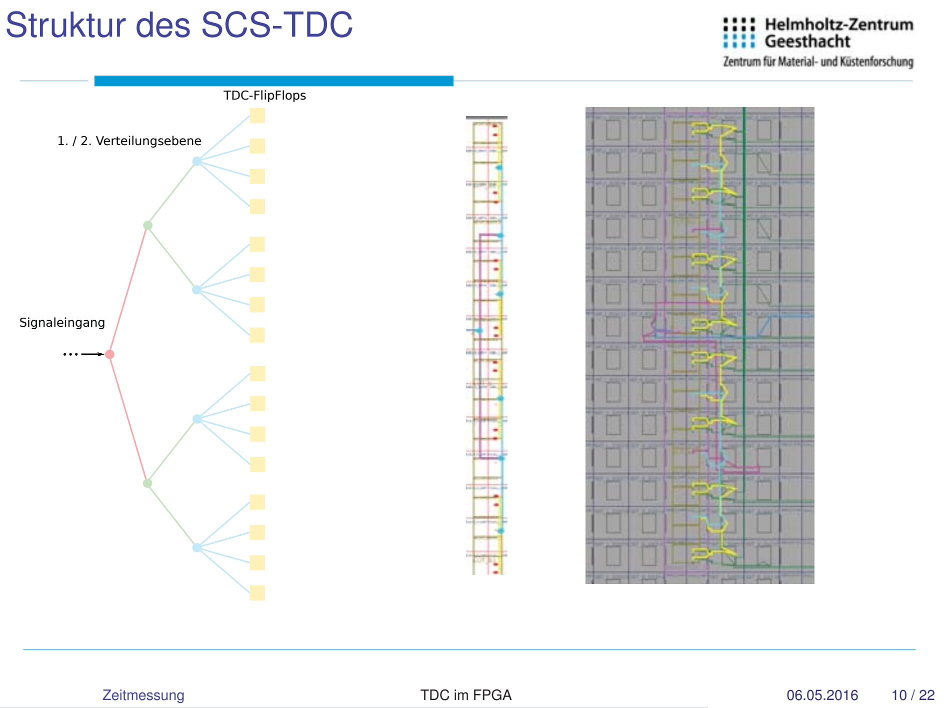
SEI-Tagung 20169 / 22[width=8cm]
└Zeitmessung
  └TDC im FPGA
    └Struktur des SCS-TDC



- Das Signal wird in Baumstruktur aufgeteilt
- Ein Baum hat vom Start zu den Enden gleich lange Wege
- Bei 16 FlipFlops werden zwei Zwischenebenen, durch LUTs als Buffer realisert, benötigt.

- Zusammenfassung der Flipflop-Signale zu einem Ausgangssignal pro Kanal
- Die ersten Wolken erkennen den Signalwechsel von low -> high
- Alle Flipflops mit einem anderen Takt, Nachbar Flipflops sind 22,5Grad verschoben
- Die vielen Taktgruppen müssen zusammengeführt werden
- Dazu Abtasten mit einem passenden Takt möglichst 180Grad phasenverschoben



Struktur des SCS-TDC

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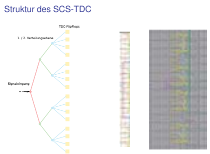
Zeitmessung TDC im FPGA 06.05.2016 10 / 22

2016-07-23

SEI-Tagung 201610 / 22[width=8cm]
└─Zeitmessung
  └─TDC im FPGA
    └─Struktur des SCS-TDC



- Links: Baumstruktur als Schema
- Mitte: Baum als Schema abgebildet auf die FPGA Struktur
– Rot Flipflops
– Bunt die einzelnen Abschnitte des Baums
– Handplatzierung aller Flipflops und LUTs durch Placement Constraint
- Rechts: Ergebnis der Implementierung

- ohne manuelles Placement ist kein sinnvolles Routing möglich

Erreichte "Gleichzeitigkeit"

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Stufe	Diff (ps)
1	10.7
2	2.0
3	2.9
Summe Diff:	15.6

Die Routingunterschiede sind wesentlich kleiner als die Auflösung von 208 ps

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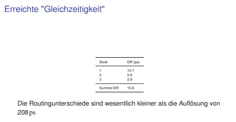
SEI-Tagung 201611 / 22[width=8cm]
└─Zeitmessung
  └─TDC im FPGA
    └─Erreichte "Gleichzeitigkeit"


Erreichte "Gleichzeitigkeit"

Die Routingunterschiede sind wesentlich kleiner als die Auflösung von 208 ps

- Auflistung der Längenunterschiede der einzelnen Wege durch den Baum
- Erste Stufe vom Eingangspin zur ersten LUT
- Zweite Stufe von Lut zu Lut
- Dritte Stufe von Lut zu Flipflop
- größter Unterschied in der ersten Stufe, auch zu sehen in der vorherigen Folie
- gesamt Unterschied in der Laufzeit deutlich kleiner als die theoretische Auflösung von 208ps, daher ist dieses Ergebnis weiterverwendet worden.
- dieser Unterschied ein Grund warum Abweichungen der Auflösung von Theorie und Praxis

Xilinx Zynq-SoC

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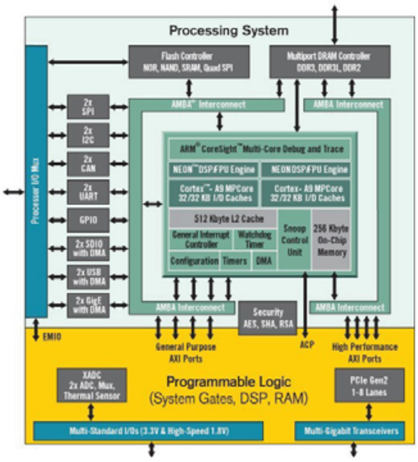
- ARM-Cortex-A9 & 7-Series Artix-FPGA als SoC
- Dualcore 700 MHz
- Neon DSP/FPU
- viele Schnittstellen verfügbar
- FPGA Logik über AMBA Interconnect direkt verbunden
- Demoboard: Zedboard



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SEI-Tagung 201612 / 22[width=8cm]
└─Prozessorsystem
  └─Zynq-FPGA
    └─Xilinx Zynq-SoC

- Für die Entwicklung wird ein Zynq FPGA verrwendet
- Zynq SoC: Artix oder Kintex FPGA und ARM Prozessor auf einem Chip
- FPGA und ARM Prozessor sind über einen gemeinsamen BUS miteinander verbunden
- Dadurch ist ein direkter Datenaustausch möglich
- Zedboard als Demoboard mit Artix FPGA

TDC als Peripherie

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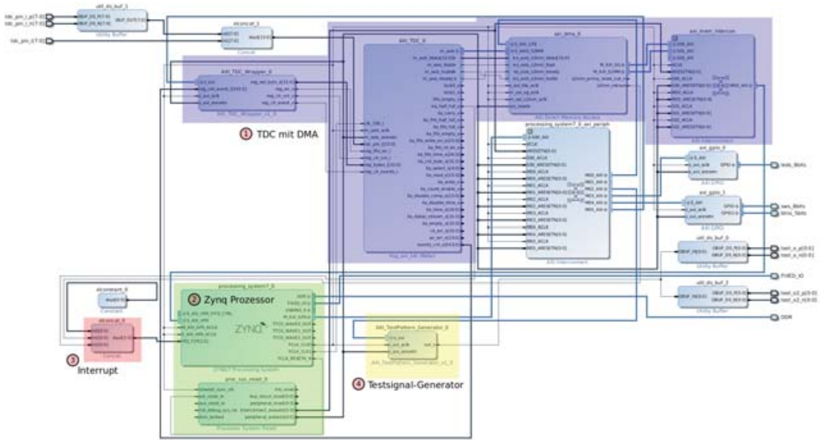
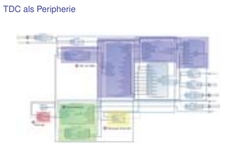
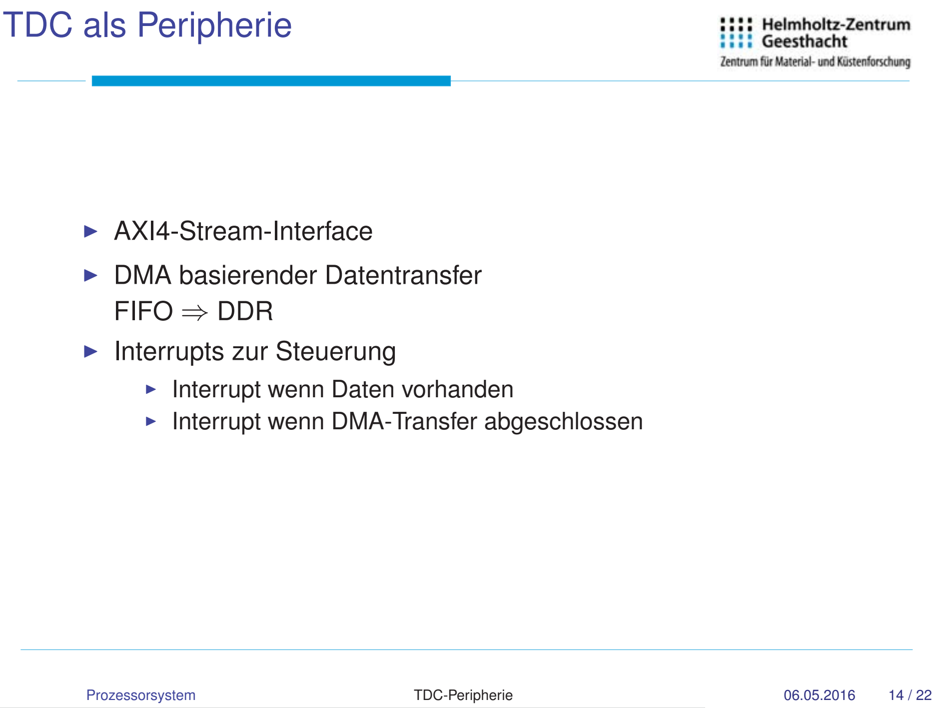


2016-07-23

SEI-Tagung 201613 / 22[width=8cm]
└─Prozessorsystem
  └─TDC-Peripherie
    └─TDC als Peripherie



- Darstellung des Vivado Projekts
– Grün: Zynq Prozessor
– Blau: TDC mit DMA-Anbindung
– Rot: Interrupts
– Geld: Testsignalgenerator
- TDC-Core kommuniziert über DMA mit dem Prozessor
- Konfiguration erfolgt über AXI-Lite Register
- Aufteilung des Cores in das reine TDC mit AXI-Stream
- und AXI-Lite Register



TDC als Peripherie

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- AXI4-Stream-Interface
- DMA basierender Datentransfer
  FIFO ⇒ DDR
- Interrupts zur Steuerung
  - Interrupt wenn Daten vorhanden
  - Interrupt wenn DMA-Transfer abgeschlossen

Prozessorsystem TDC-Peripherie 06.05.2016 14 / 22

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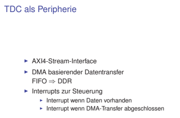
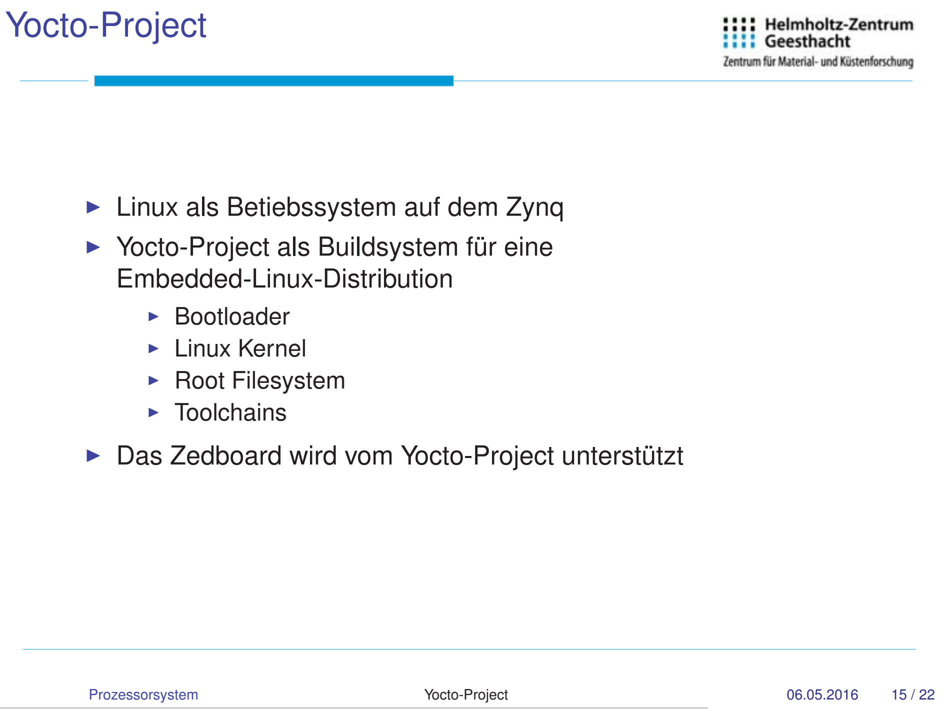
SEI-Tagung 201614 / 22[width=8cm]
└─Prozessorsystem
  └─TDC-Peripherie
    └─TDC als Peripherie


TDC als Peripherie
- AXI4-Stream-Interface
- DMA basierender Datentransfer
  FIFO ⇒ DDR
- Interrupts zur Steuerung
  - Interrupt wenn Daten vorhanden
  - Interrupt wenn DMA-Transfer abgeschlossen

- Streaming Interface für die Zeitstempel
– Streaming Daten werden per DMA zum Hauptspeicher des ARM kopiert
- Interrupts für die Flusssteuerung
– Interrupt vom TDC wird gesetzt, wenn der Ausgangsfifo halb gefüllt ist -> DMA Transfer starten
– DMA setzt Interrupt, wenn Transfer abgeschlossen ist -> Weitere Verarbeitung beginnen



Yocto-Project

- Linux als Betiebssystem auf dem Zynq
- Yocto-Project als Buildsystem für eine Embedded-Linux-Distribution
  - Bootloader
  - Linux Kernel
  - Root Filesystem
  - Toolchains
- Das Zedboard wird vom Yocto-Project unterstützt

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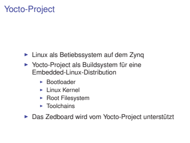
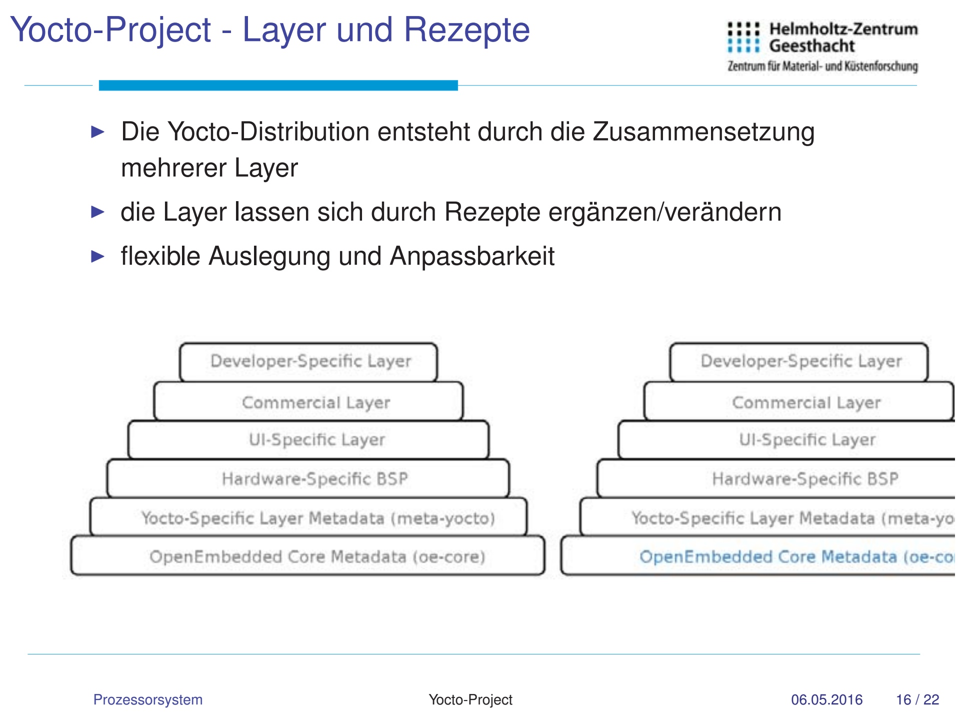
SEI-Tagung 201615 / 22[width=8cm]
└─Prozessorsystem
  └─Yocto-Project
    └─Yocto-Project



Yocto-Project

- Linux als Betiebssystem auf dem Zynq
- Yocto-Project als Buildsystem für eine Embedded-Linux-Distribution
  - Bootloader
  - Linux Kernel
  - Root Filesystem
  - Toolchains
- Das Zedboard wird vom Yocto-Project unterstützt

- Auf dem Dualcore ARM lässt sich Linux ausführen
- Wahl ist auf Yocto gefallen -> hohe Flexibilität
- Yocto-Project ist eine Umgebung zum erstellen einer eigenen Linux-Distribution
- Xilinx supportet das Zedboard für Yocto



Yocto-Project - Layer und Rezepte

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- Die Yocto-Distribution entsteht durch die Zusammensetzung mehrerer Layer
- die Layer lassen sich durch Rezepte ergänzen/verändern
- flexible Auslegung und Anpassbarkeit

Prozessorsystem Yocto-Project 06.05.2016 16 / 22

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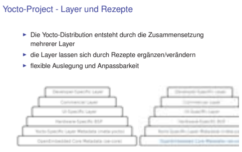
SEI-Tagung 201616 / 22[width=8cm]
└─Prozessorsystem
  └─Yocto-Project
    └─Yocto-Project - Layer und Rezepte

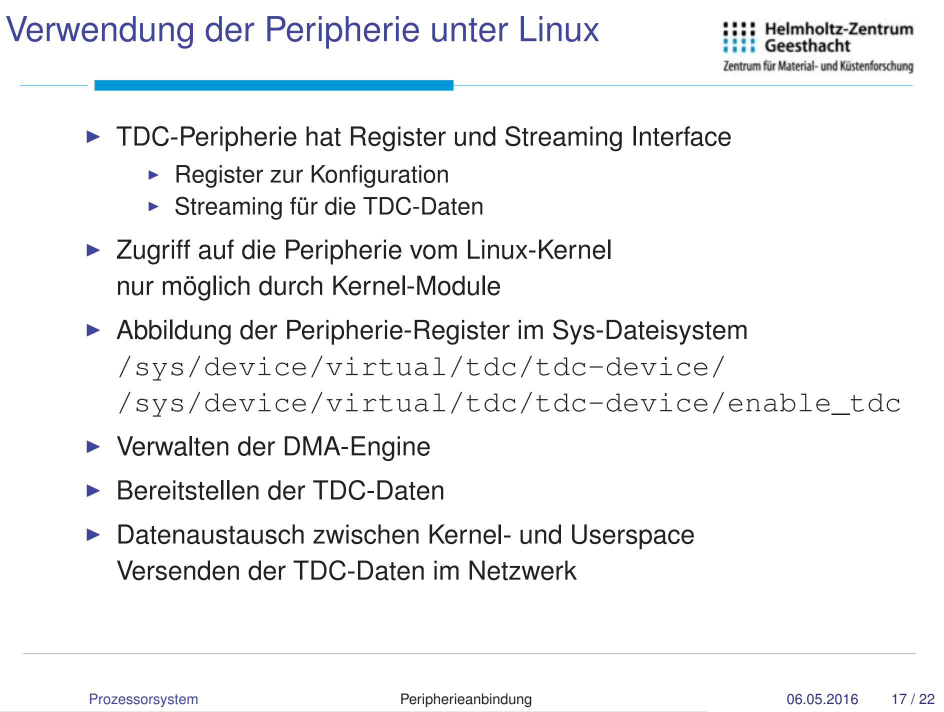


- Zum Bauen einer Distribution werden mehrere Layer und Rezepte benötigt
- Layer enthalten eine Sammlung von Rezepten
- Bestehende Layer lassen sich verwenden und durch eigene Rezepte anpassen
- dadurch sehr flexibel

* OpenEmbedded Layer: Grundlayer, welcher die Buildtools enthält
* Yocto Layer: Grundlayer
* Hardware Layer: Board Support Package, enthält alle hardwareabhängigen Einstellungen
* Software Layer: definieren die Programme, Kernel, RootFS, usw.

\+ Durch Austausch des Hardware Layer lässt sich das angepasste Linux auf anderen Plattformen ausführen

\+ Durch Anpassen des Software Layers lassen sich verschiedene Programme hinzufügen



Verwendung der Peripherie unter Linux

- TDC-Peripherie hat Register und Streaming Interface
  - Register zur Konfiguration
  - Streaming für die TDC-Daten
- Zugriff auf die Peripherie vom Linux-Kernel nur möglich durch Kernel-Module
- Abbildung der Peripherie-Register im Sys-Dateisystem
  `/sys/device/virtual/tdc/tdc-device/`
  `/sys/device/virtual/tdc/tdc-device/enable_tdc`
- Verwalten der DMA-Engine
- Bereitstellen der TDC-Daten
- Datenaustausch zwischen Kernel- und Userspace
  Versenden der TDC-Daten im Netzwerk

Prozessorsystem | Peripherieanbindung | 06.05.2016 | 17 / 22

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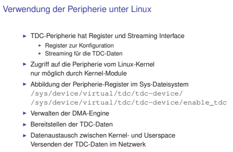
SEI-Tagung 201617 / 22[width=8cm]
└─Prozessorsystem
  └─Peripherieanbindung
    └─Verwendung der Peripherie unter Linux



- Zwei Möglichkeiten zur Kommunikation mit dem TDC-Core
– Register
– Streaming - DMA
- Unterscheidung Userspace und Kernelspace, Benutzerprogramme im Userspace, Hardwaretreiber und Systemkomponenten im Kernelspace
– Kein direkter Zugriff vom Userspace in den Kernelspace
- Zugriff auf den AXI-Bus nur vom Kernel aus möglich (außer Userspace IO (UIO) oder /dev/mem)
- Bereitstellen der Register für den Userspace über SysFS Einträge
- SysFS ist ein virtuelles Dateisystem für den Kernel, kann vom Userspace beschrieben und gelesen werden
- Weitere Aufgaben des Kernelmoduls: DMA-Engine Verwalten, eine Schnittstelle anbieten für den Transport vom Kernel zum User

Darstellung einer Webseite

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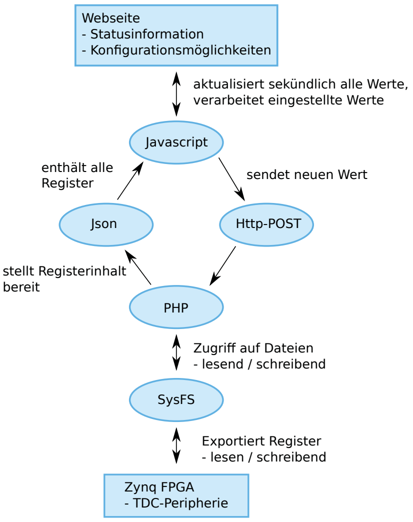
HZG - TKE
TDC -Detektorauslese
TDC
Testsignal Generator
Counter stats
Counter stats
Device stats



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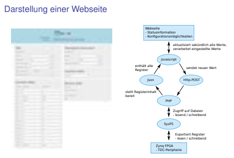
SEI-Tagung 201618 / 22[width=8cm]
└─Prozessorsystem
  └─Peripherieanbindung
    └─Darstellung einer Webseite



- Webserver mit PHP für Webseite
- Darstellung der Register aus dem SysFS durch PHP
- Livedarstellung aktueller Werte durch Javascript
- Bereitstellen der Daten durch PHP im JSON Format

Verteilung der BINs

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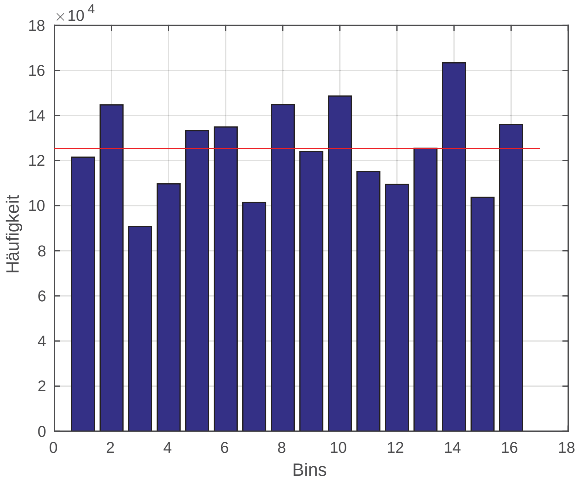
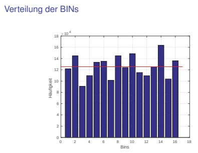


2016-07-23

SEI-Tagung 201619 / 22[width=8cm]
└─Ergebnisse
  └─Abweichungen
    └─Verteilung der BINs



- Anregung durch Funktionsgenerator
- Dargestellt ist ein TDC-Kanal
- x-Achse: jede Säule ein Flipflop
- y-Achse: Anzahl der Ereignisse pro Flipflop
- Erwartung: identische Anzahl von Ereignissen bei allen Flipflops
- Abweichung bspw. durch verschiedene Laufzeiten im Baum
- Abweichungen durch verschiedene Laufzeiten der Taktsignale
- Abweichung durch den lokalen Inverter

DNL

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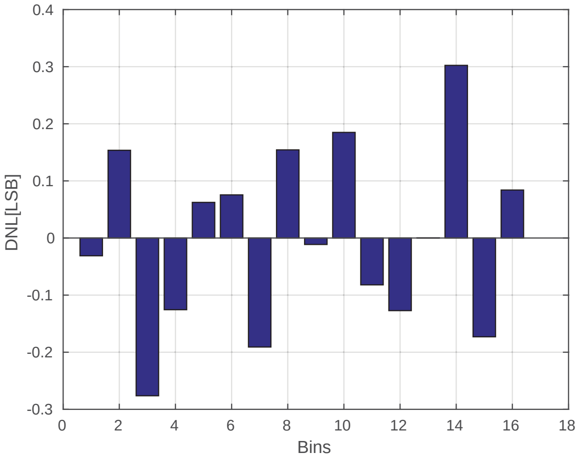
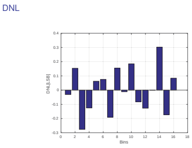


2016-07-23

SEI-Tagung 201620 / 22[width=8cm]
└Ergebnisse
  └Abweichungen
    └DNL



- Berechnung der Abweichung vom theoretischen Wert
- Kanal 14 etwa 30% zu viele Ereignisse
- Bedeutung: die Kennlinie entspricht nicht einer Treppe mit identischen Stufen, manche sind breiter andere schmaler
- Kanal 14 ist zu breit +62ps

* Auflösung daher $208\,\mathrm{ps} \pm 30\%$
* Geforderte Auflösung für Drahtdekodierung Delayline: $1\,\mathrm{ns} - 1.8\,\mathrm{ns}$ -> deutlich besser

Delayline X2-X1

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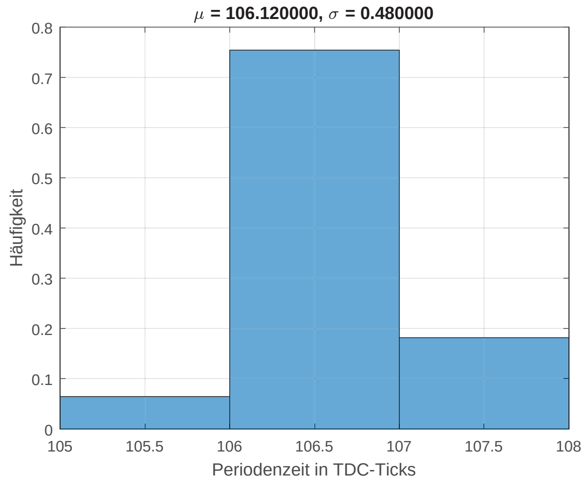
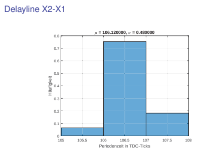
Zentrum für Material- und Küstenforschung



2016-07-23

SEI-Tagung 201621 / 22[width=8cm]
└─Ergebnisse
  └─Delayline
    └─Delayline X2-X1



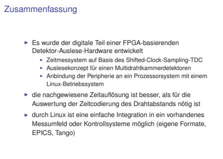
- Messung an einer echten Delayline.
- Einspeisung des Generatorsignals an beliebiger stelle in die Delayline
- Zwei TDC-Kanäle werden für die Auswertung verwendet
- Dargestellt ist die Differenz der Zweitstempel von beiden Kanälen
- 75% der registrierten Ereignisse entfallen auf einen TDC-Wert. Die restlichen Ereignisse verteilen sich auf die direkten Nachbarsignale.

Zusammenfassung

- Es wurde der digitale Teil einer FPGA-basierenden Detektor-Auslese-Hardware entwickelt
    - Zeitmessystem auf Basis des Shifted-Clock-Sampling-TDC
    - Auslesekonzept für einen Multidrahtkammerdetektoren
    - Anbindung der Peripherie an ein Prozessorsystem mit einem Linux-Betriebssystem
- die nachgewiesene Zeitauflösung ist besser, als für die Auswertung der Zeitcodierung des Drahtabstands nötig ist
- durch Linux ist eine einfache Integration in ein vorhandenes Messumfeld oder Kontrollsysteme möglich (eigene Formate, EPICS, Tango)

2016-07-23

SEI-Tagung 201622 / 22[width=8cm]
└─Ergebnisse
  └─Zusammenfassung
    └─Zusammenfassung



Zusammenfassung

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Backup

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Backup

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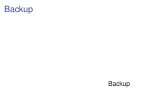
SEI-Tagung 20161 / 7[width=8cm]

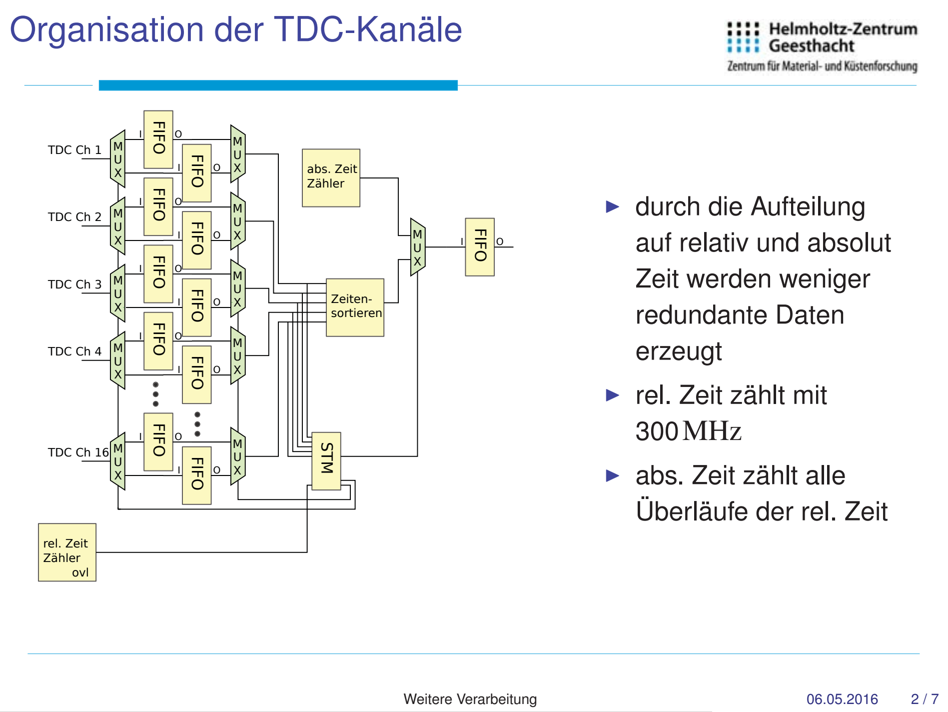
└─Weitere Verarbeitung
  └─Backup



Backup

Backup

- Zusatzfolien



Organisation der TDC-Kanäle

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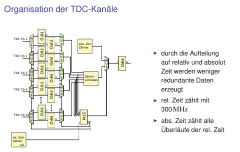
- durch die Aufteilung auf relativ und absolut Zeit werden weniger redundante Daten erzeugt
- rel. Zeit zählt mit 300 MHz
- abs. Zeit zählt alle Überläufe der rel. Zeit

Weitere Verarbeitung 06.05.2016 2 / 7

SEI-Tagung 20162 / 7[width=8cm]

2016-07-23

Weitere Verarbeitung
  Organisation der TDC-Kanäle



- Abbildung mehrerer TDC-Kanäle in einem FPGA, hier 16
- Besonderheit: Aufteilung in absolut- und relativ-Zeit
- dadurch Reduzierung der redundanten Informationen
- durch diese Aufteilung sind sehr große Zeitstempel möglich -> > 20 Tage
- Absolutzeit zählt die Überläufe des Relativzeitzählers
- Relativzeit zählt mit 300MHz der Abtastfrequenz jedes einzelnen Flipflop
- doppelte Anzahl von FIFOs für die Intervallumschaltung
- Zeitstempel werden sortiert weitergegeben

Zeitstempel

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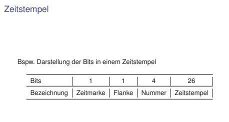
Bspw. Darstellung der Bits in einem Zeitstempel

Bits	1	1	4	26
Bezeichnung	Zeitmarke	Flanke	Nummer	Zeitstempel

2016-07-23

SEI-Tagung 20163 / 7[width=8cm]

└Weitere Verarbeitung
  └Zeitstempel



Zeitstempel

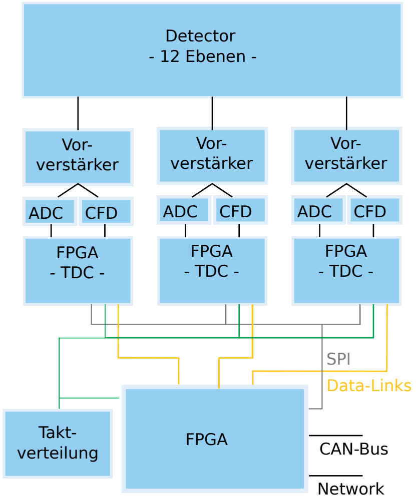
Bspw. Darstellung der Bits in einem Zeitstempel

Bits	1	1	4	26
Bezeichnung	Zeitmarke	Flanke	Nummer	Zeitstempel

- Darstellung eines möglichen Zeitstempelformates
- Zeitmarke: relativ oder Absolutzeit
- Flanke: ob fallende oder steigende Flanke
- Nummer: Identifizierung des jeweiligen FlipFlop
- Zeitstempel

Konzept

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung



Detector
- 12 Ebenen -

Vor-
verstärker

ADC
CFD

FPGA
- TDC -

SPI
Data-Links

Takt-
verteilung

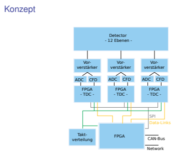
FPGA

CAN-Bus
Network

SEI-Tagung 20164 / 7[width=8cm]

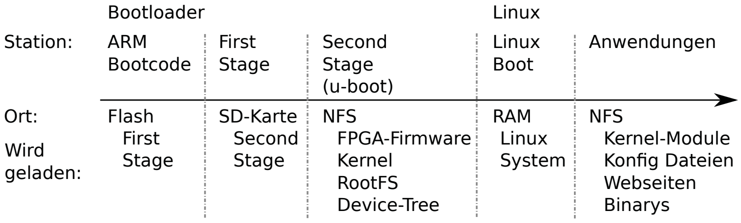
2016-07-23

└Weitere Verarbeitung
  └Konzept

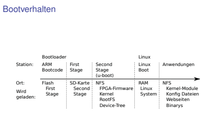


- Möglicher Realisierungsweg zur Auswertung des vollständigen Detektors
- Aufteilung des Detektors in mehrere Gruppen, die von jeweils einem FPGA verarbeitet werden
- Ein Haupt-FPGA sammelt die Ereignisse von den anderen FPGAs ein und berechnet weitere Zwischenergebnisse
- Eine gemeinsame Taktverteilung sorgt für synchrone TDCs

Bootverhalten



	Bootloader			Linux	
Station:	ARM Bootcode	First Stage	Second Stage (u-boot)	Linux Boot	Anwendungen
Ort:	Flash	SD-Karte	NFS	RAM	NFS
Wird geladen:	First Stage	Second Stage	FPGA-Firmware Kernel RootFS Device-Tree	Linux System	Kernel-Module Konfig Dateien Webseiten Binarys



- Darstellung der einzelnen Stufen, die beim starten des Linux Systems auf dem Zynq durchlaufen werden.

Koordinatnberechnung

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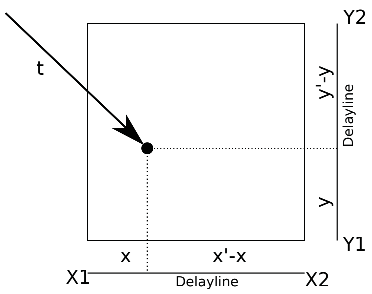
Zentrum für Material- und Küstenforschung

x', y': Delayline länge
t: Time of Flight (ToF)



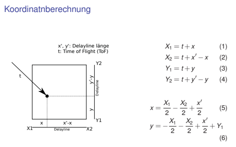
$$X_1 = t + x \qquad (1)$$
$$X_2 = t + x' - x \qquad (2)$$
$$Y_1 = t + y \qquad (3)$$
$$Y_2 = t + y' - y \qquad (4)$$

$$x = \frac{X_1}{2} - \frac{X_2}{2} + \frac{x'}{2} \qquad (5)$$
$$y = -\frac{X_1}{2} - \frac{X_2}{2} + \frac{x'}{2} + Y_1 \qquad (6)$$

2016-07-23

SEI-Tagung 20166 / 7[width=8cm]

└Weitere Verarbeitung
  └Koordinatnberechnung



Koordinatnberechnung

- Berechnungsschritte um von den Einzelsignalen der Delaylines auf die Position des Neutrons schließend zu können.
- Für die Berechnung werden durch die Grundrechenarten benötigt, dadurch lassen sich die Berechnungsvorschriften in Hardware implementieren.

Kerner- und Userspace

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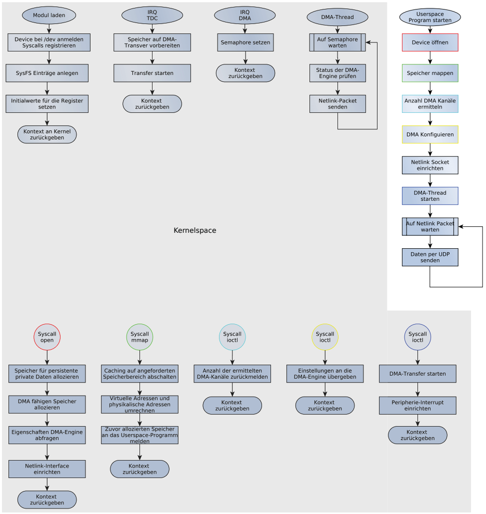
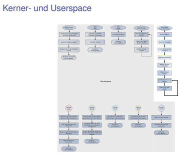
Zentrum für Material- und Küstenforschung



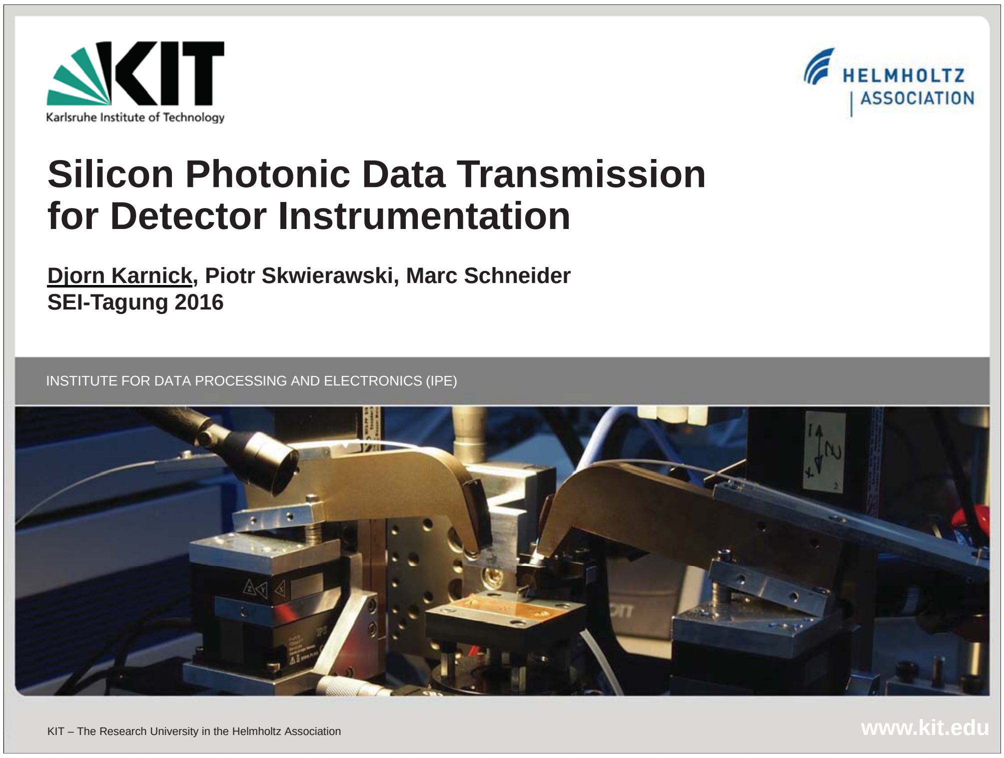
2016-07-23

SEI-Tagung 20167 / 7[width=8cm]

└Weitere Verarbeitung
  └Kerner- und Userspace



- Das Programm auf dem Zynq besteht aus mehreren Komponenten
- Teile laufen im Kernelspace oder im Userspace des Linuxsystems
- Dargestellt sind die Funktionen zum Initialisieren, aber auch die Interrupts und System Calls.



Karlsruhe Institute of Technology

HELMHOLTZ ASSOCIATION

Silicon Photonic Data Transmission for Detector Instrumentation

Djorn Karnick, Piotr Skwierawski, Marc Schneider
SEI-Tagung 2016

INSTITUTE FOR DATA PROCESSING AND ELECTRONICS (IPE)

KIT – The Research University in the Helmholtz Association

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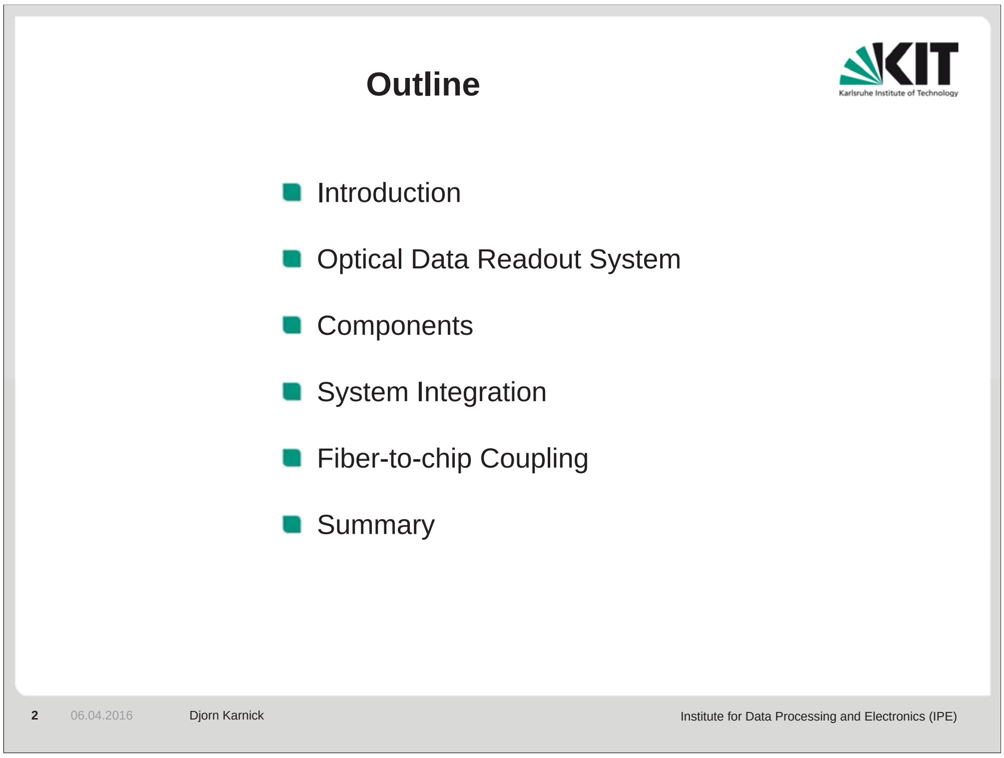

Karlsruhe Institute of Technology

Outline

- Introduction
- Optical Data Readout System
- Components
- System Integration
- Fiber-to-chip Coupling
- Summary

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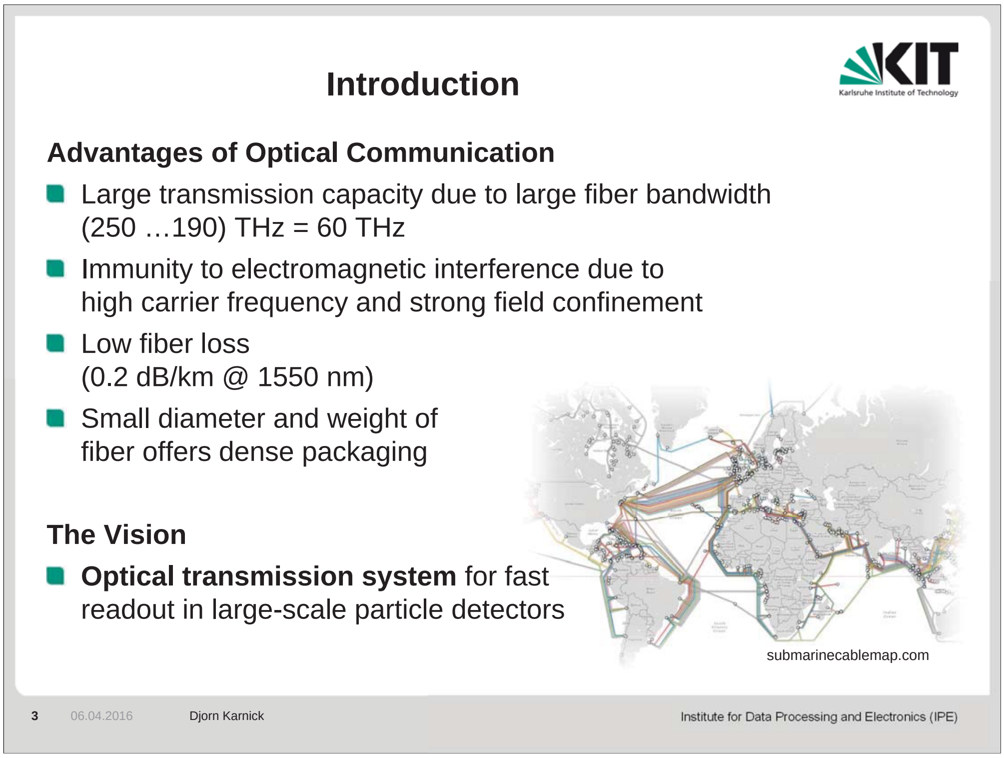


Introduction

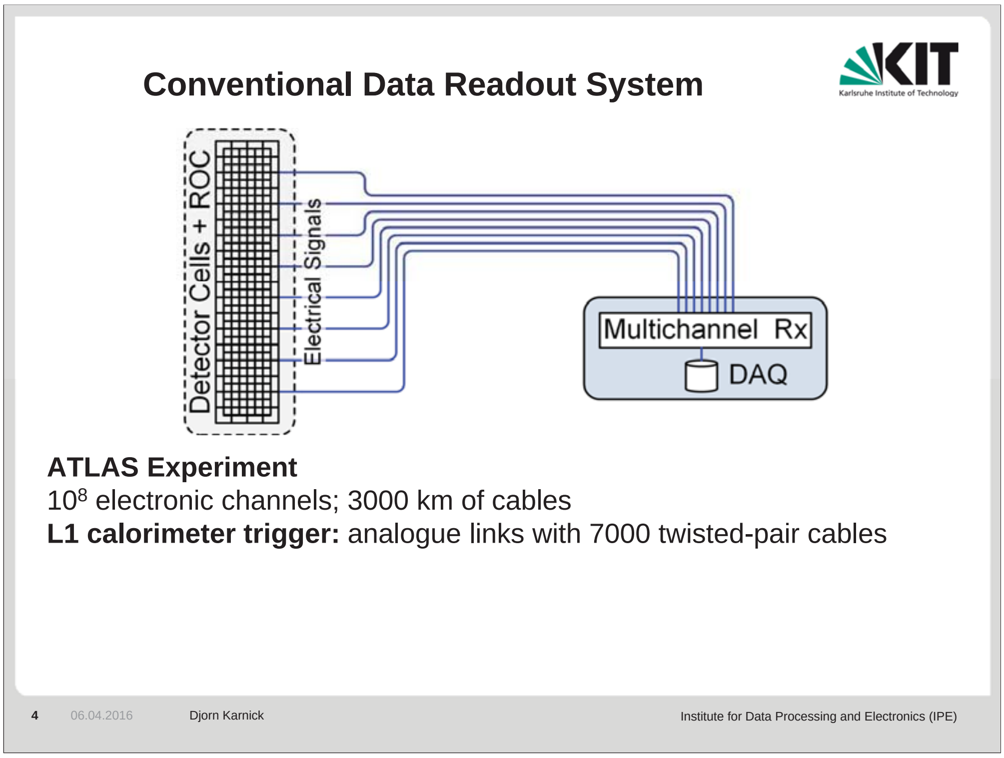
Advantages of Optical Communication

- Large transmission capacity due to large fiber bandwidth (250 …190) THz = 60 THz
- Immunity to electromagnetic interference due to high carrier frequency and strong field confinement
- Low fiber loss (0.2 dB/km @ 1550 nm)
- Small diameter and weight of fiber offers dense packaging

The Vision

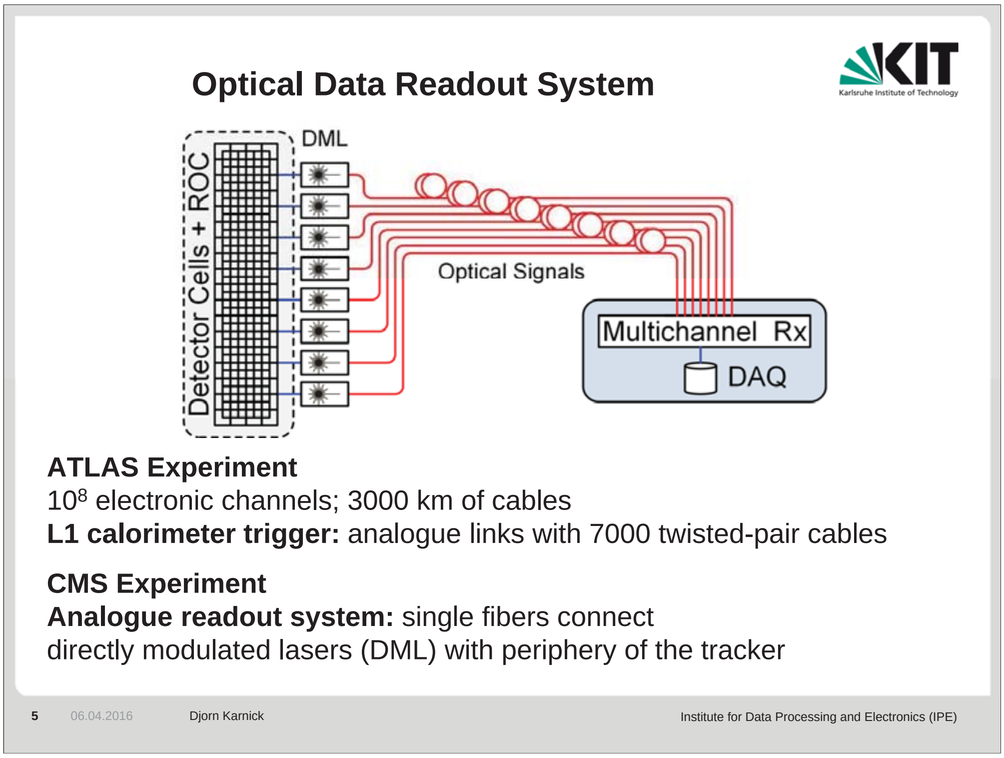
- **Optical transmission system** for fast readout in large-scale particle detectors

submarinecablemap.com



Conventional Data Readout System

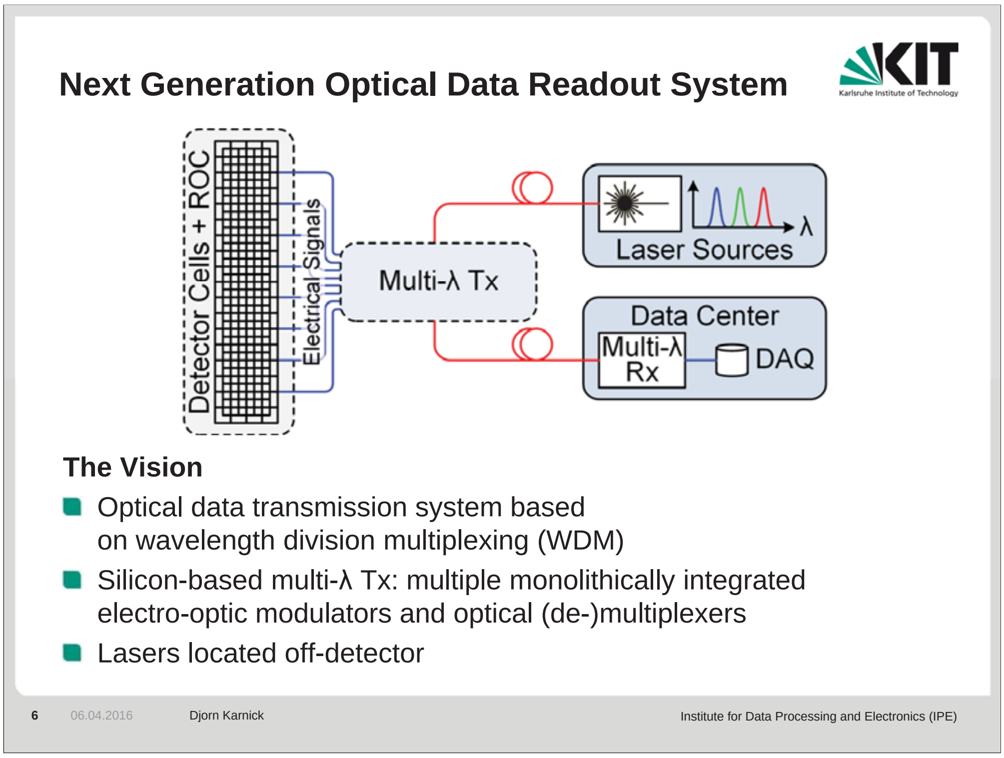
ATLAS Experiment
10^8 electronic channels; 3000 km of cables
L1 calorimeter trigger: analogue links with 7000 twisted-pair cables



Optical Data Readout System

ATLAS Experiment
10^8 electronic channels; 3000 km of cables
L1 calorimeter trigger: analogue links with 7000 twisted-pair cables

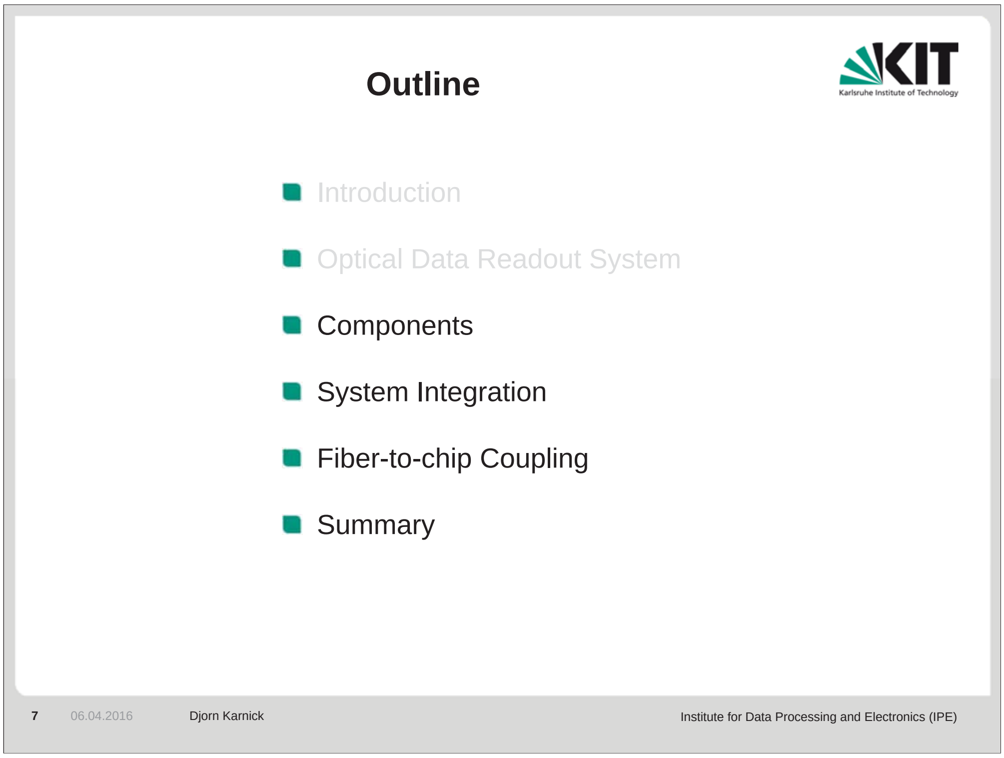
CMS Experiment
Analogue readout system: single fibers connect directly modulated lasers (DML) with periphery of the tracker



Next Generation Optical Data Readout System

The Vision

- Optical data transmission system based on wavelength division multiplexing (WDM)
- Silicon-based multi-λ Tx: multiple monolithically integrated electro-optic modulators and optical (de-)multiplexers
- Lasers located off-detector



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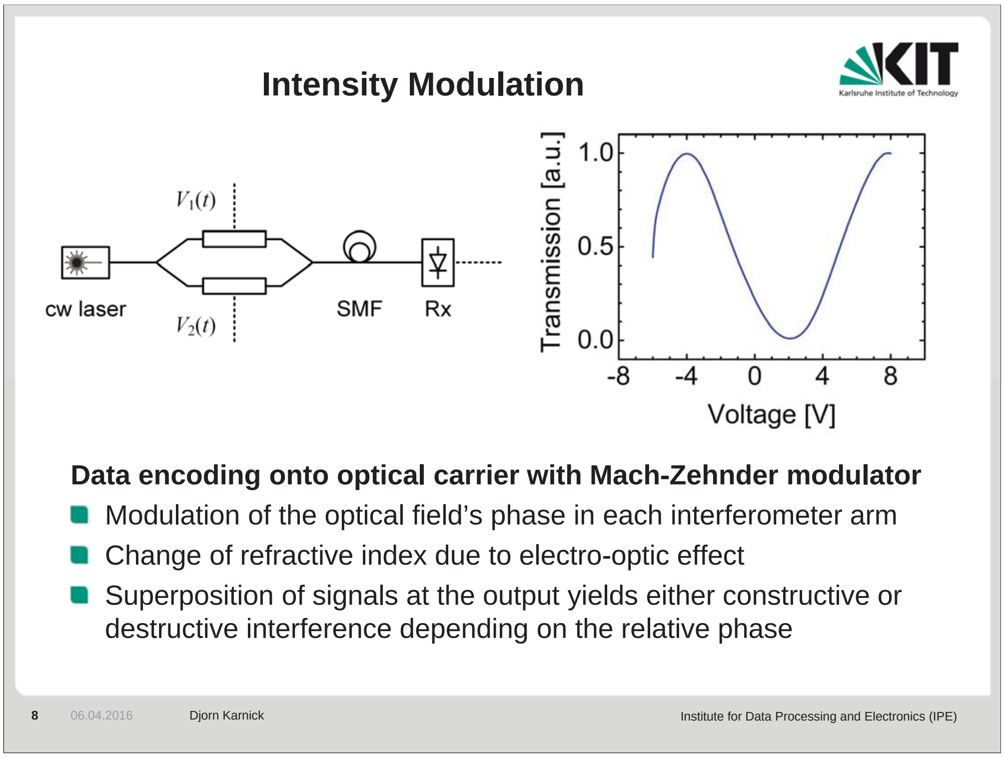
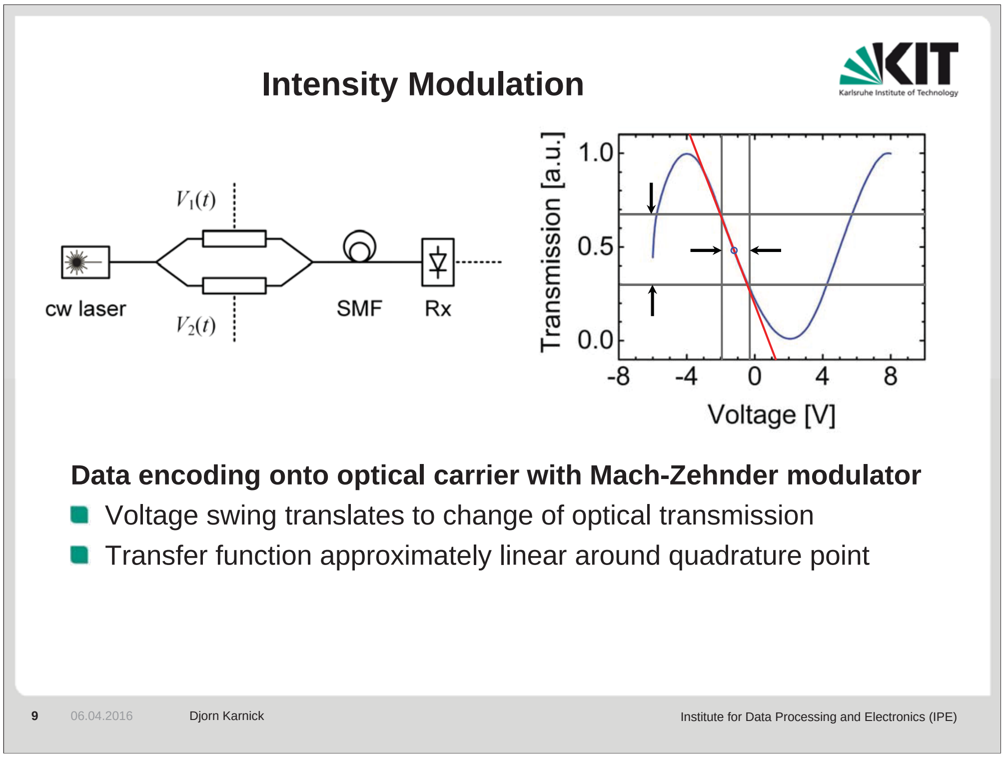


Intensity Modulation

Data encoding onto optical carrier with Mach-Zehnder modulator

- Modulation of the optical field’s phase in each interferometer arm
- Change of refractive index due to electro-optic effect
- Superposition of signals at the output yields either constructive or destructive interference depending on the relative phase



Intensity Modulation

Data encoding onto optical carrier with Mach-Zehnder modulator

- Voltage swing translates to change of optical transmission
- Transfer function approximately linear around quadrature point

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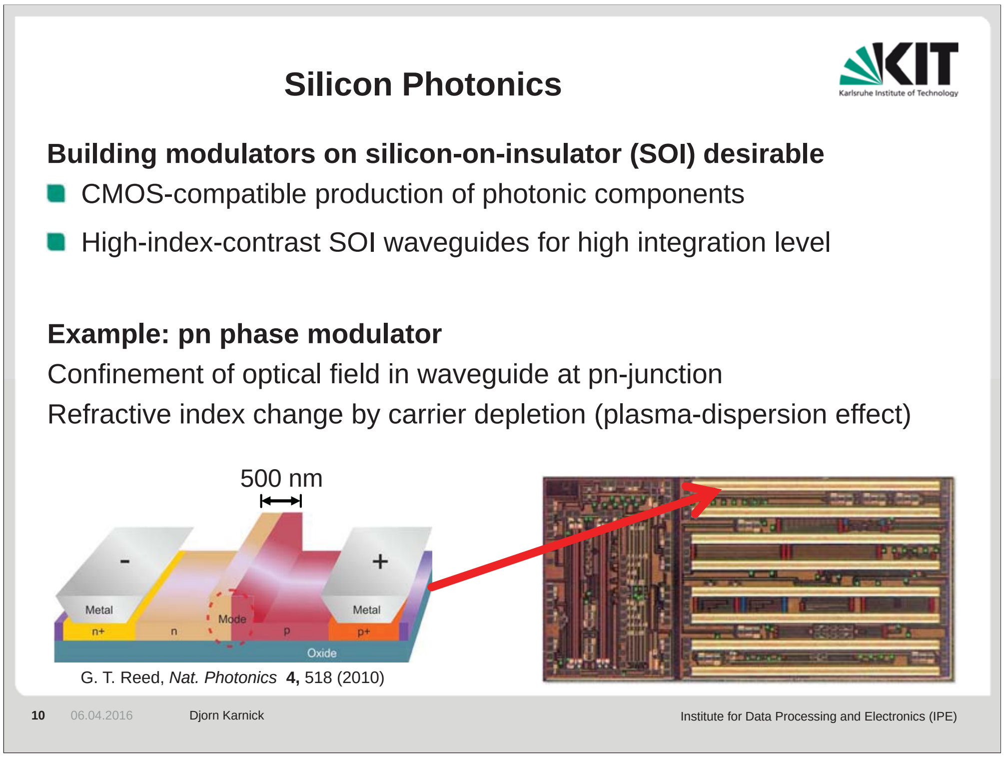

Silicon Photonics

Building modulators on silicon-on-insulator (SOI) desirable

- CMOS-compatible production of photonic components
- High-index-contrast SOI waveguides for high integration level

Example: pn phase modulator

Confinement of optical field in waveguide at pn-junction

Refractive index change by carrier depletion (plasma-dispersion effect)

G. T. Reed, *Nat. Photonics* **4,** 518 (2010)

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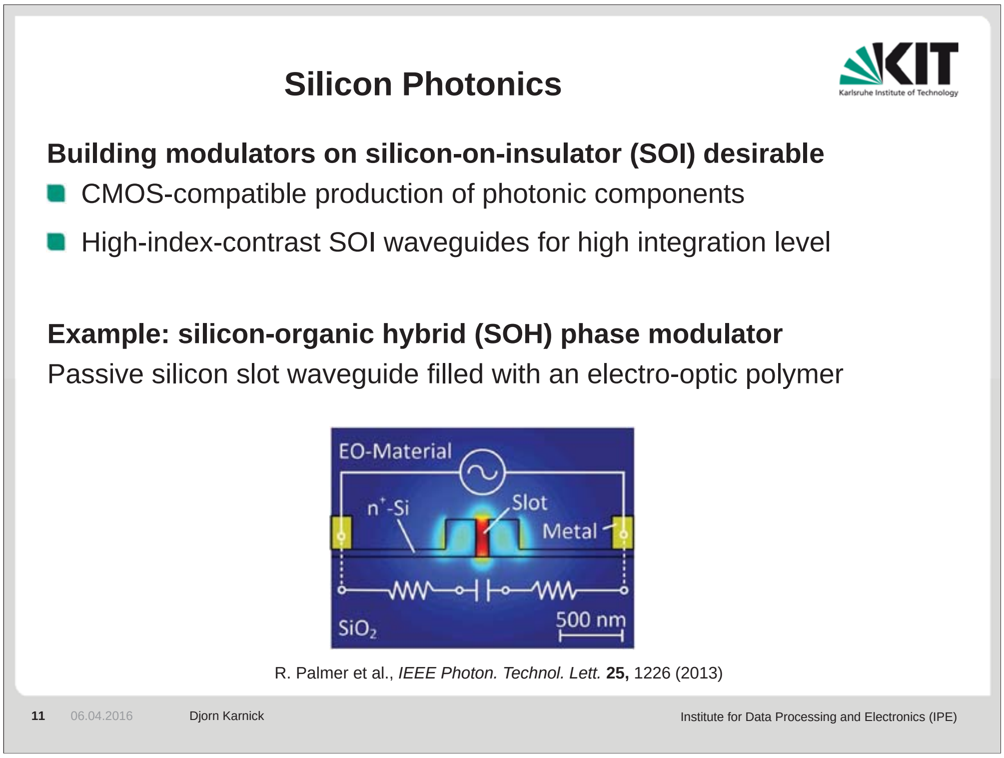


Silicon Photonics

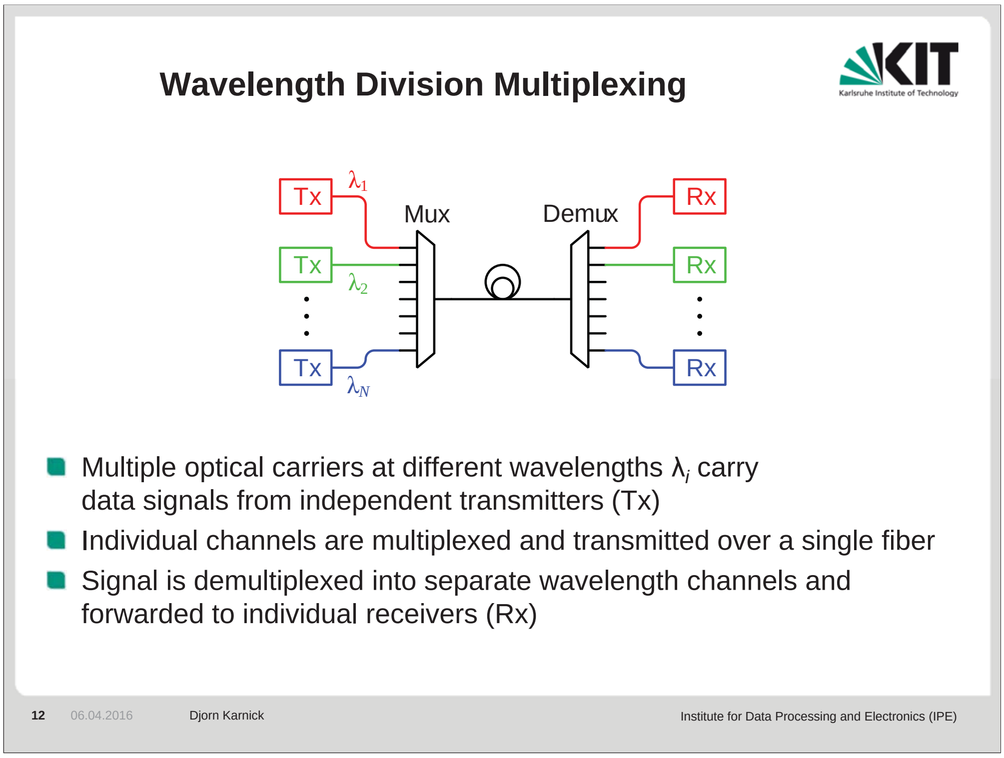
Building modulators on silicon-on-insulator (SOI) desirable

- CMOS-compatible production of photonic components
- High-index-contrast SOI waveguides for high integration level

Example: silicon-organic hybrid (SOH) phase modulator

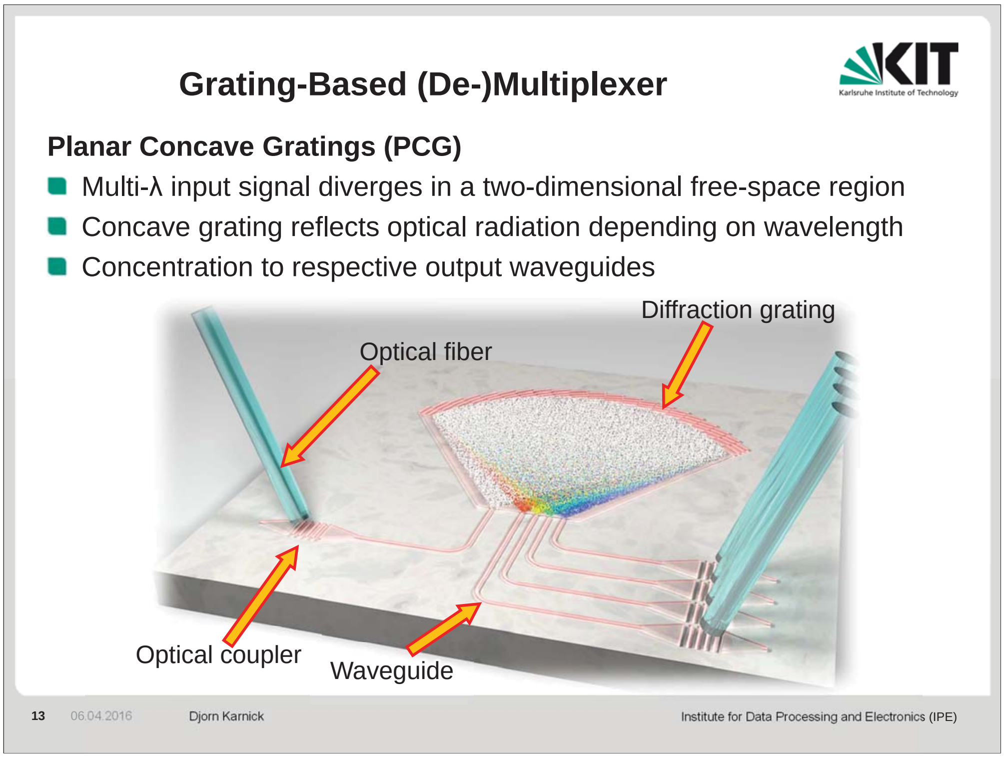
Passive silicon slot waveguide filled with an electro-optic polymer

R. Palmer et al., *IEEE Photon. Technol. Lett.* **25,** 1226 (2013)



Wavelength Division Multiplexing

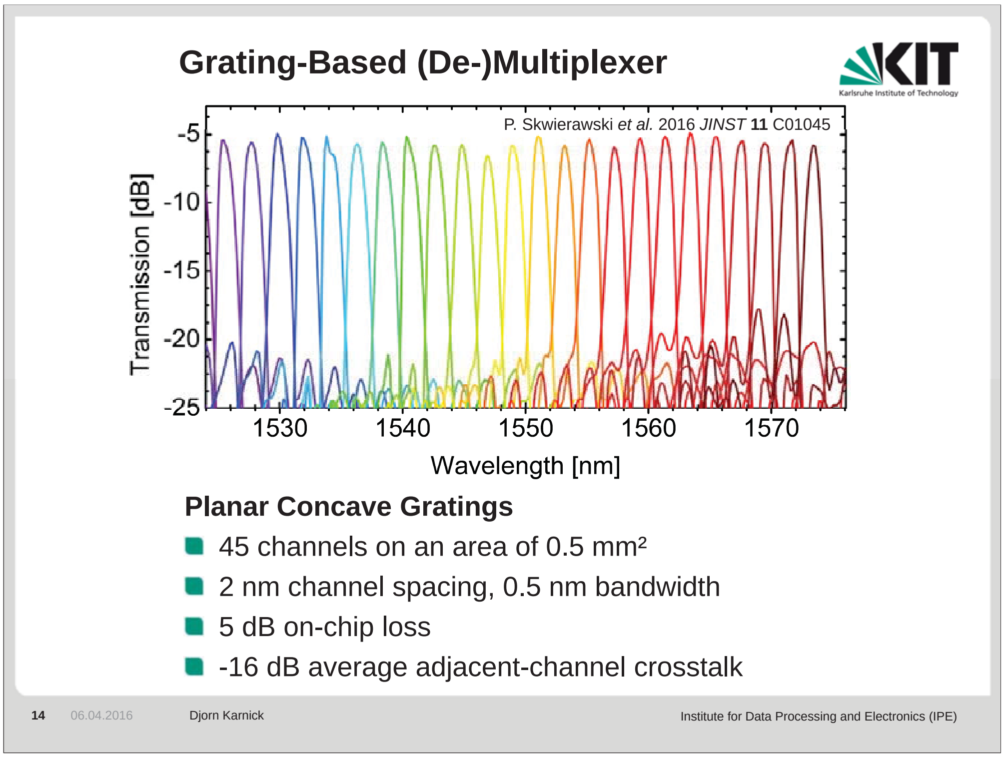
- Multiple optical carriers at different wavelengths λ_i carry data signals from independent transmitters (Tx)
- Individual channels are multiplexed and transmitted over a single fiber
- Signal is demultiplexed into separate wavelength channels and forwarded to individual receivers (Rx)



Grating-Based (De-)Multiplexer

Planar Concave Gratings (PCG)

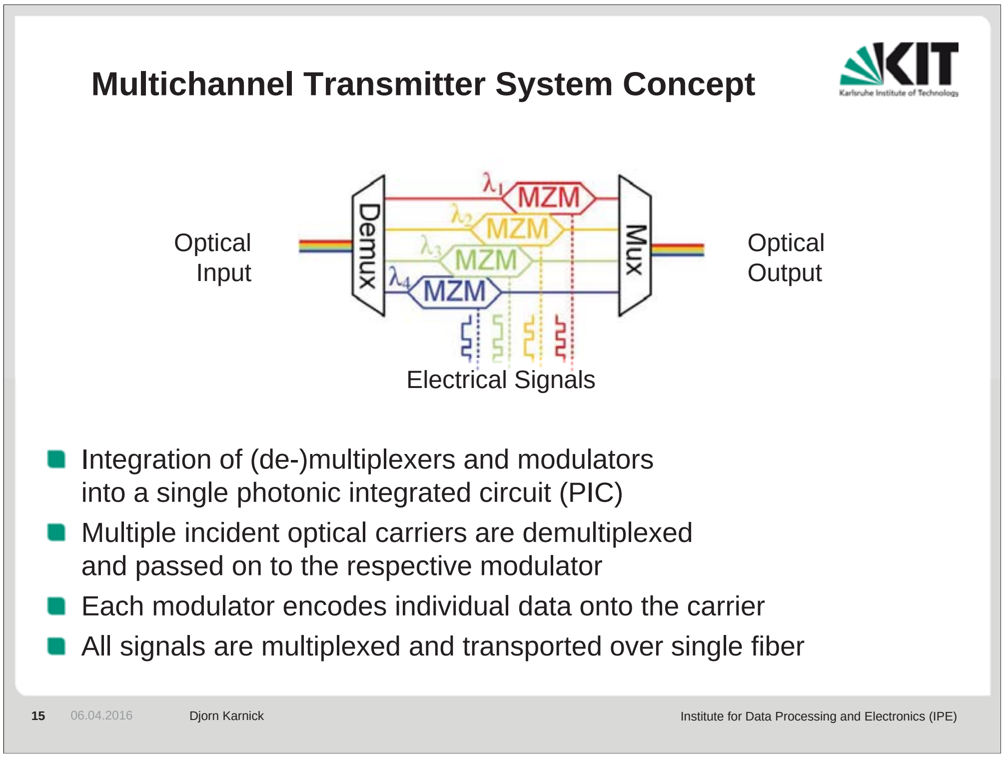
- Multi-λ input signal diverges in a two-dimensional free-space region
- Concave grating reflects optical radiation depending on wavelength
- Concentration to respective output waveguides



Grating-Based (De-)Multiplexer

Planar Concave Gratings

- 45 channels on an area of 0.5 mm²
- 2 nm channel spacing, 0.5 nm bandwidth
- 5 dB on-chip loss
- -16 dB average adjacent-channel crosstalk



Multichannel Transmitter System Concept

- Integration of (de-)multiplexers and modulators into a single photonic integrated circuit (PIC)
- Multiple incident optical carriers are demultiplexed and passed on to the respective modulator
- Each modulator encodes individual data onto the carrier
- All signals are multiplexed and transported over single fiber

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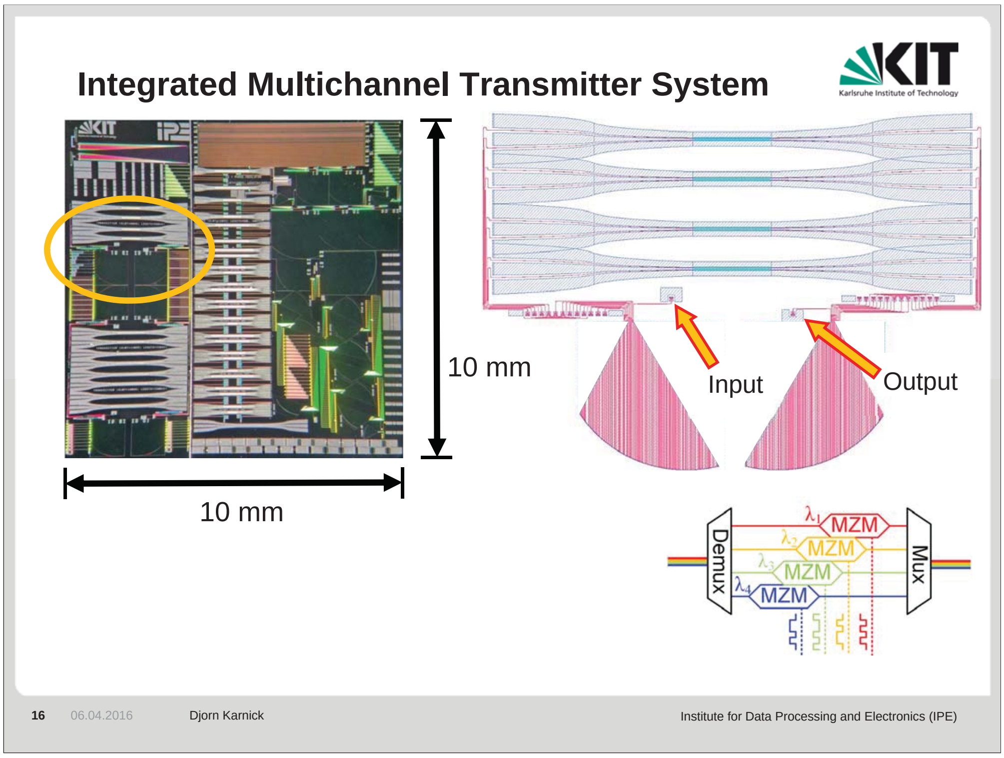

Integrated Multichannel Transmitter System

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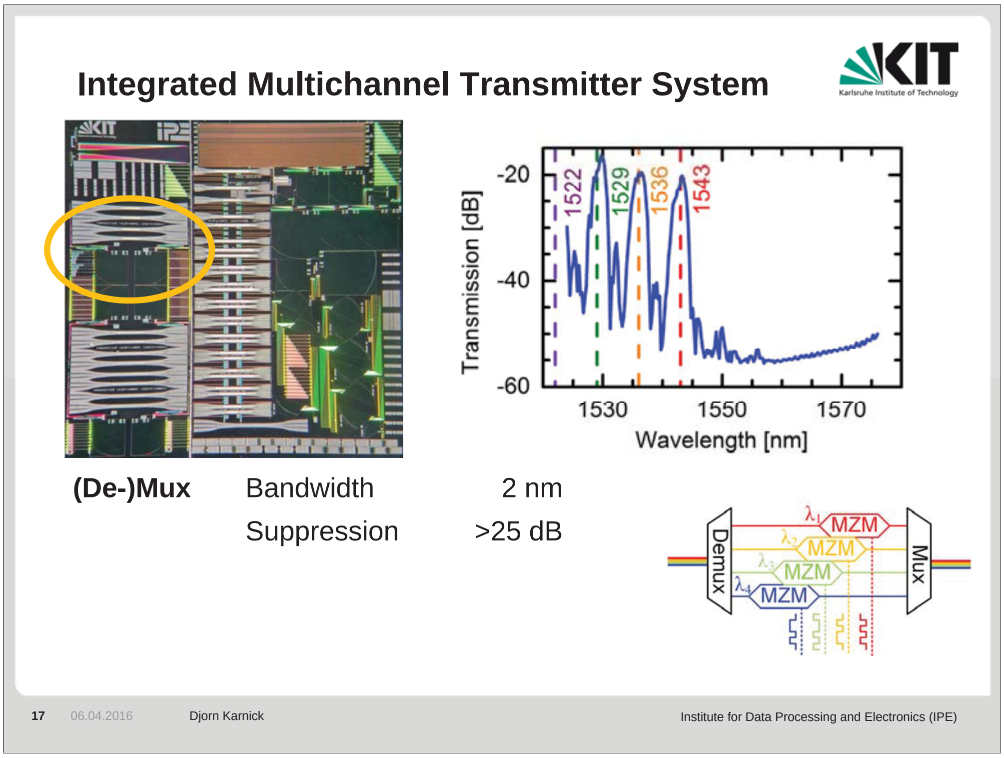

Integrated Multichannel Transmitter System

(De-)Mux	Bandwidth	2 nm
	Suppression	>25 dB

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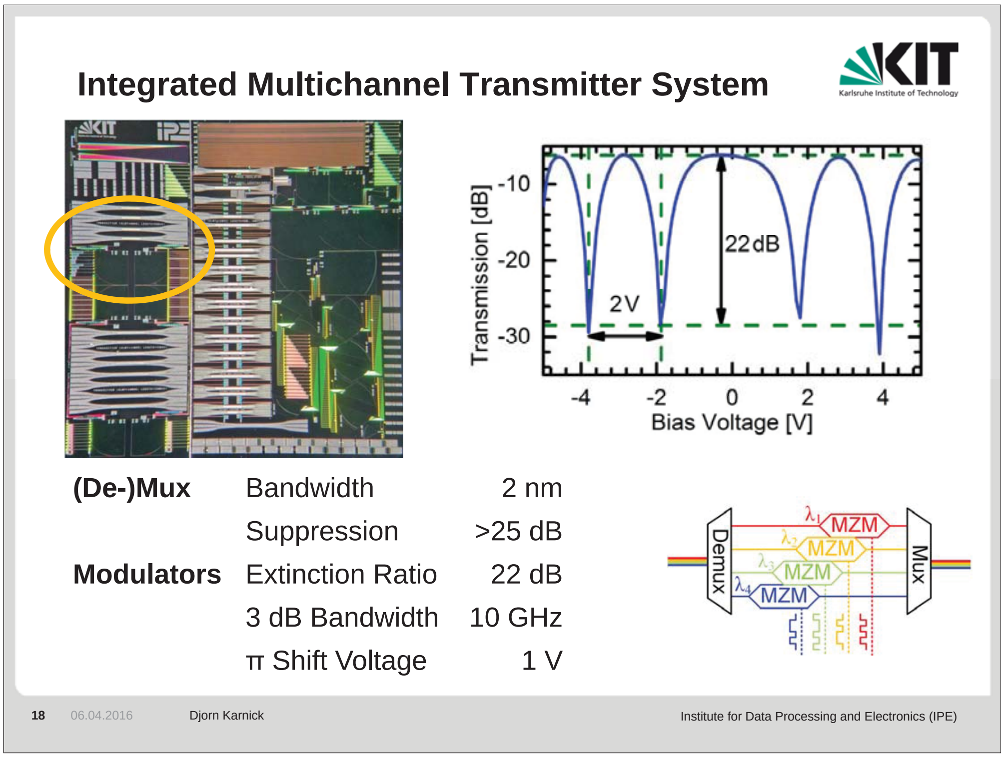

Integrated Multichannel Transmitter System

(De-)Mux	Bandwidth	2 nm
	Suppression	>25 dB
Modulators	Extinction Ratio	22 dB
	3 dB Bandwidth	10 GHz
	π Shift Voltage	1 V

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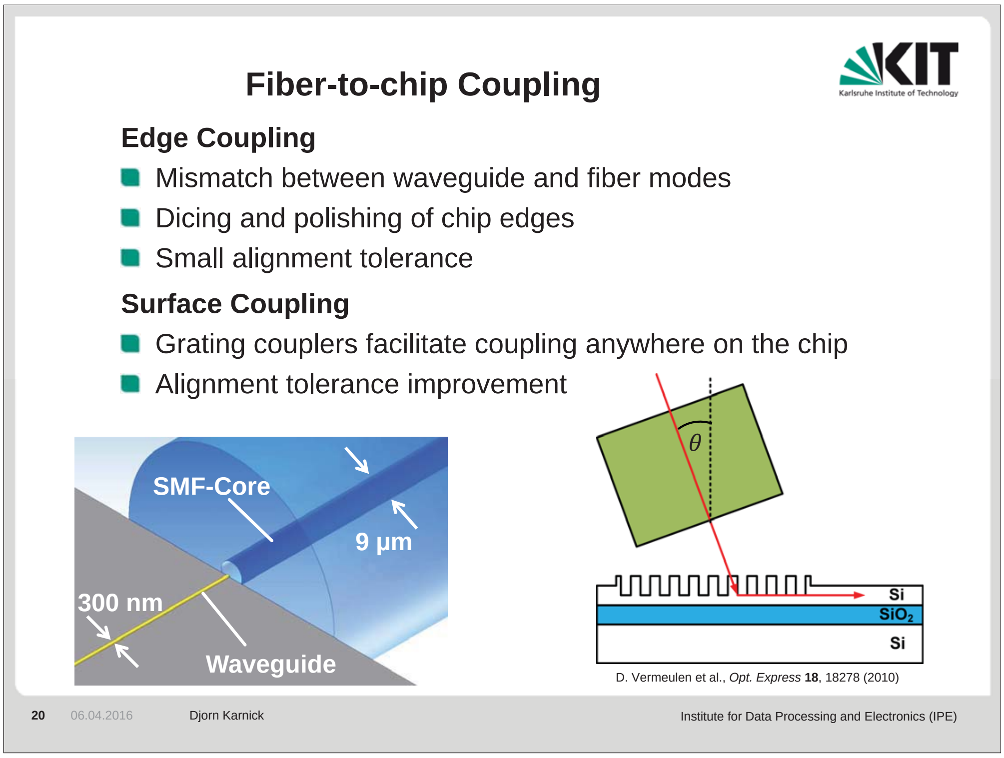


Fiber-to-chip Coupling

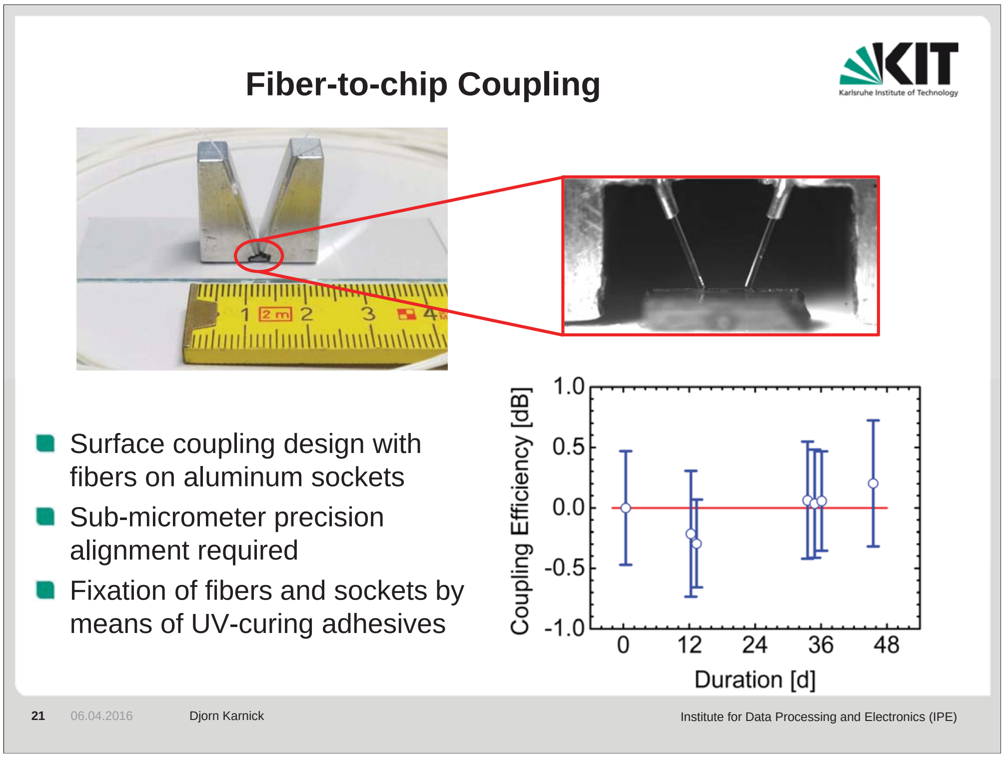
Edge Coupling

- Mismatch between waveguide and fiber modes
- Dicing and polishing of chip edges
- Small alignment tolerance

Surface Coupling

- Grating couplers facilitate coupling anywhere on the chip
- Alignment tolerance improvement

D. Vermeulen et al., *Opt. Express* **18**, 18278 (2010)



Fiber-to-chip Coupling

- Surface coupling design with fibers on aluminum sockets
- Sub-micrometer precision alignment required
- Fixation of fibers and sockets by means of UV-curing adhesives

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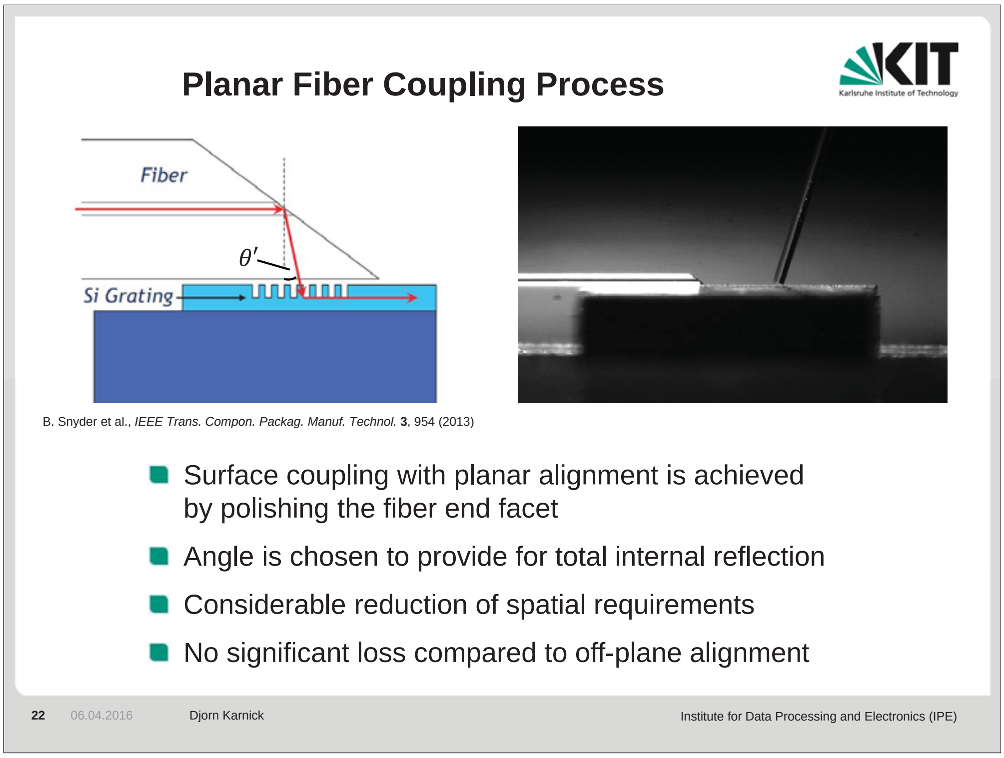

Planar Fiber Coupling Process

B. Snyder et al., *IEEE Trans. Compon. Packag. Manuf. Technol.* **3**, 954 (2013)

- Surface coupling with planar alignment is achieved by polishing the fiber end facet
- Angle is chosen to provide for total internal reflection
- Considerable reduction of spatial requirements
- No significant loss compared to off-plane alignment

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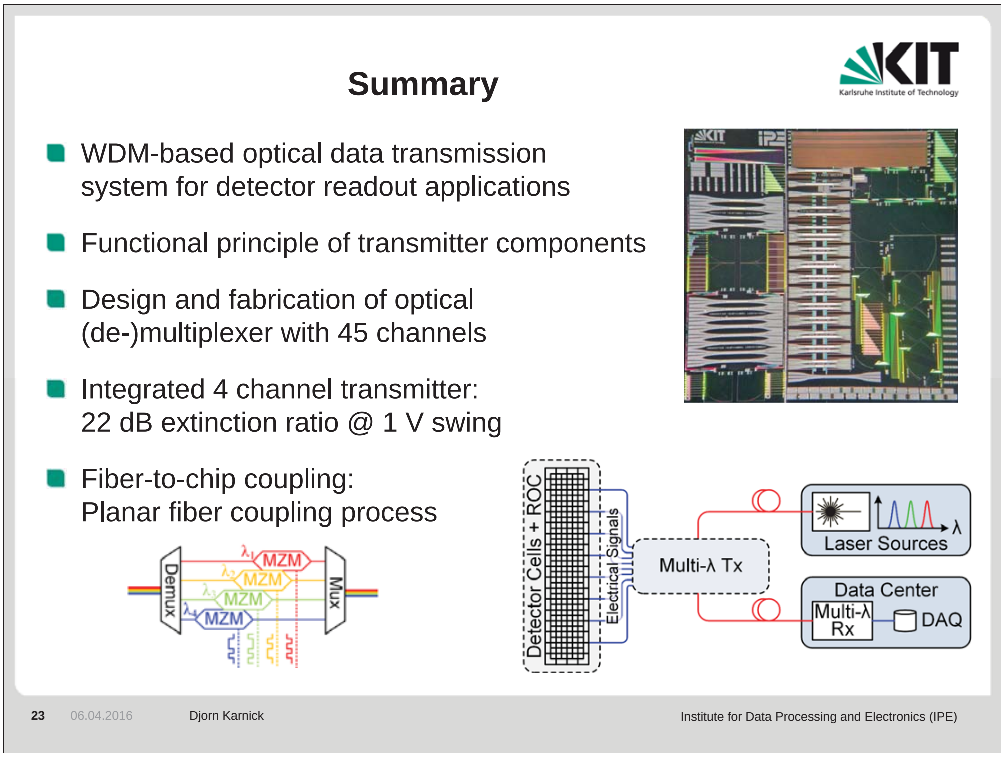

Summary

- WDM-based optical data transmission system for detector readout applications
- Functional principle of transmitter components
- Design and fabrication of optical (de-)multiplexer with 45 channels
- Integrated 4 channel transmitter: 22 dB extinction ratio @ 1 V swing
- Fiber-to-chip coupling: Planar fiber coupling process

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Mitglied der Helmholtz-Gemeinschaft

SEI Tagung 2016

Maria @ FRM2 eine EMV Begutachtung

Apr 2016 | G. Vehres

Überblick

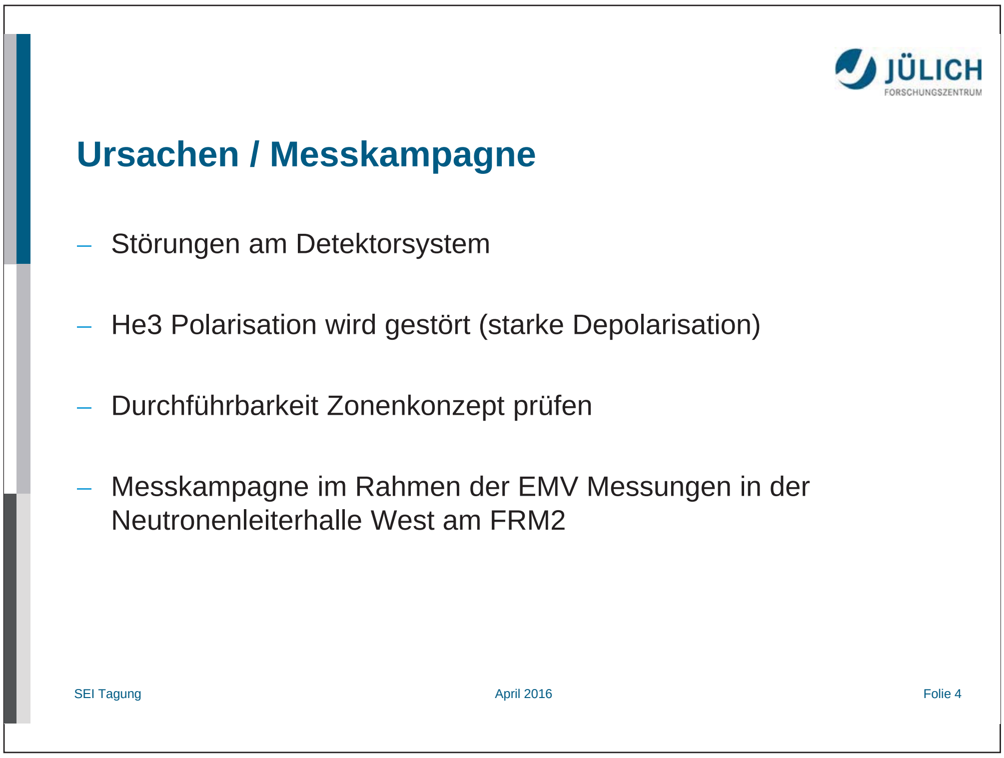
- Ursachen / Messkampagne
- Grundlagen / Geräte
- Vorgehensweise / Durchführung
- Ergebnisse
- Schlussfolgerungen
- Maßnahmen

JÜLICH
FORSCHUNGSZENTRUM

Das Instrument Maria am FRM2

Quelle: Forschungsneutronenquelle Heinz Maier Leibnitz W.Schürmann

SEI Tagung April 2016 Folie 3

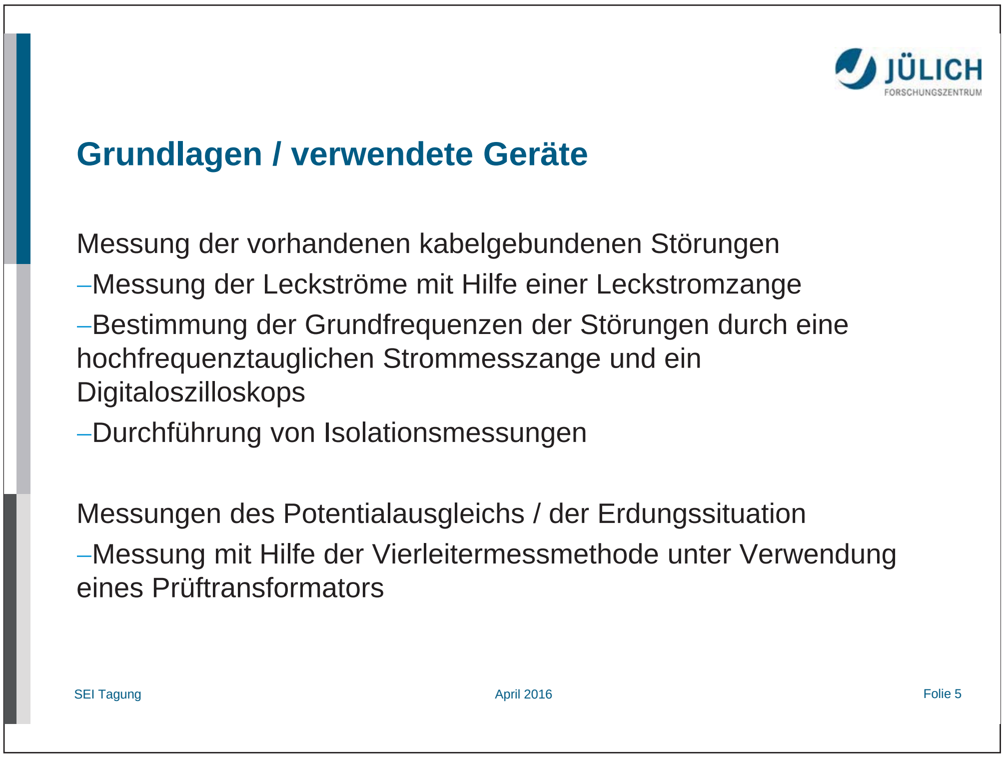


JÜLICH
FORSCHUNGSZENTRUM

Ursachen / Messkampagne

- Störungen am Detektorsystem
- He3 Polarisation wird gestört (starke Depolarisation)
- Durchführbarkeit Zonenkonzept prüfen
- Messkampagne im Rahmen der EMV Messungen in der Neutronenleiterhalle West am FRM2

SEI Tagung April 2016 Folie 4



Grundlagen / verwendete Geräte

Messung der vorhandenen kabelgebundenen Störungen

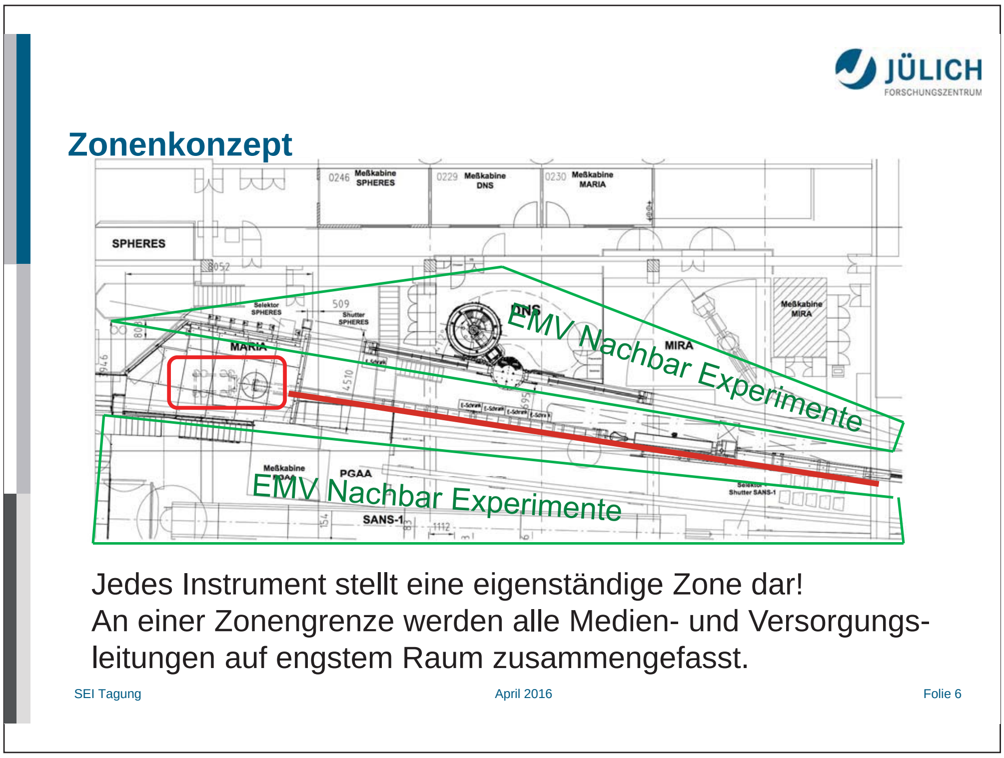
–Messung der Leckströme mit Hilfe einer Leckstromzange

–Bestimmung der Grundfrequenzen der Störungen durch eine hochfrequenztauglichen Strommesszange und ein Digitaloszilloskops

–Durchführung von Isolationsmessungen

Messungen des Potentialausgleichs / der Erdungssituation

–Messung mit Hilfe der Vierleitermessmethode unter Verwendung eines Prüftransformators



Zonenkonzept

Jedes Instrument stellt eine eigenständige Zone dar!
An einer Zonengrenze werden alle Medien- und Versorgungsleitungen auf engstem Raum zusammengefasst.

Vorgehensweise / Durchführung

1) Bestimmung der Grundfrequenzen
   - In den Zuleitungen zum Energieverteiler des Detektorarms
   - In den Zuleitungen zum He3 Polarisationssystems
   - In der Zuleitung zu den Motoren am Detektorarm
   - Am Potentialausgleich des Detektorarms
   - Am Potentialausgleich der Hexapodsteuerung

2) Bestimmung des ohmschen Wiederstandes der Verbindung zwischen PA Sternpunkt und Teilen des Instruments mit Hilfe einer Vierleiter Messmethode

Vorgehensweise / Durchführung Leckstrom

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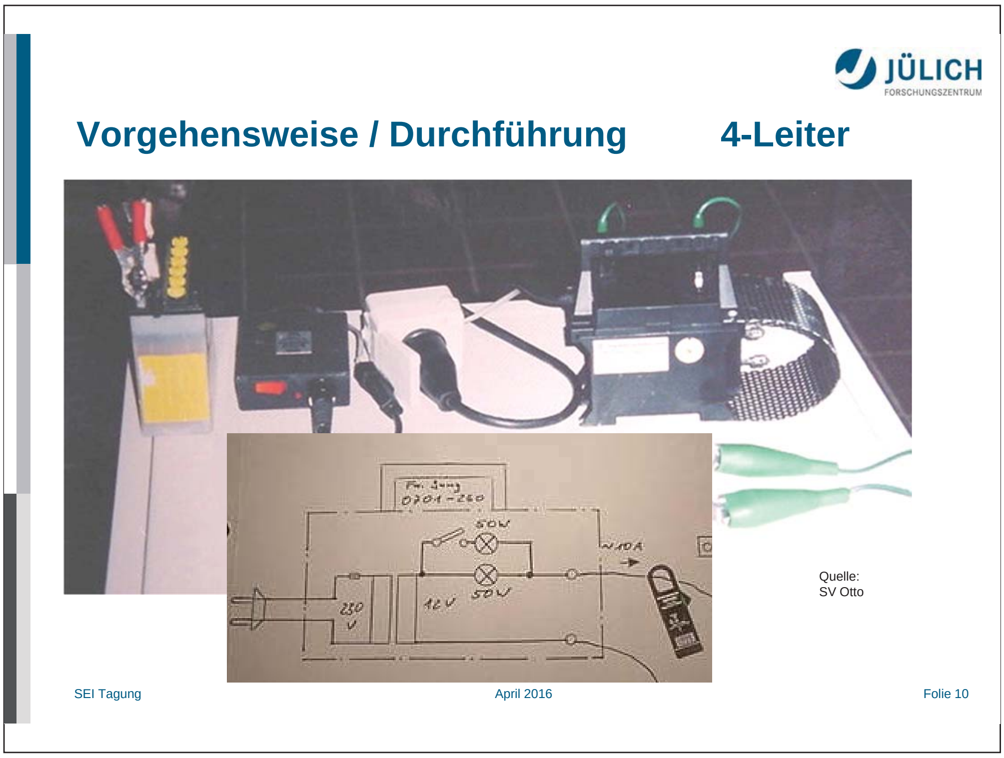
Vorgehensweise / Durchführung HF



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Vorgehensweise / Durchführung 4-Leiter

Quelle:
SV Otto

Ergebnisse / Energieversorgung Detektor

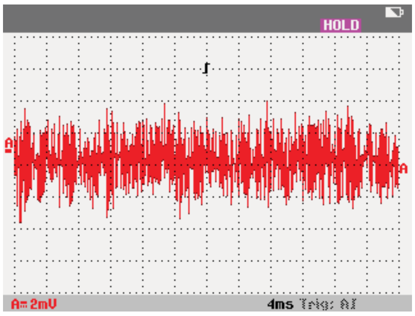
Am Energieverteiler des Detektorarms sind angeschlossen
- He3 Polarisation
- Detektorsystem

Leck- / Strommessung an der Zuleitung / PA
- Alles eingesteckt 62mA / 50mA
  Summe L1-L2-L3-N = Leckstrom 4,2mA
- Detektorsystem ausgesteckt 56mA / 40mA
- Alles ausgesteckt 0mA /12mA

Es fließt ein Strom über den PA ohne angeschlossene Verbraucher!

Wir führen daher einen Strom über den PE in der Zuleitung der dann durch unsere Geräten fliest! (PA?!)

Ergebnisse / Detektor

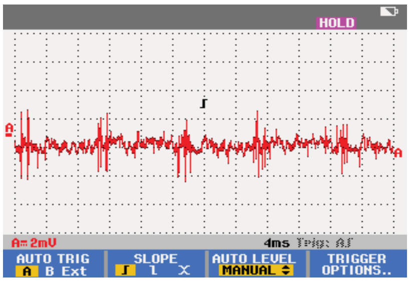


10mA/Unit

Hier ist ein Leckstrom mit einer Frequenz von 250kHz auf der Versorgungsleitung zum Siemens Rahmen des Detektors messbar.
Dieser ist abhängig von der der Lage der Kabel!

Die Flachbandkabel / Lemokabel sind vermutlich beschädigt
Isolationsfehler, der Detektor ist nicht mehr isoliert aufgebaut!

Ergebnisse Reibrad / Hexapod



Unstetiges Signal auf der Zuleitung zum Reibrad.

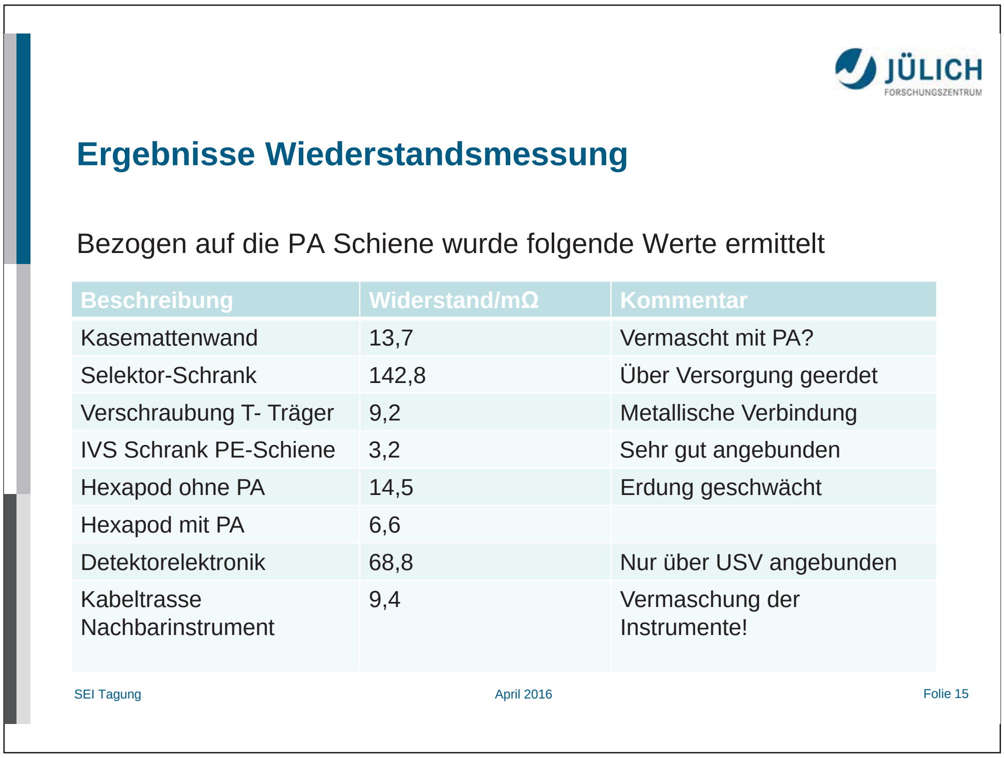
10mA/Unit 4ms/Unit

Das Motorkabel zum Reibrad führt eine PE Leitung und einen Schirm mit sich. Der Schirm ist wiederum mit dem PA /PE des weit entfernten Steuerschranks verbunden, auch das auf der Achse angebrachte Sensorkabel führt PA/PE mit sich. Schleifenbildung!

Ergebnisse Hexapod / Detektorarm

Erster Versuch:
PA Verbindung des Hexapod im Steuerschranks nicht mehr aufgelegt um Störungen auf Detektorarm zu verringern. Schleife schwächen!

- Entfernen des PA‘s unzulässig / Gefährdung.
- Metallische Verbindung zwischen Probenort / Hexapod und Detektorarm durch Befestigungsblech.
- Mehrere PE Verbindungen über Leitungswege.



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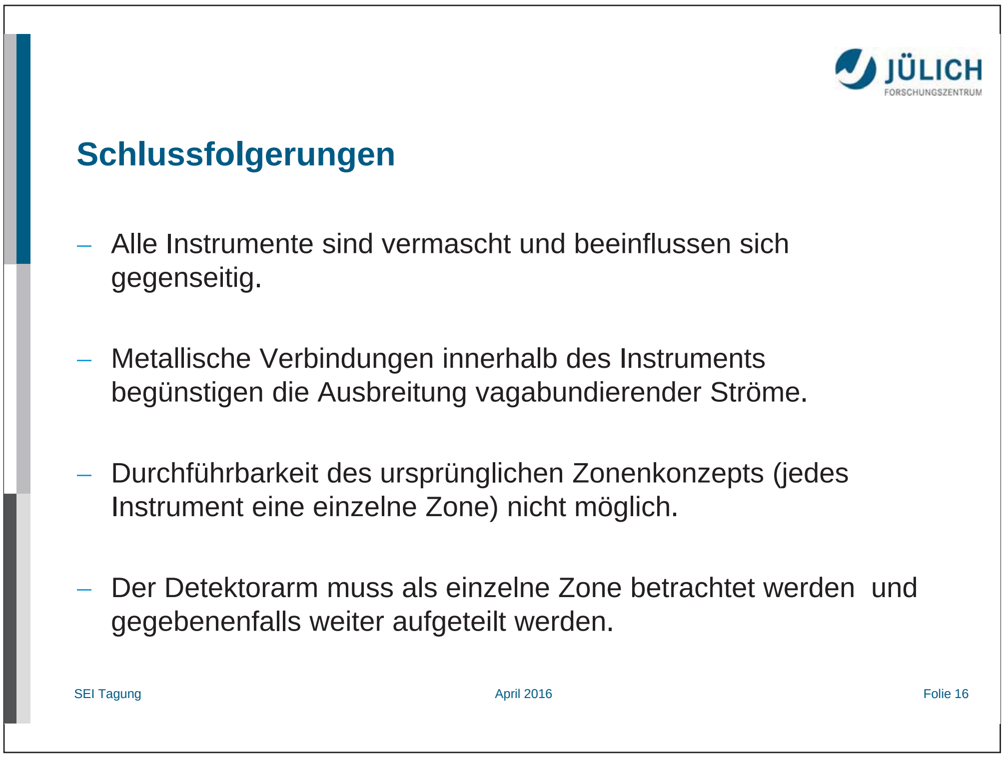
Ergebnisse Wiederstandsmessung

Bezogen auf die PA Schiene wurde folgende Werte ermittelt

Beschreibung	Widerstand/mΩ	Kommentar
Kasemattenwand	13,7	Vermascht mit PA?
Selektor-Schrank	142,8	Über Versorgung geerdet
Verschraubung T- Träger	9,2	Metallische Verbindung
IVS Schrank PE-Schiene	3,2	Sehr gut angebunden
Hexapod ohne PA	14,5	Erdung geschwächt
Hexapod mit PA	6,6	
Detektorelektronik	68,8	Nur über USV angebunden
Kabeltrasse Nachbarinstrument	9,4	Vermaschung der Instrumente!



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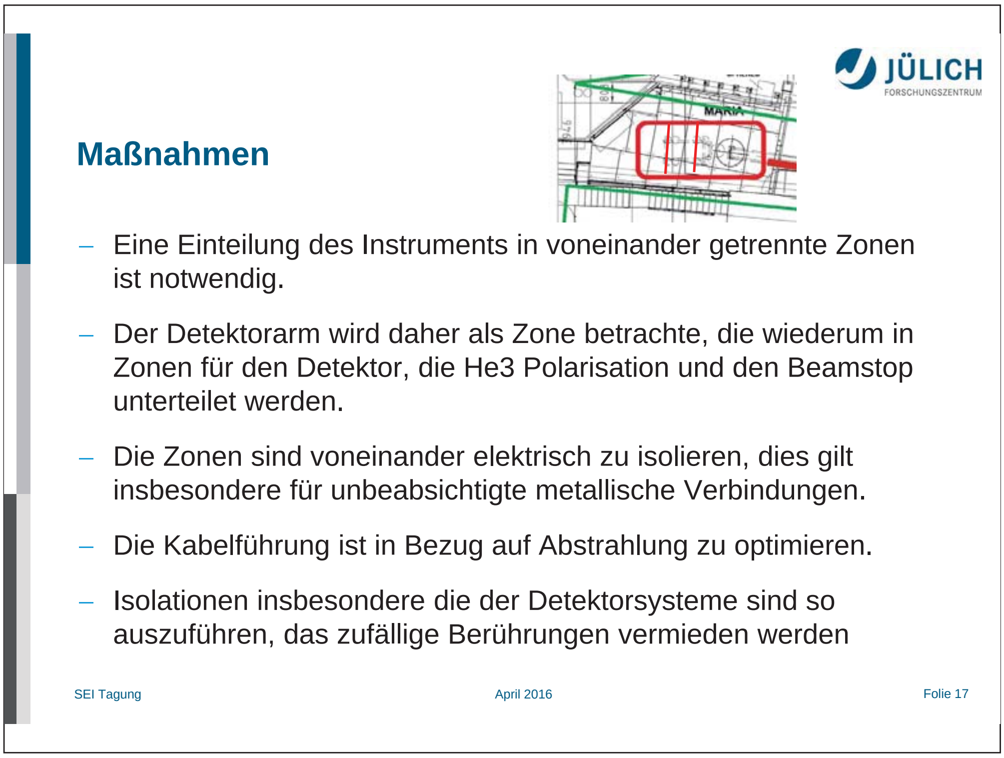
Schlussfolgerungen

- Alle Instrumente sind vermascht und beeinflussen sich gegenseitig.
- Metallische Verbindungen innerhalb des Instruments begünstigen die Ausbreitung vagabundierender Ströme.
- Durchführbarkeit des ursprünglichen Zonenkonzepts (jedes Instrument eine einzelne Zone) nicht möglich.
- Der Detektorarm muss als einzelne Zone betrachtet werden und gegebenenfalls weiter aufgeteilt werden.



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Maßnahmen

- Eine Einteilung des Instruments in voneinander getrennte Zonen ist notwendig.
- Der Detektorarm wird daher als Zone betrachte, die wiederum in Zonen für den Detektor, die He3 Polarisation und den Beamstop unterteilet werden.
- Die Zonen sind voneinander elektrisch zu isolieren, dies gilt insbesondere für unbeabsichtigte metallische Verbindungen.
- Die Kabelführung ist in Bezug auf Abstrahlung zu optimieren.
- Isolationen insbesondere die der Detektorsysteme sind so auszuführen, das zufällige Berührungen vermieden werden

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JÜLICH
FORSCHUNGSZENTRUM

Mitwirkende

- Dr. Peter Göttlicher (Desy)
- Dr. Stefan Mattauch (JCNS)
- Ulrich Bünten (JCNS-1)
- Vladimier Ossovy (JCNS)
- Andreas Nebel (JCNS)
- Abt. G-ELI (Forschungszentrum Jülich)
- Dr. Nikolas Arend (JCNS)

Vielen Dank an alle Mitwirkenden.

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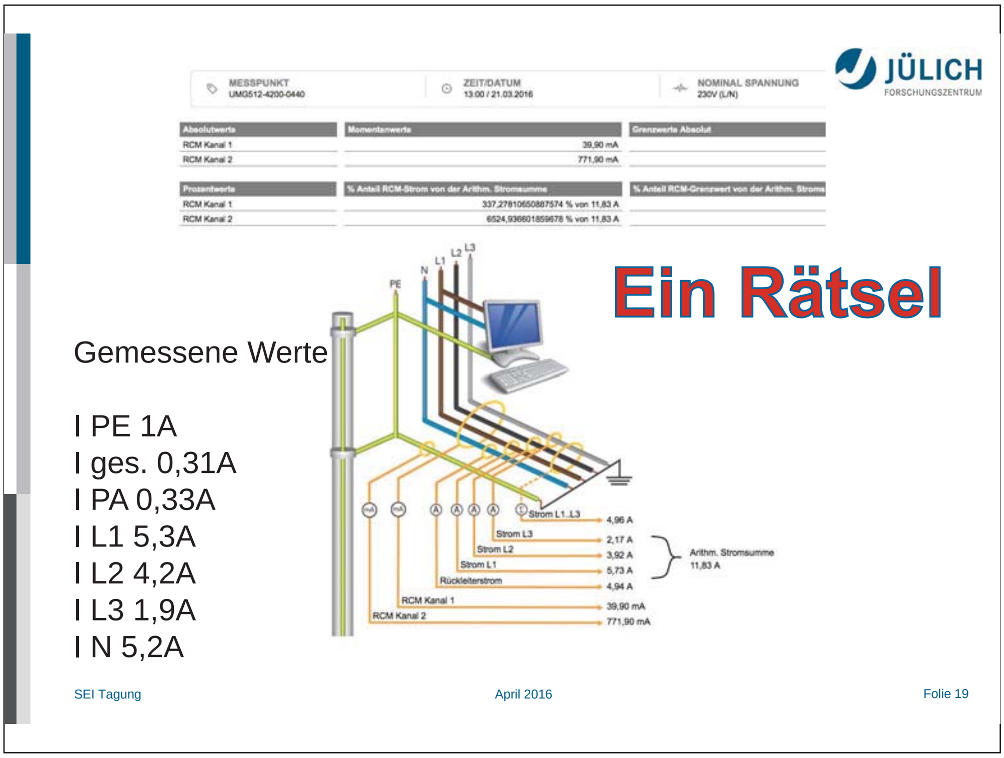


MESSPUNKT
UMG512-4200-0440

ZEIT/DATUM
13:00 / 21.03.2016

NOMINAL SPANNUNG
230V (L/N)

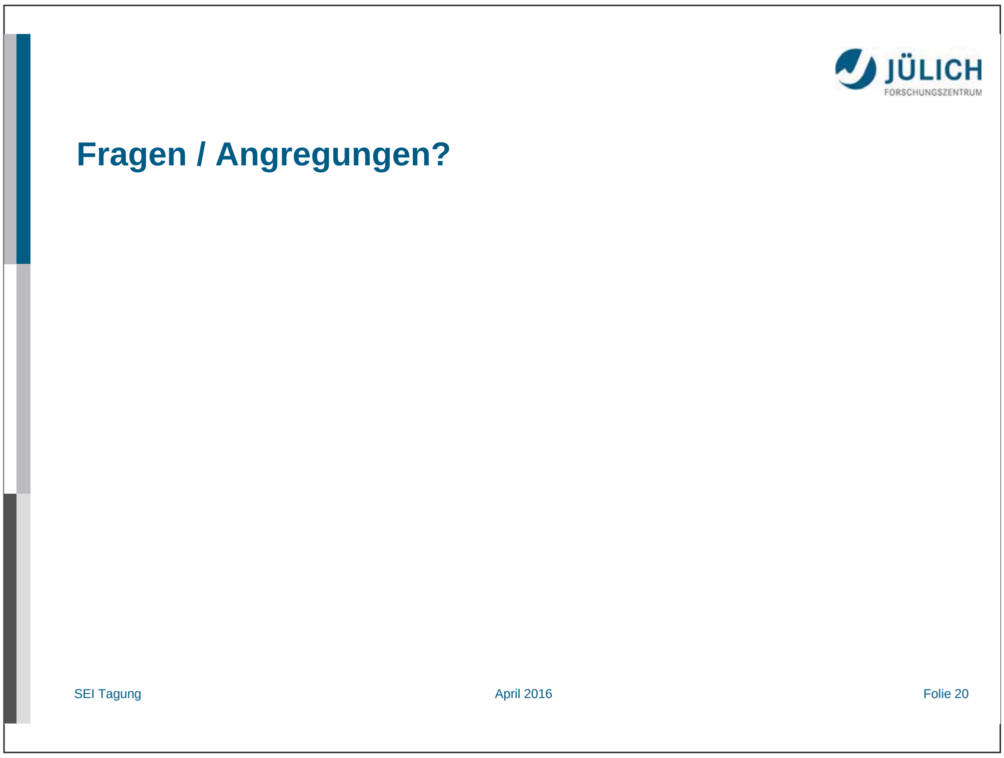
Absolutwerte	Momentanwerte	Grenzwerte Absolut
RCM Kanal 1	39,90 mA	
RCM Kanal 2	771,90 mA	

Prozentwerte	% Anteil RCM-Strom von der Arithm. Stromsumme	% Anteil RCM-Grenzwert von der Arithm. Stroms
RCM Kanal 1	337,27810650887574 % von 11,83 A	
RCM Kanal 2	6524,936601859678 % von 11,83 A	

Ein Rätsel

Gemessene Werte

I PE 1A
I ges. 0,31A
I PA 0,33A
I L1 5,3A
I L2 4,2A
I L3 1,9A
I N 5,2A



Fragen / Angregungen?

Quench Detectors for FAIR

Samuel Ayet San Andrés

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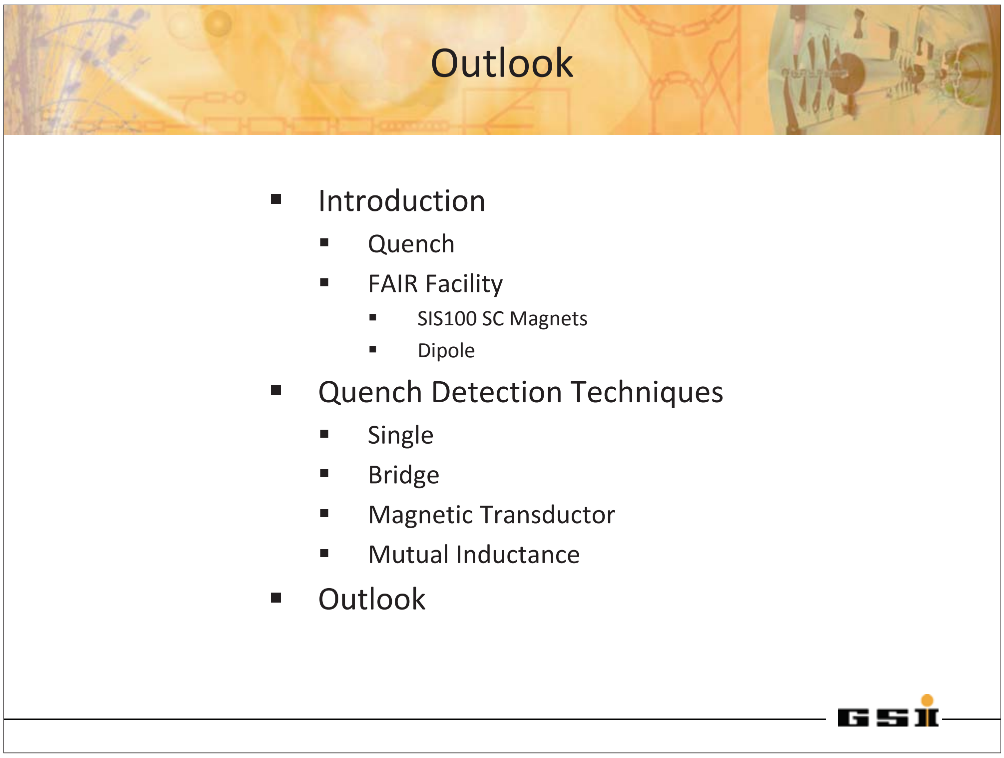
FAIR Facility for Antiproton and Ion Research in Europe GmbH

Studiengruppe für
Elektronische Instrumentierung

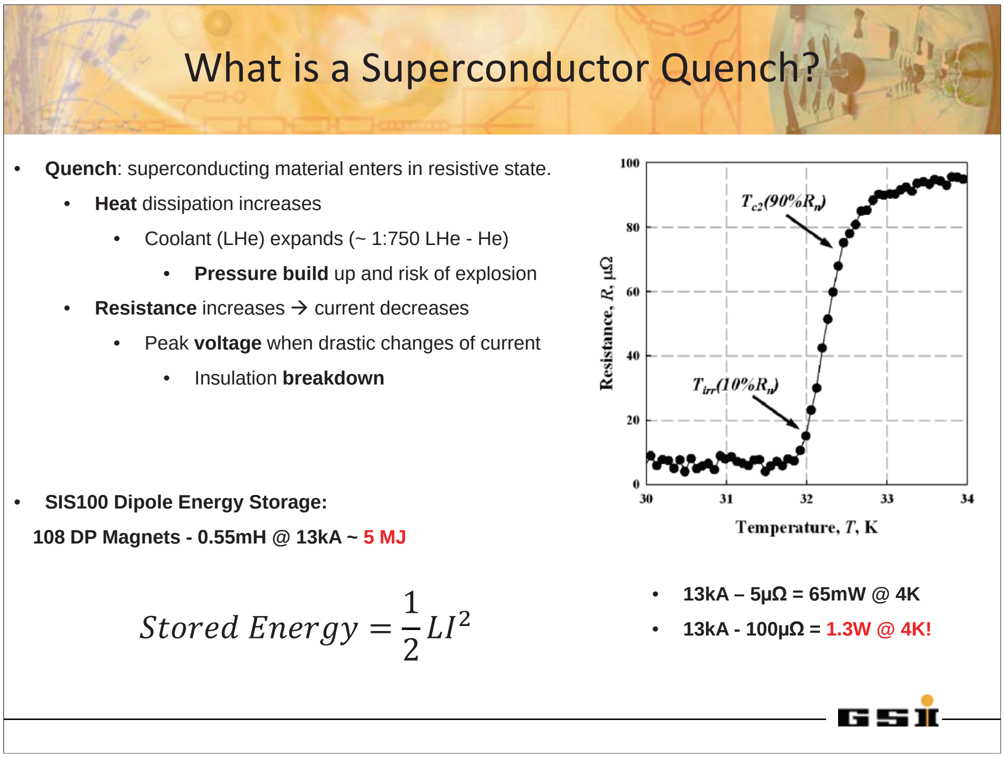
GSI



Outlook

- Introduction
  - Quench
  - FAIR Facility
    - SIS100 SC Magnets
    - Dipole
- Quench Detection Techniques
  - Single
  - Bridge
  - Magnetic Transductor
  - Mutual Inductance
- Outlook

GSI



What is a Superconductor Quench?

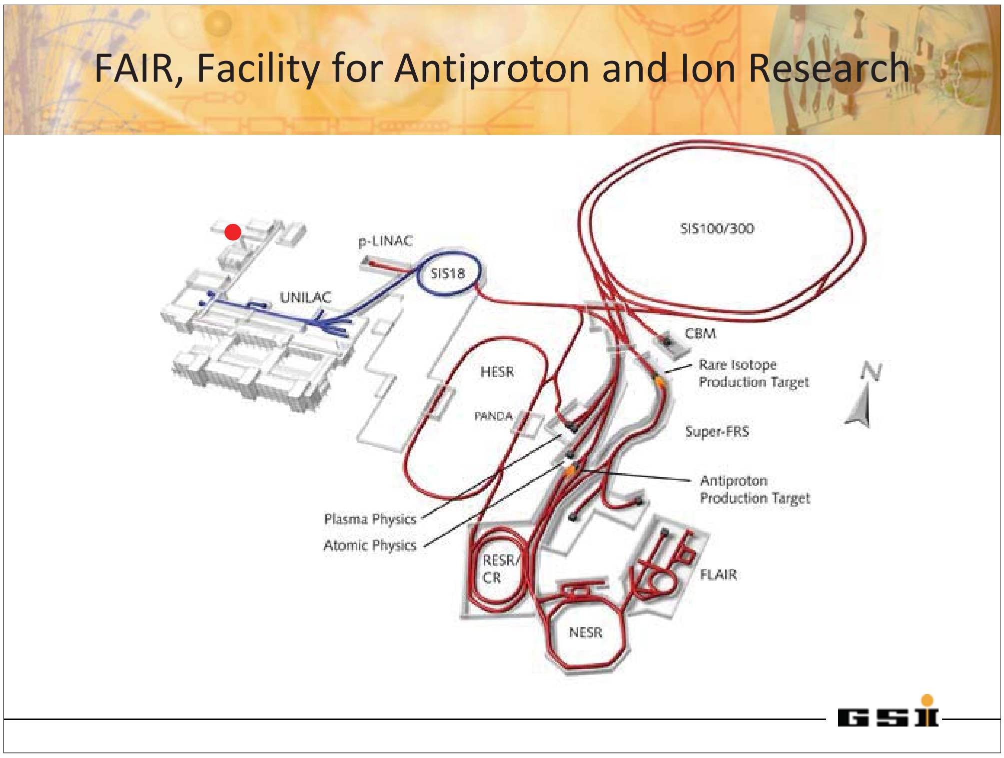
- **Quench**: superconducting material enters in resistive state.
  - **Heat** dissipation increases
    - Coolant (LHe) expands (~ 1:750 LHe - He)
      - **Pressure build** up and risk of explosion
  - **Resistance** increases → current decreases
    - Peak **voltage** when drastic changes of current
      - Insulation **breakdown**

- **SIS100 Dipole Energy Storage:**

108 DP Magnets - 0.55mH @ 13kA ~ 5 MJ

$$Stored\ Energy = \frac{1}{2}LI^2$$

- **13kA – 5μΩ = 65mW @ 4K**
- **13kA - 100μΩ = 1.3W @ 4K!**



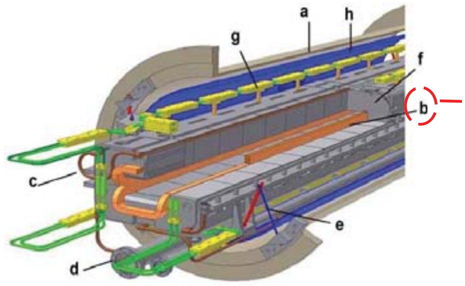
FAIR, Facility for Antiproton and Ion Research

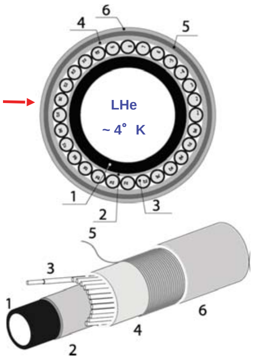
SIS100 Magnets

Magnet Type	Quantity | Circuits	Inductive Voltage (V)	Inductance (mH)	Current (kA)
Main Dipole	108 | 1	15.4	0.55	13.1
Main Quadrupoles	166 | 3	7.5	0.41	10.512
Chromaticity Sextupoles	42 | 7	62	43	0.25
Steer Dipole	83 | 166	25	21	0.25
Multipole Corrector	12 | 36	1.8-7.7	1.1-7.4	0.25
Injection/Extraction Quadrupole	4 | 16	147	139	0.5

...and current leads!

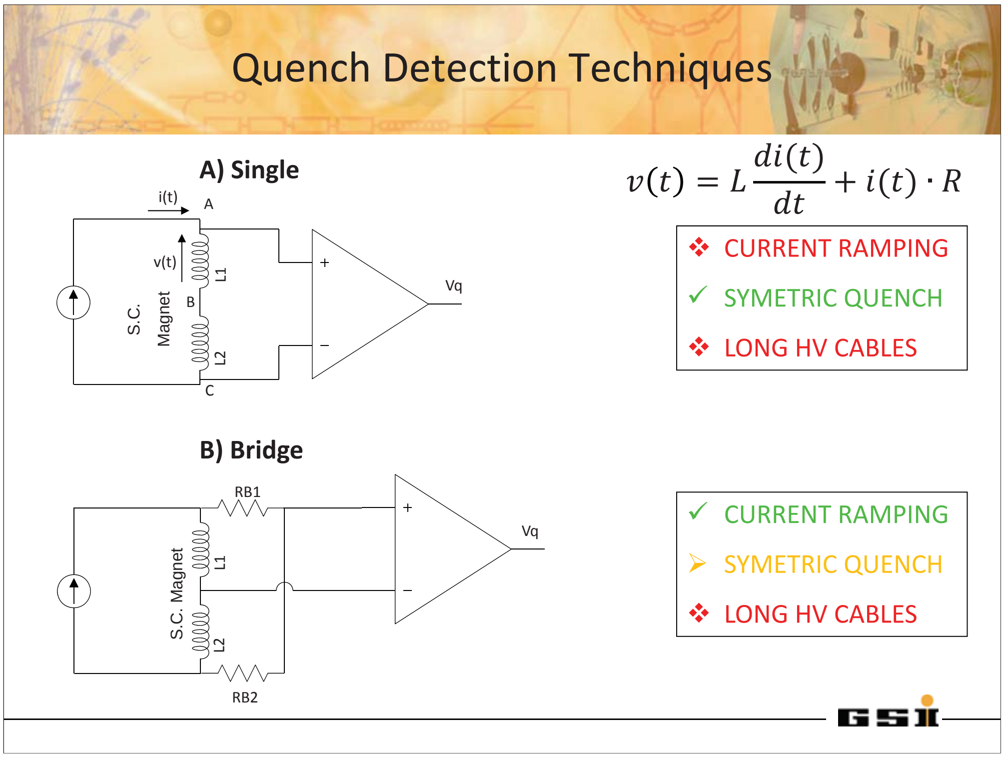
Example SIS100 Dipole





- SIS100 Dipole Design
    - a.- Cryostat Vessel
    - b.- Half Superconducting Coil
    - c.- Yoke and Cooling Pipes
    - d.- Liquid He Lines
    - e.- Suspension Rods
    - f.- Soft iron yoke
    - g.- Bus bars
    - h.- Thermal shield

- SC Cable
    - 1.- 4mm CuNi tube (Liquid He Flow)
    - 2.- (Kapton Insulation Layer)
    - 3.- Superconducting Strands
    - 4.- Kapton Insulation Layer
    - 5.- CrNi Wire for Fixation
    - 6.- Kapton Insulation Layer



Quench Detection Techniques

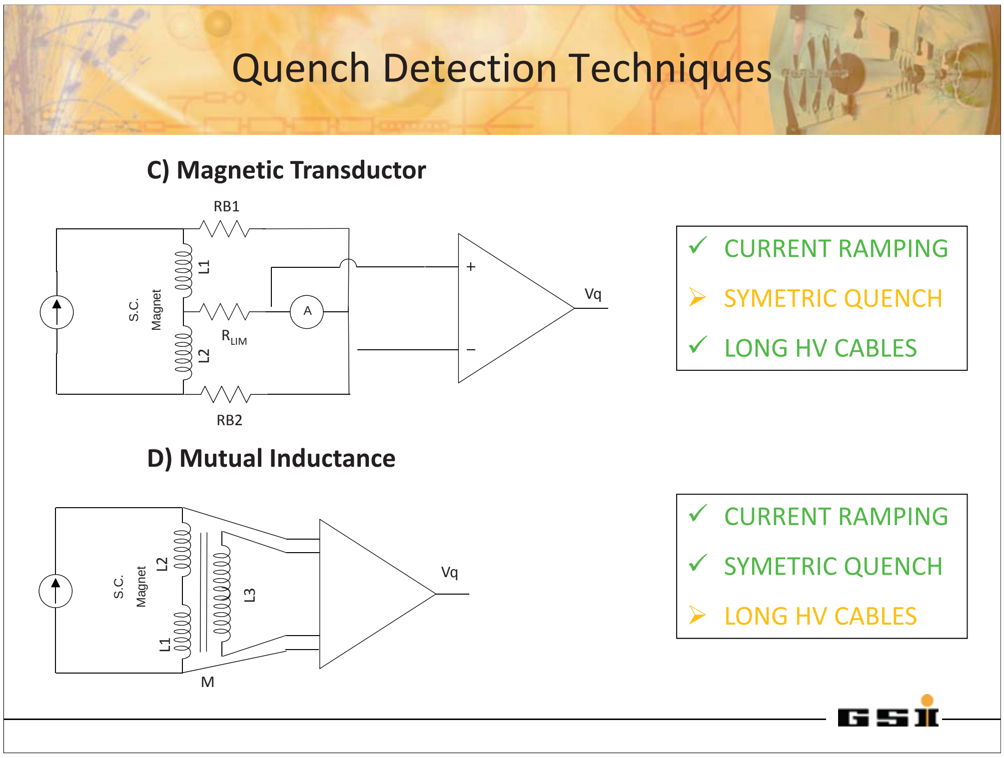
A) Single

$$v(t) = L\frac{di(t)}{dt} + i(t) \cdot R$$

- ❖ CURRENT RAMPING
- ✓ SYMETRIC QUENCH
- ❖ LONG HV CABLES

B) Bridge

- ✓ CURRENT RAMPING
- ➢ SYMETRIC QUENCH
- ❖ LONG HV CABLES



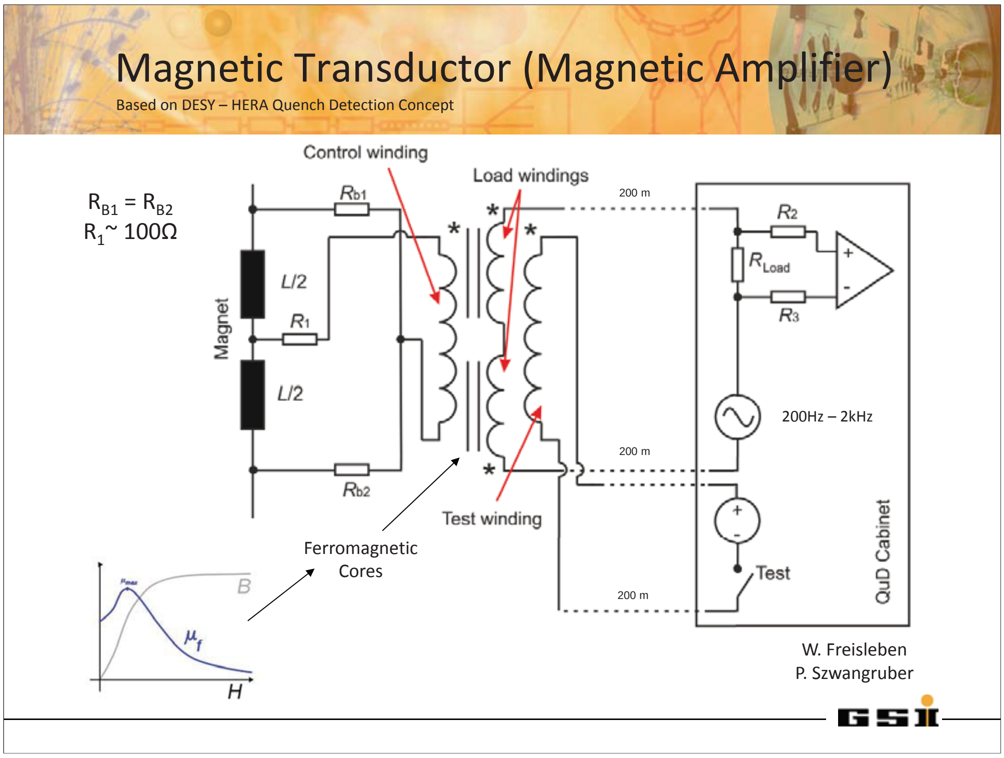
Quench Detection Techniques

C) Magnetic Transductor

- ✓ CURRENT RAMPING
- ➢ SYMETRIC QUENCH
- ✓ LONG HV CABLES

D) Mutual Inductance

- ✓ CURRENT RAMPING
- ✓ SYMETRIC QUENCH
- ➢ LONG HV CABLES



Magnetic Transductor (Magnetic Amplifier)

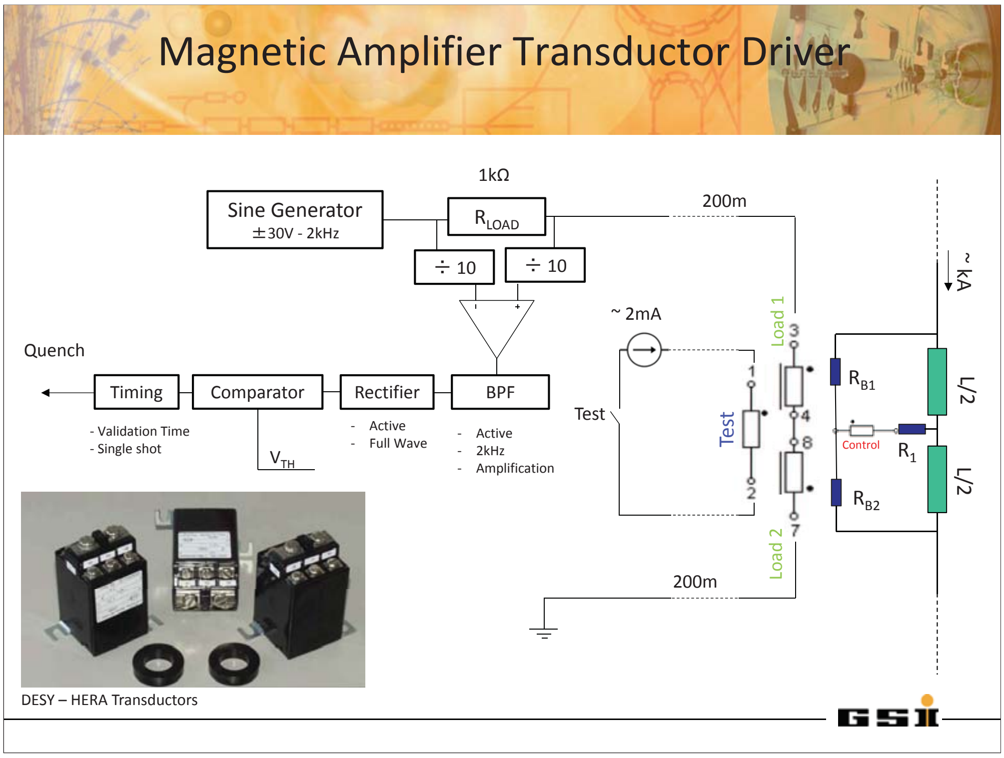
Based on DESY – HERA Quench Detection Concept

$R_{B1} = R_{B2}$

$R_1 \sim 100\Omega$

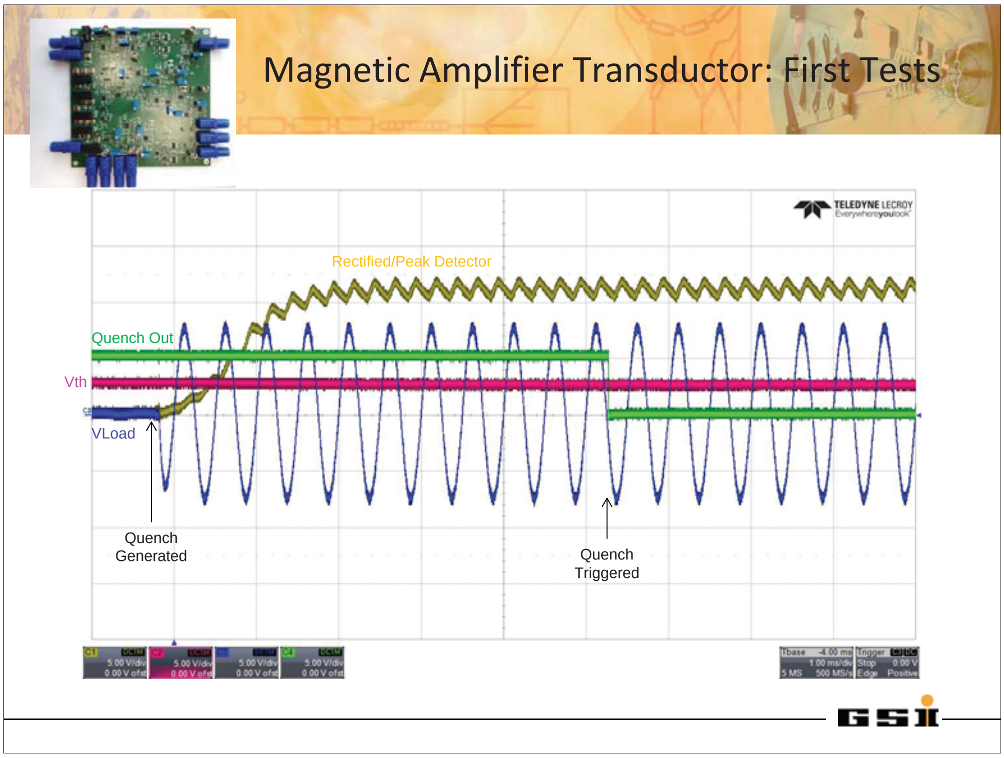
W. Freisleben

P. Szwangruber

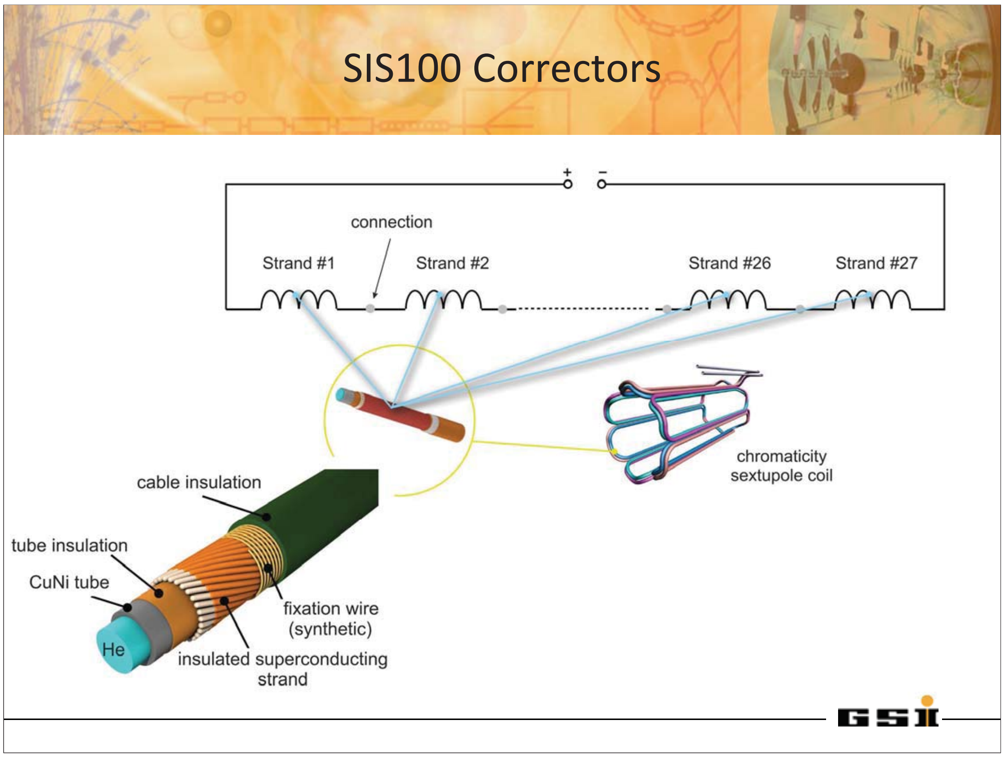


Magnetic Amplifier Transductor Driver

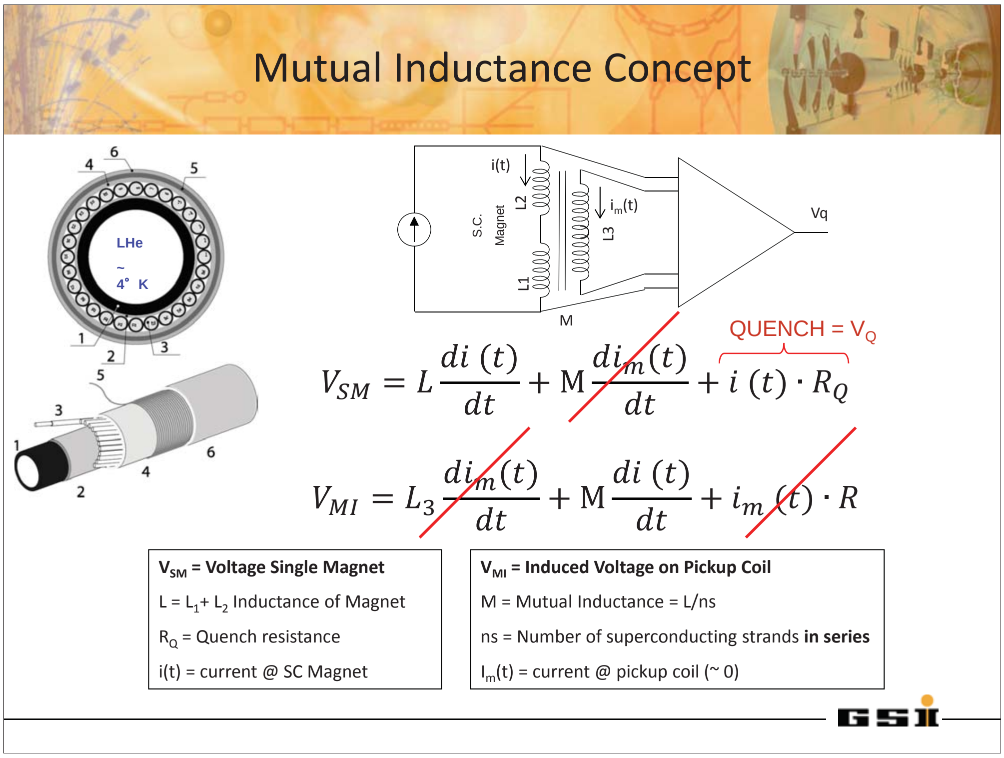
DESY – HERA Transductors



Magnetic Amplifier Transductor: First Tests



SIS100 Correctors



Mutual Inductance Concept

$$V_{SM} = L\frac{di\,(t)}{dt} + \cancel{M\frac{di_m(t)}{dt}} + \overbrace{i\,(t)\cdot R_Q}^{\text{QUENCH} = V_Q}$$

$$V_{MI} = \cancel{L_3\frac{di_m(t)}{dt}} + M\frac{di\,(t)}{dt} + \cancel{i_m\,(t)\cdot R}$$

V_{SM} = Voltage Single Magnet

L = L_1+ L_2 Inductance of Magnet

R_Q = Quench resistance

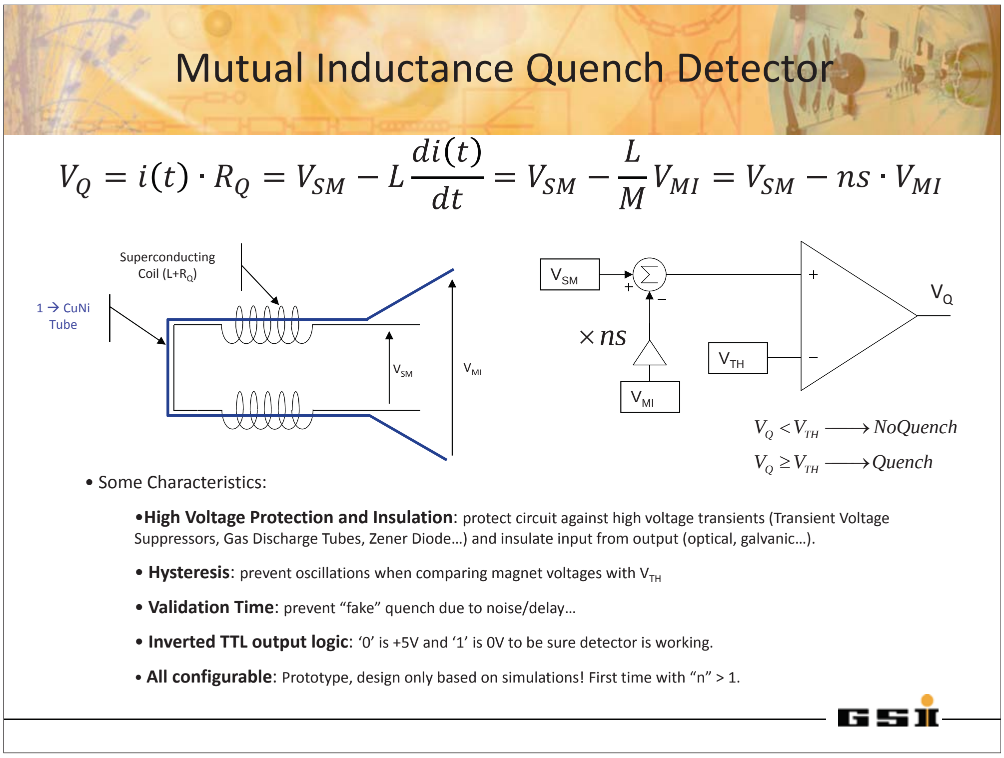
i(t) = current @ SC Magnet

V_{MI} = Induced Voltage on Pickup Coil

M = Mutual Inductance = L/ns

ns = Number of superconducting strands **in series**

I_m(t) = current @ pickup coil (~ 0)



Mutual Inductance Quench Detector

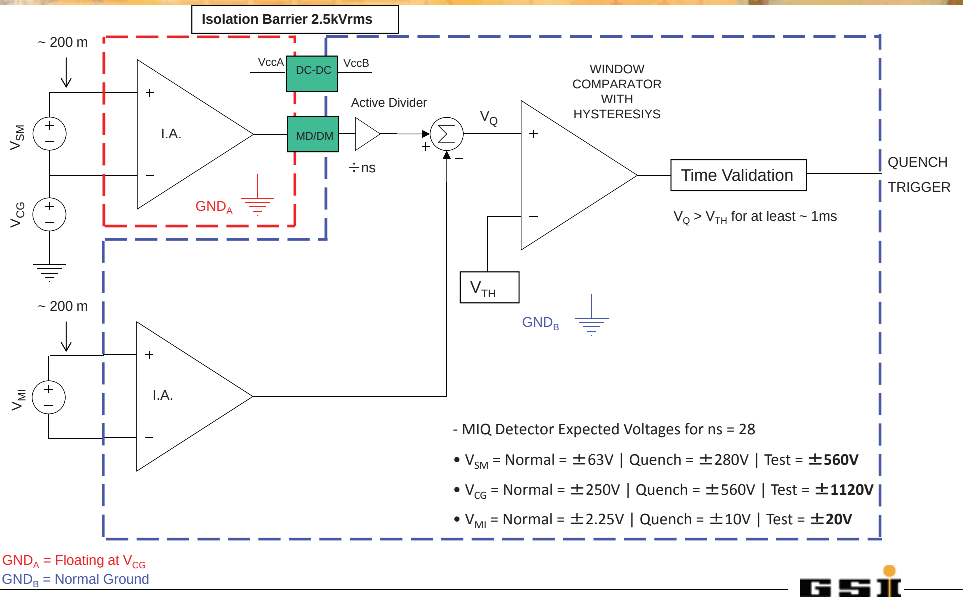
$$V_Q = i(t)\cdot R_Q = V_{SM} - L\frac{di(t)}{dt} = V_{SM} - \frac{L}{M}V_{MI} = V_{SM} - ns\cdot V_{MI}$$

$$V_Q < V_{TH} \longrightarrow NoQuench$$

$$V_Q \geq V_{TH} \longrightarrow Quench$$

- Some Characteristics:
  - **High Voltage Protection and Insulation**: protect circuit against high voltage transients (Transient Voltage Suppressors, Gas Discharge Tubes, Zener Diode…) and insulate input from output (optical, galvanic…).
  - **Hysteresis**: prevent oscillations when comparing magnet voltages with V_{TH}
  - **Validation Time**: prevent “fake” quench due to noise/delay…
  - **Inverted TTL output logic**: ‘0’ is +5V and ‘1’ is 0V to be sure detector is working.
  - **All configurable**: Prototype, design only based on simulations! First time with “n” > 1.

Designed MIQ Detector

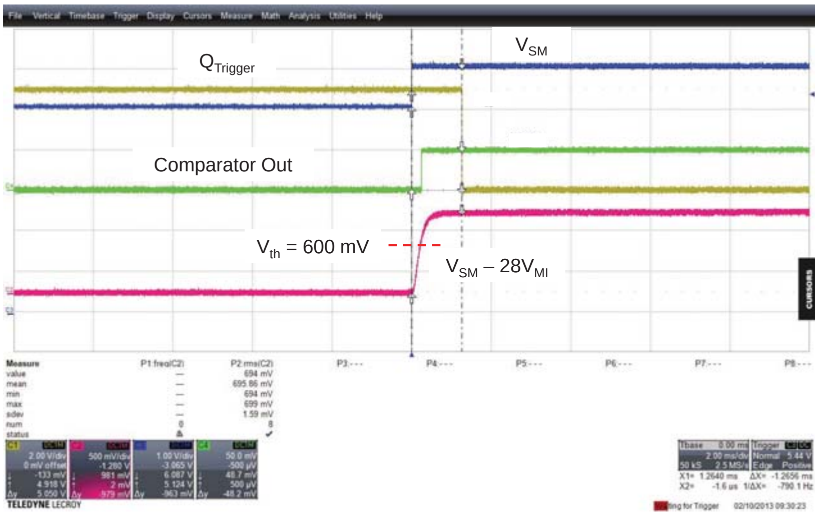


- MIQ Detector Expected Voltages for ns = 28

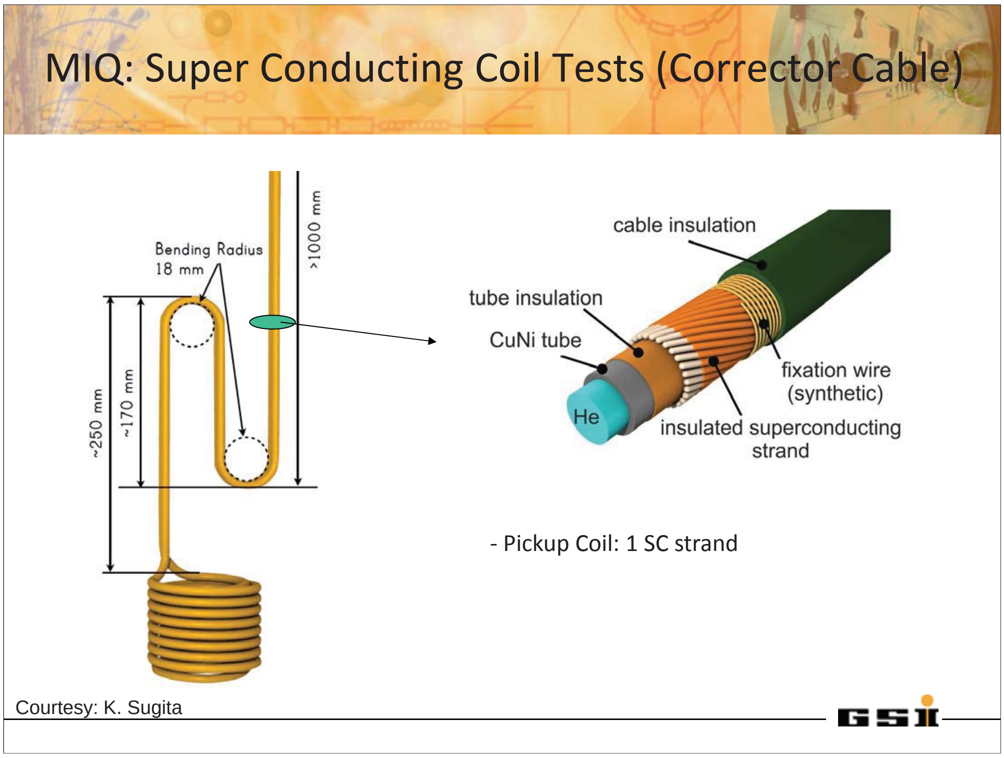
- V_{SM} = Normal = ±63V | Quench = ±280V | Test = **±560V**
- V_{CG} = Normal = ±250V | Quench = ±560V | Test = **±1120V**
- V_{MI} = Normal = ±2.25V | Quench = ±10V | Test = **±20V**

GND_A = Floating at V_{CG}
GND_B = Normal Ground

MIQ: Laboratory Tests



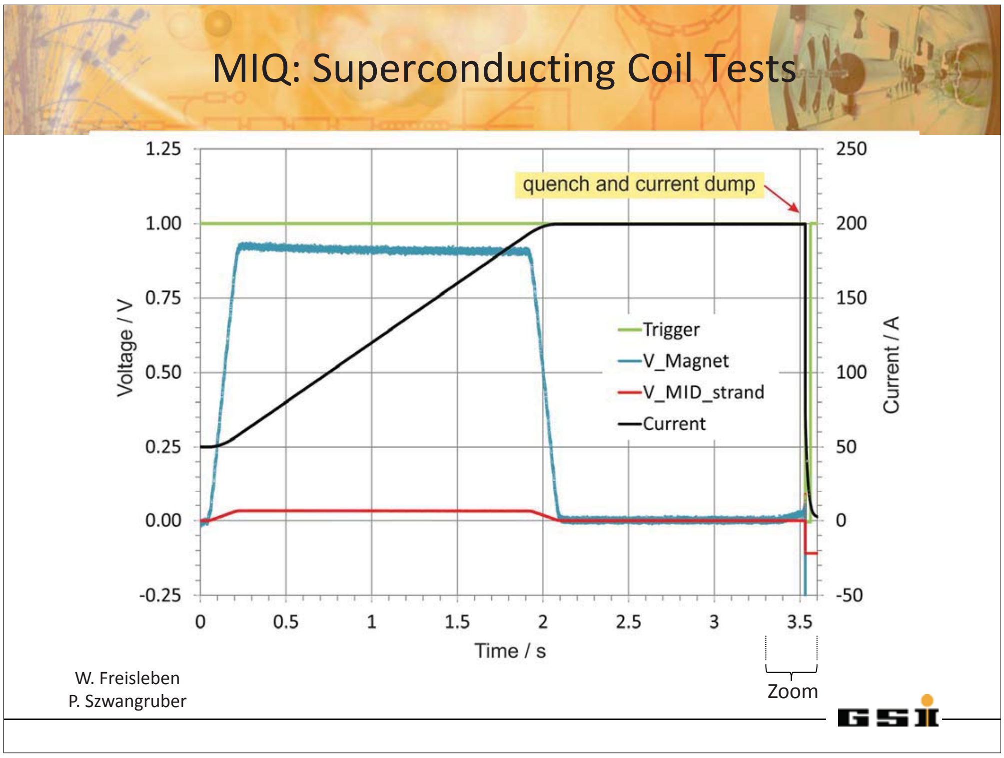
Measure	P1:freq(C2)	P2:rms(C2)	P3:---	P4:---	P5:---	P6:---	P7:---	P8:---
value	—	694 mV						
mean	—	695.86 mV						
min	—	694 mV						
max	—	699 mV						
sdev	—	1.59 mV						
num	0	8						
status	⚠	✓						



MIQ: Super Conducting Coil Tests (Corrector Cable)

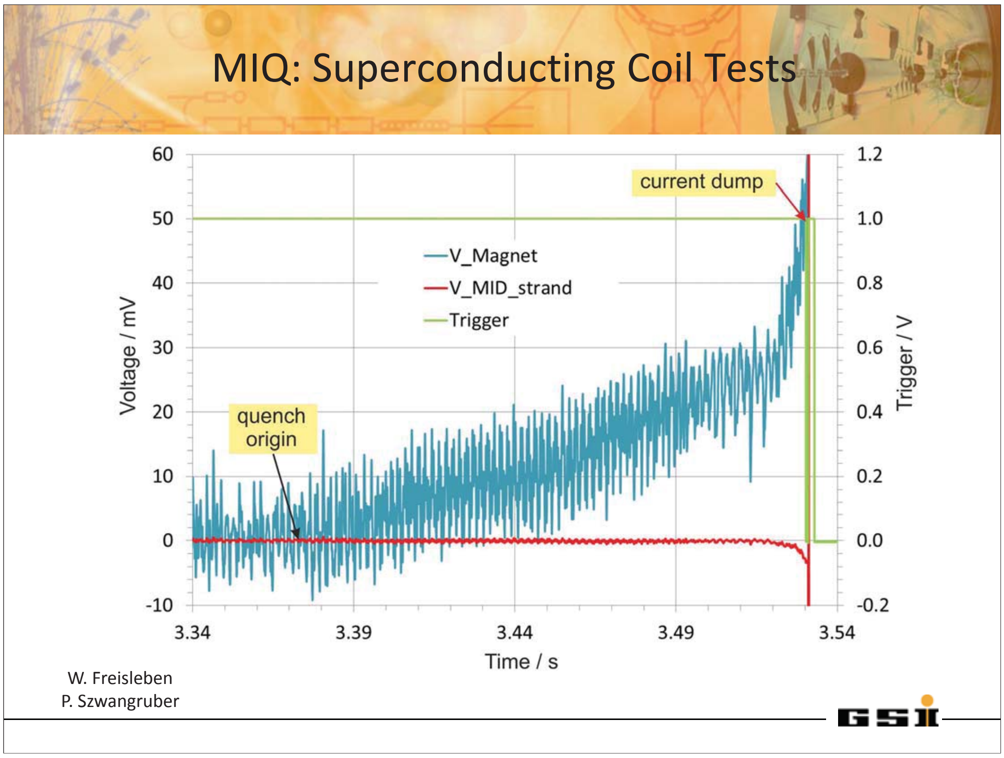
- Pickup Coil: 1 SC strand

Courtesy: K. Sugita



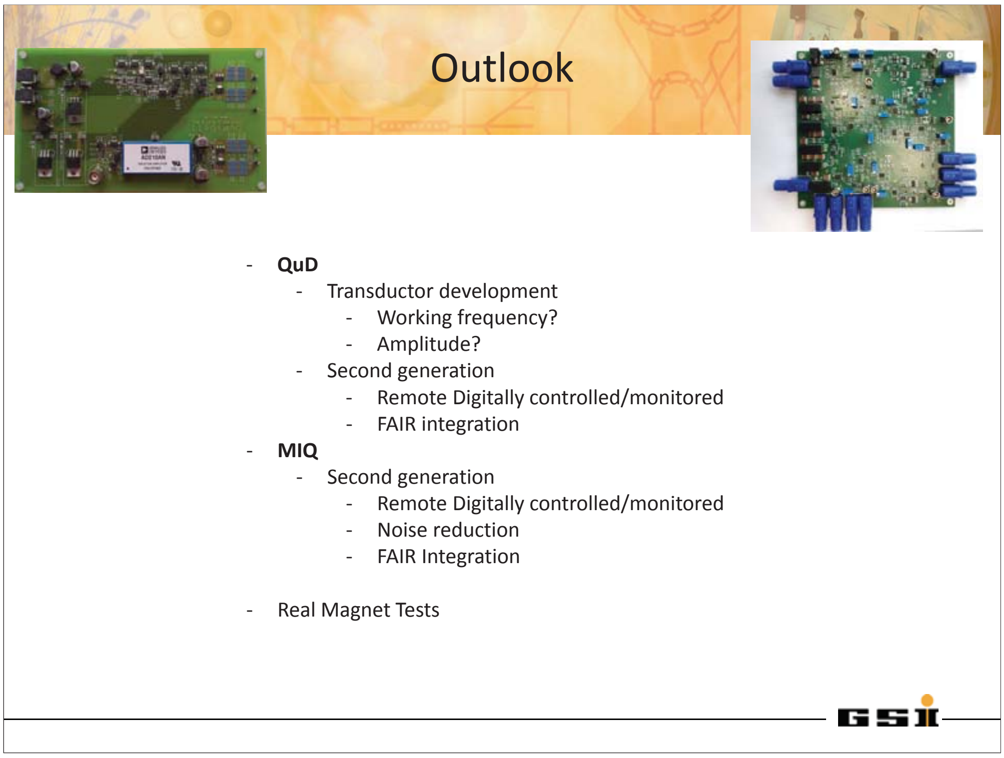
MIQ: Superconducting Coil Tests

W. Freisleben
P. Szwangruber



MIQ: Superconducting Coil Tests

W. Freisleben
P. Szwangruber

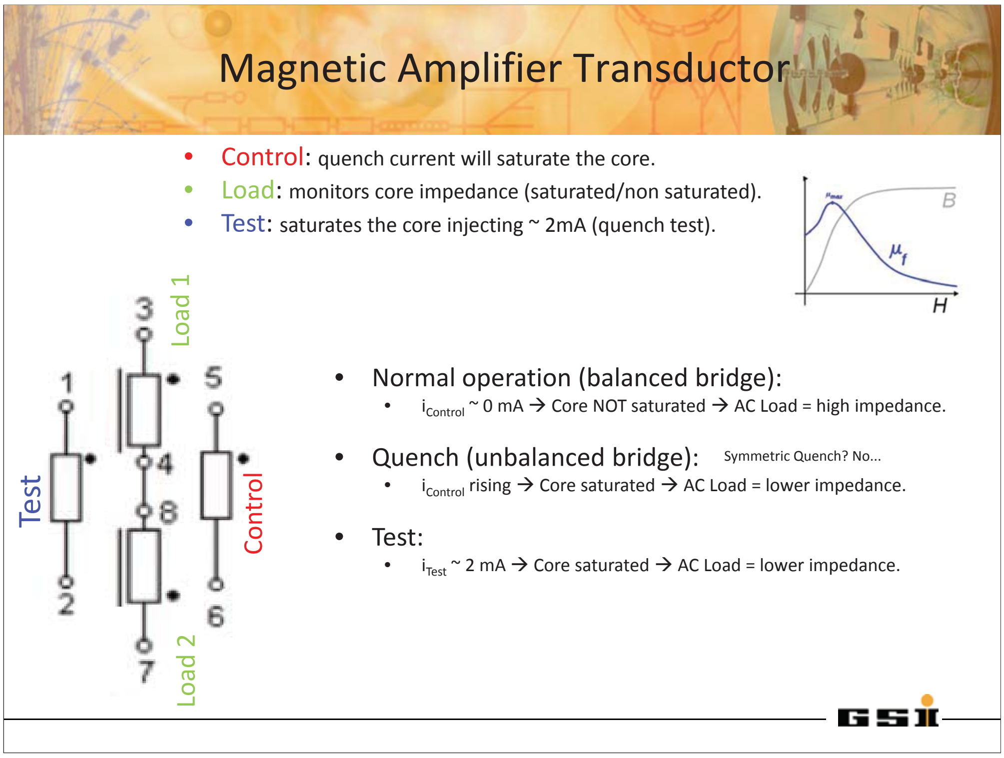


Outlook

- **QuD**
  - Transductor development
    - Working frequency?
    - Amplitude?
  - Second generation
    - Remote Digitally controlled/monitored
    - FAIR integration
- **MIQ**
  - Second generation
    - Remote Digitally controlled/monitored
    - Noise reduction
    - FAIR Integration

- Real Magnet Tests

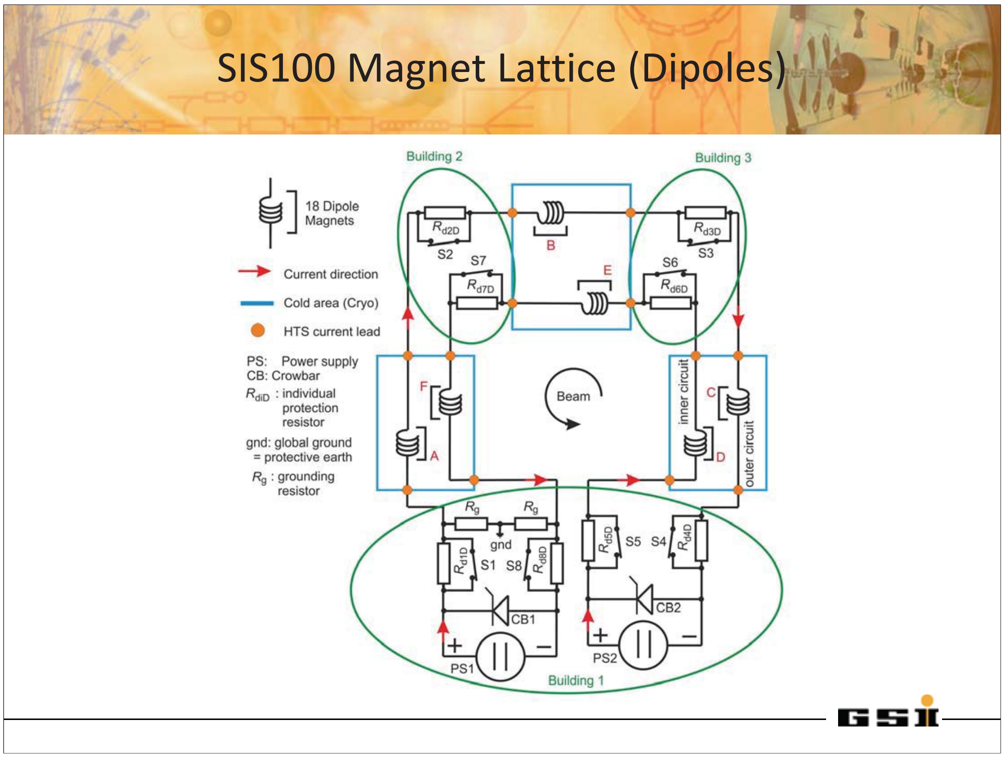
Thank you!



Magnetic Amplifier Transductor

- Control: quench current will saturate the core.
- Load: monitors core impedance (saturated/non saturated).
- Test: saturates the core injecting ~ 2mA (quench test).

- Normal operation (balanced bridge):
  - $i_{Control}$ ~ 0 mA → Core NOT saturated → AC Load = high impedance.
- Quench (unbalanced bridge): Symmetric Quench? No...
  - $i_{Control}$ rising → Core saturated → AC Load = lower impedance.
- Test:
  - i_{Test} ~ 2 mA → Core saturated → AC Load = lower impedance.



SIS100 Magnet Lattice (Dipoles)

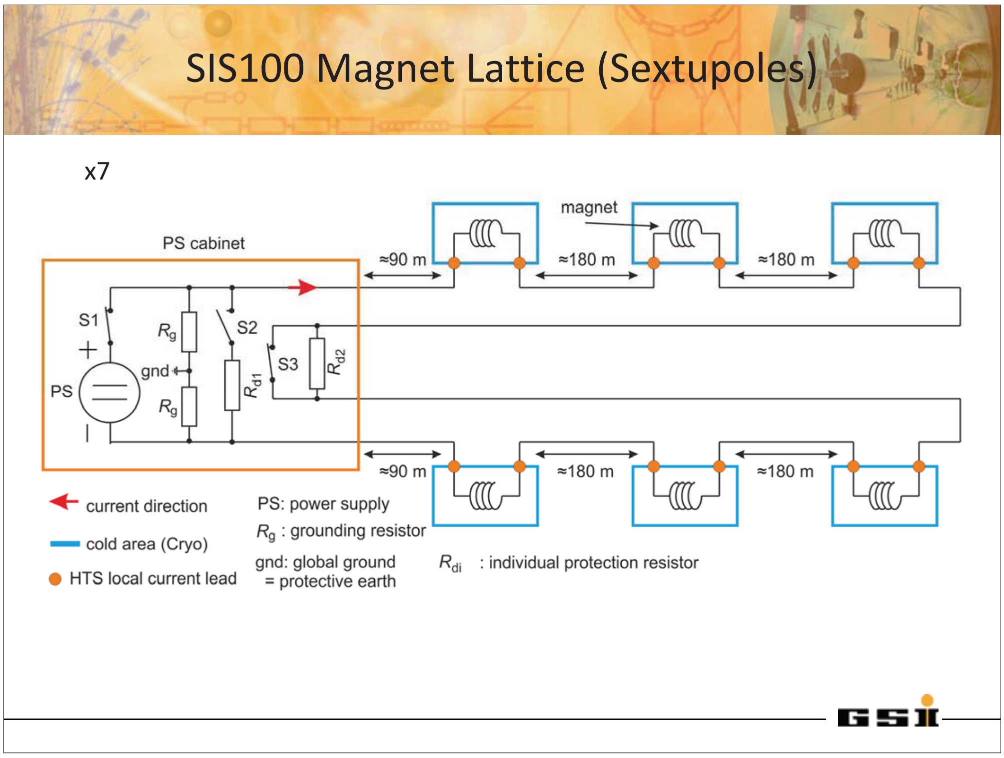
18 Dipole Magnets

Current direction

Cold area (Cryo)

HTS current lead

PS: Power supply
CB: Crowbar
R_{diD} : individual protection resistor
gnd: global ground = protective earth
R_g : grounding resistor



SIS100 Magnet Lattice (Sextupoles)

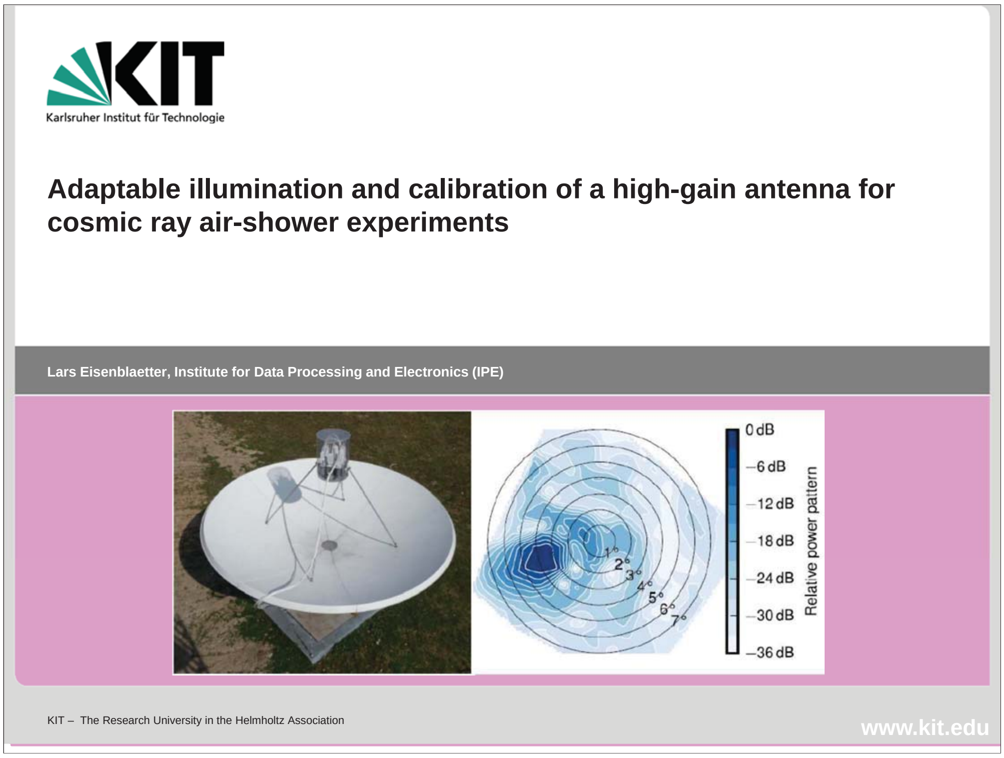
x7

current direction

cold area (Cryo)

HTS local current lead

PS: power supply
R_g : grounding resistor
gnd: global ground
= protective earth
R_{di} : individual protection resistor



Karlsruher Institut für Technologie

Adaptable illumination and calibration of a high-gain antenna for cosmic ray air-shower experiments

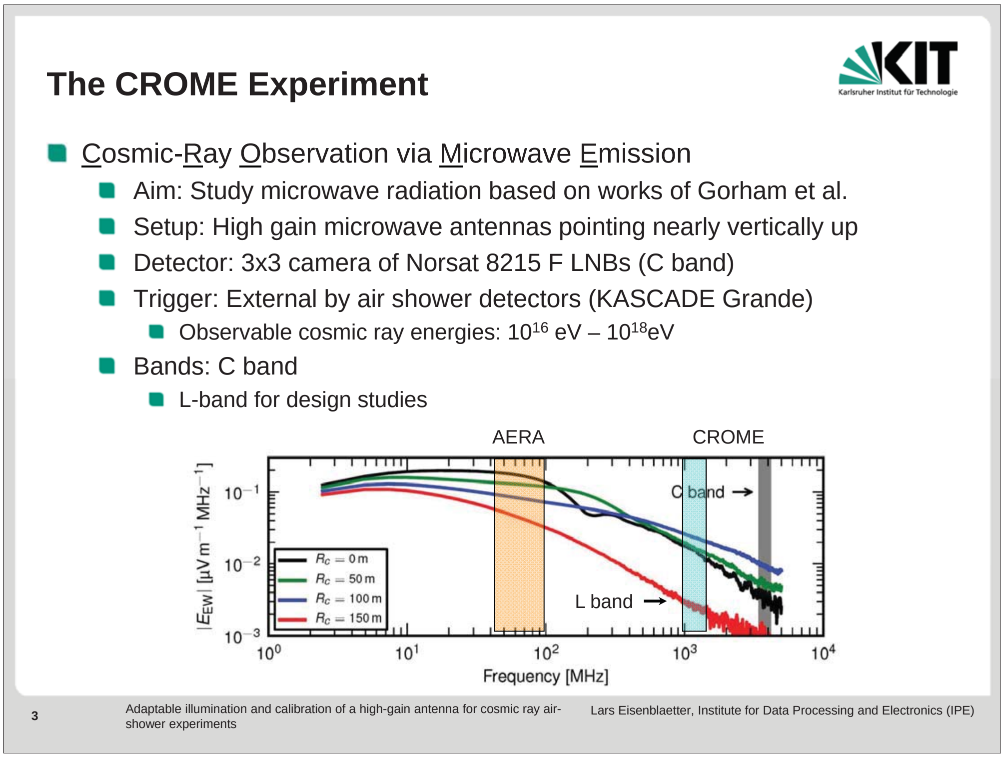
Lars Eisenblaetter, Institute for Data Processing and Electronics (IPE)

KIT – The Research University in the Helmholtz Association

www.kit.edu

Outline

- The CROME Experiment
- Circular Waveguide Feedhorn
  - L band setup
  - Kumar-Feed
    - Simulation
    - Measurements
- Calibration process
  - Calibration transmitter
  - Process and results
    - Radiation pattern
    - Uncertainties
- Conclusion

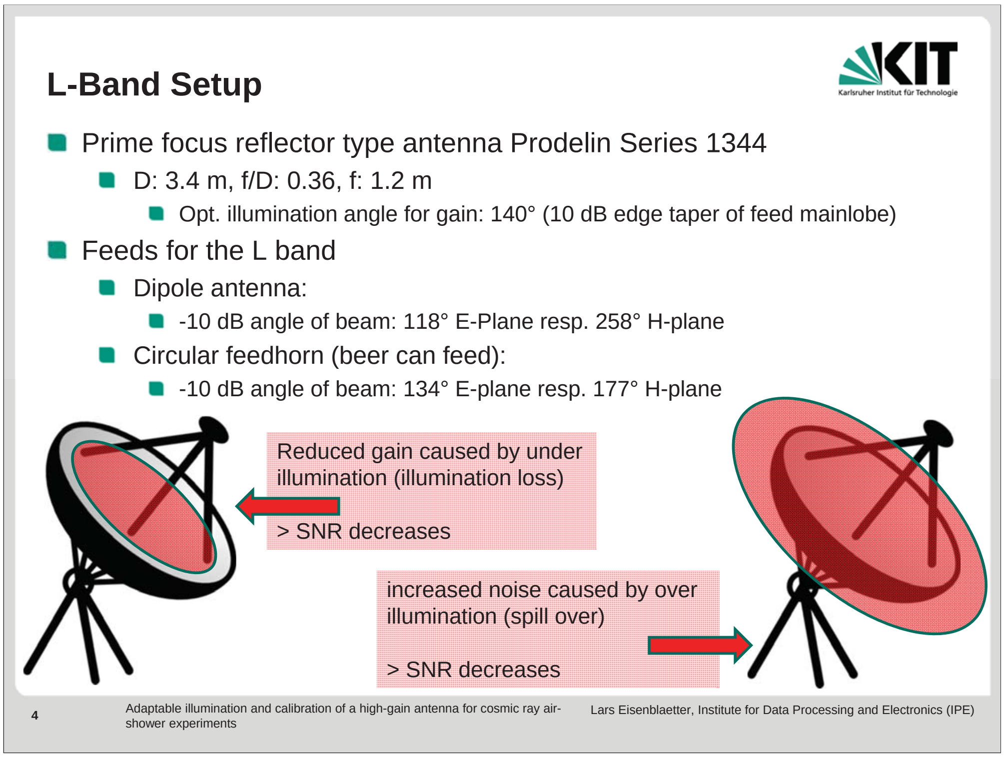


The CROME Experiment

- Cosmic-Ray Observation via Microwave Emission
  - Aim: Study microwave radiation based on works of Gorham et al.
  - Setup: High gain microwave antennas pointing nearly vertically up
  - Detector: 3x3 camera of Norsat 8215 F LNBs (C band)
  - Trigger: External by air shower detectors (KASCADE Grande)
    - Observable cosmic ray energies: 10^{16} eV – 10^{18}eV
  - Bands: C band
    - L-band for design studies

3 Adaptable illumination and calibration of a high-gain antenna for cosmic ray air-shower experiments

Lars Eisenblaetter, Institute for Data Processing and Electronics (IPE)



L-Band Setup

- Prime focus reflector type antenna Prodelin Series 1344
  - D: 3.4 m, f/D: 0.36, f: 1.2 m
    - Opt. illumination angle for gain: 140° (10 dB edge taper of feed mainlobe)
- Feeds for the L band
  - Dipole antenna:
    - -10 dB angle of beam: 118° E-Plane resp. 258° H-plane
  - Circular feedhorn (beer can feed):
    - -10 dB angle of beam: 134° E-plane resp. 177° H-plane

Reduced gain caused by under illumination (illumination loss)

> SNR decreases

increased noise caused by over illumination (spill over)

> SNR decreases

4 Adaptable illumination and calibration of a high-gain antenna for cosmic ray air-shower experiments

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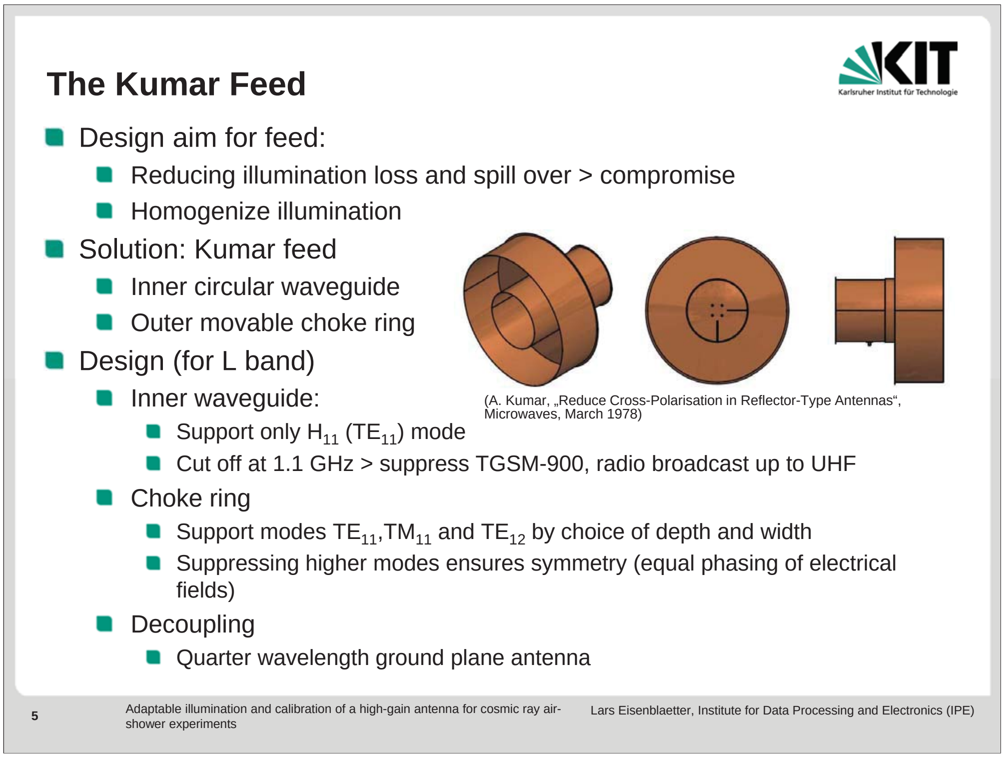
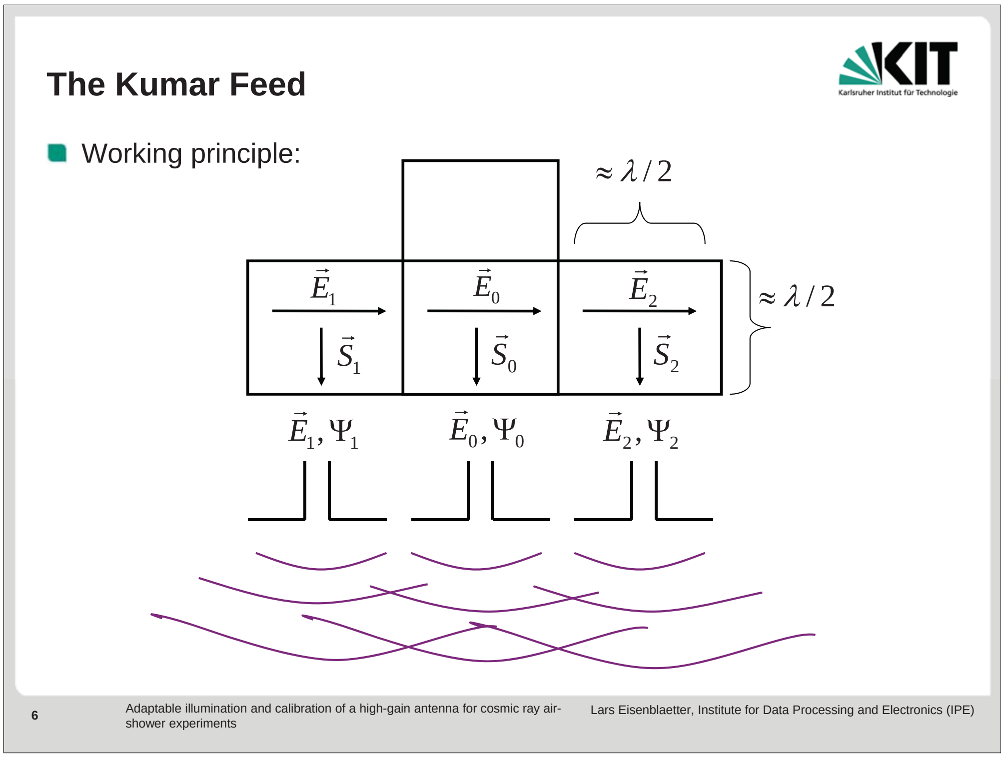


The Kumar Feed

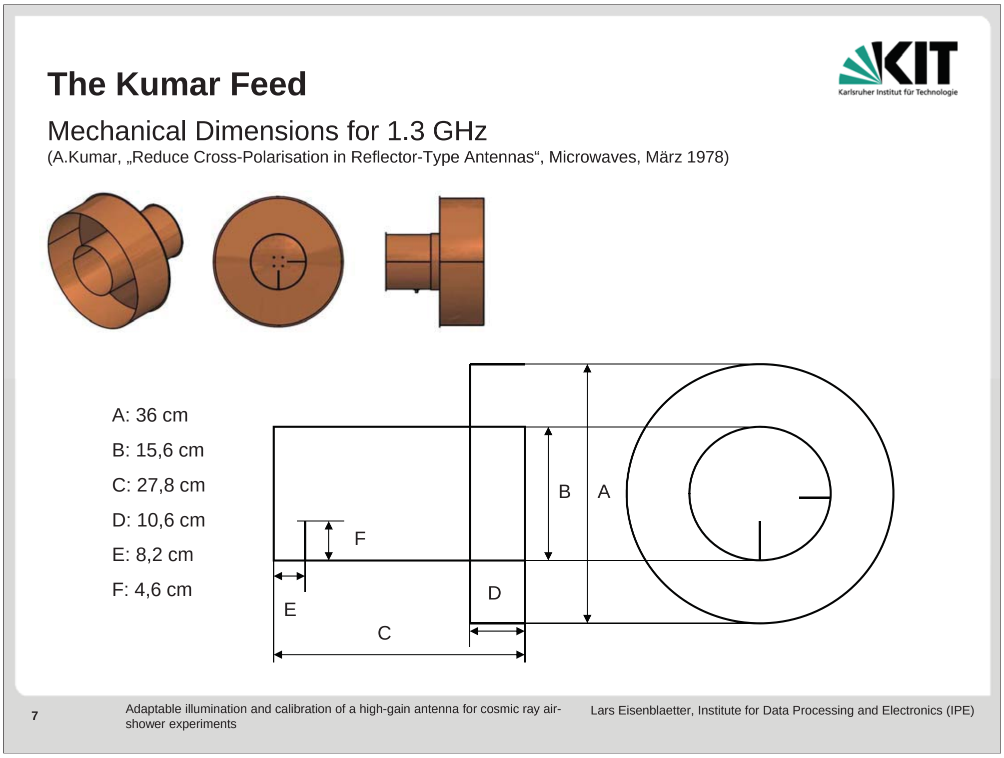
- Design aim for feed:
  - Reducing illumination loss and spill over > compromise
  - Homogenize illumination
- Solution: Kumar feed
  - Inner circular waveguide
  - Outer movable choke ring
- Design (for L band)
  - Inner waveguide:
    - Support only H_{11} (TE_{11}) mode
    - Cut off at 1.1 GHz > suppress TGSM-900, radio broadcast up to UHF
  - Choke ring
    - Support modes TE_{11},TM_{11} and TE_{12} by choice of depth and width
    - Suppressing higher modes ensures symmetry (equal phasing of electrical fields)
  - Decoupling
    - Quarter wavelength ground plane antenna

(A. Kumar, „Reduce Cross-Polarisation in Reflector-Type Antennas“, Microwaves, March 1978)



The Kumar Feed

- Working principle:

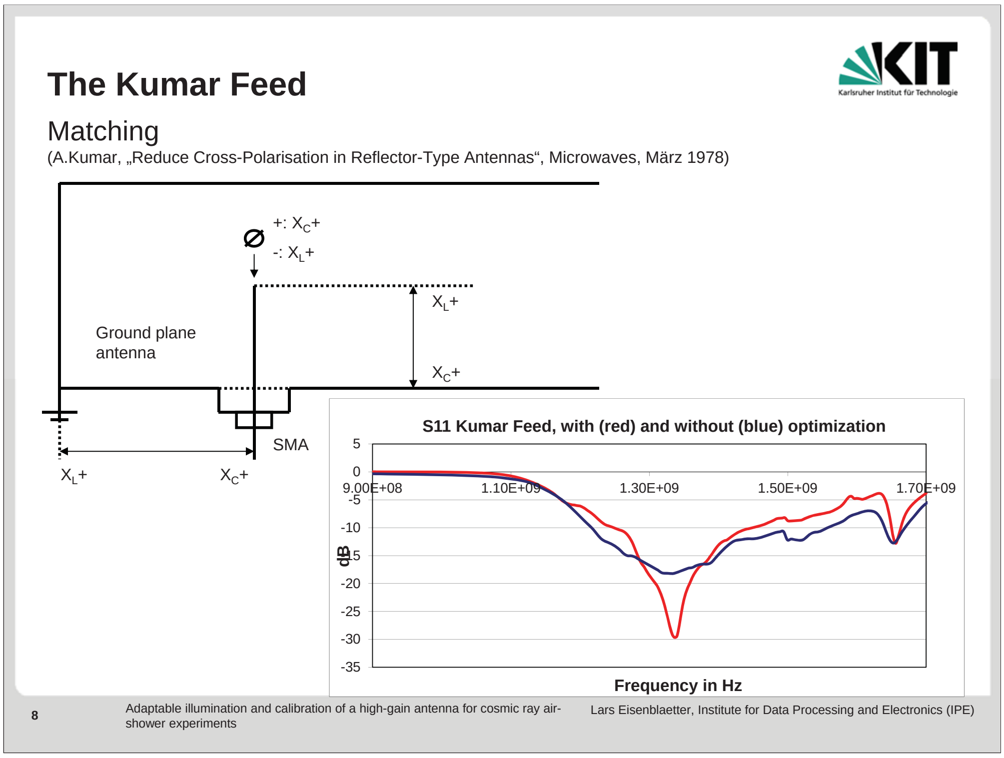


The Kumar Feed

Mechanical Dimensions for 1.3 GHz

(A.Kumar, „Reduce Cross-Polarisation in Reflector-Type Antennas“, Microwaves, März 1978)

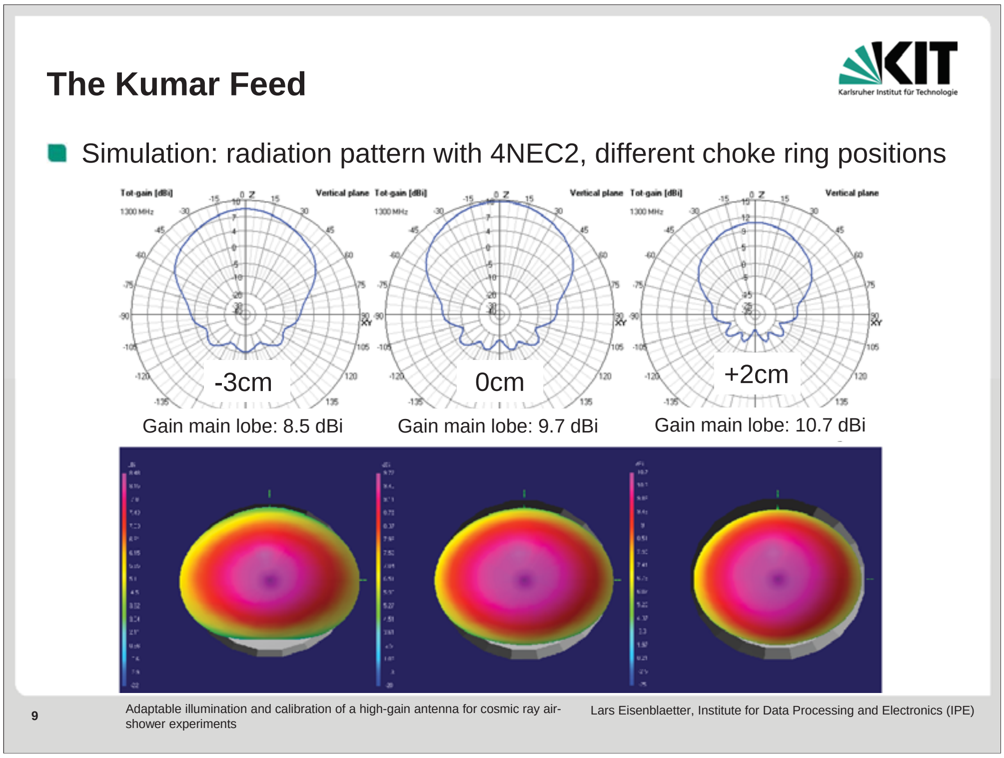
A: 36 cm
B: 15,6 cm
C: 27,8 cm
D: 10,6 cm
E: 8,2 cm
F: 4,6 cm



The Kumar Feed

Matching

(A.Kumar, „Reduce Cross-Polarisation in Reflector-Type Antennas“, Microwaves, März 1978)



The Kumar Feed

- Simulation: radiation pattern with 4NEC2, different choke ring positions

Gain main lobe: 8.5 dBi

Gain main lobe: 9.7 dBi

Gain main lobe: 10.7 dBi

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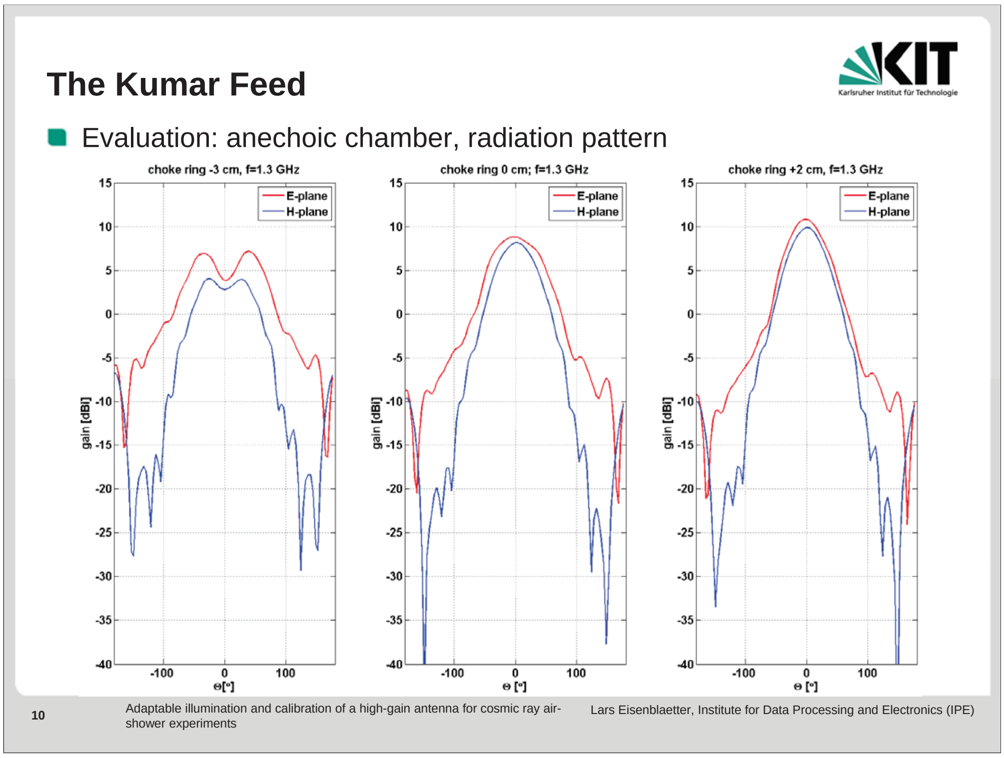
Adaptable illumination and calibration of a high-gain antenna for cosmic ray air-shower experiments

Lars Eisenblaetter, Institute for Data Processing and Electronics (IPE)



The Kumar Feed

- Evaluation: anechoic chamber, radiation pattern

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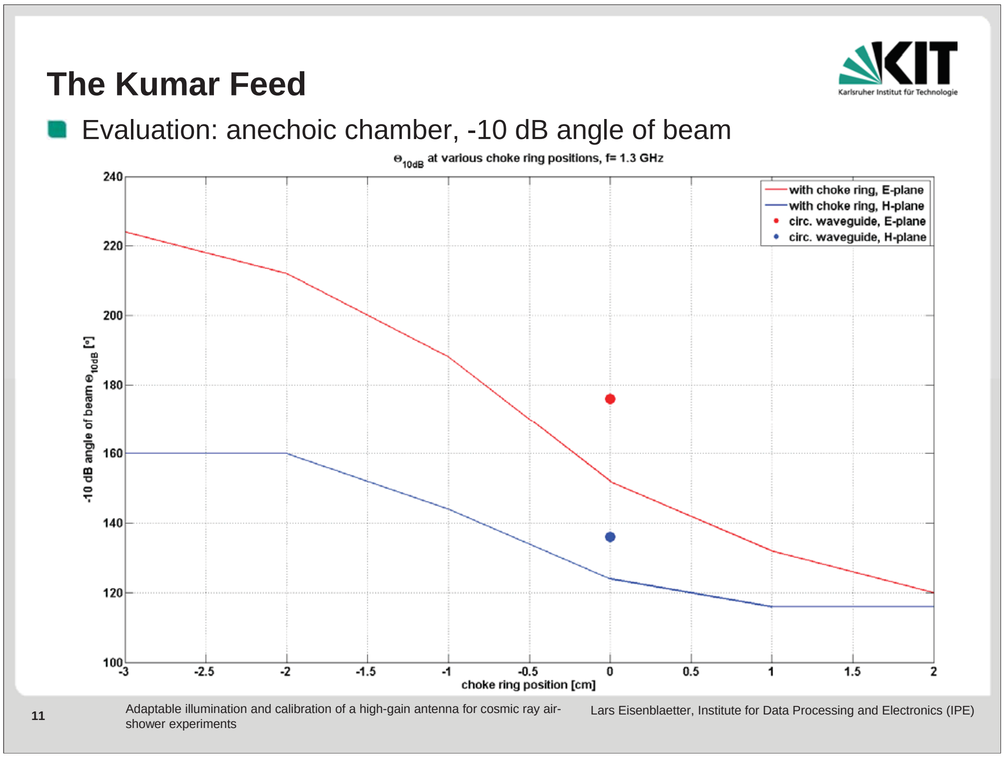
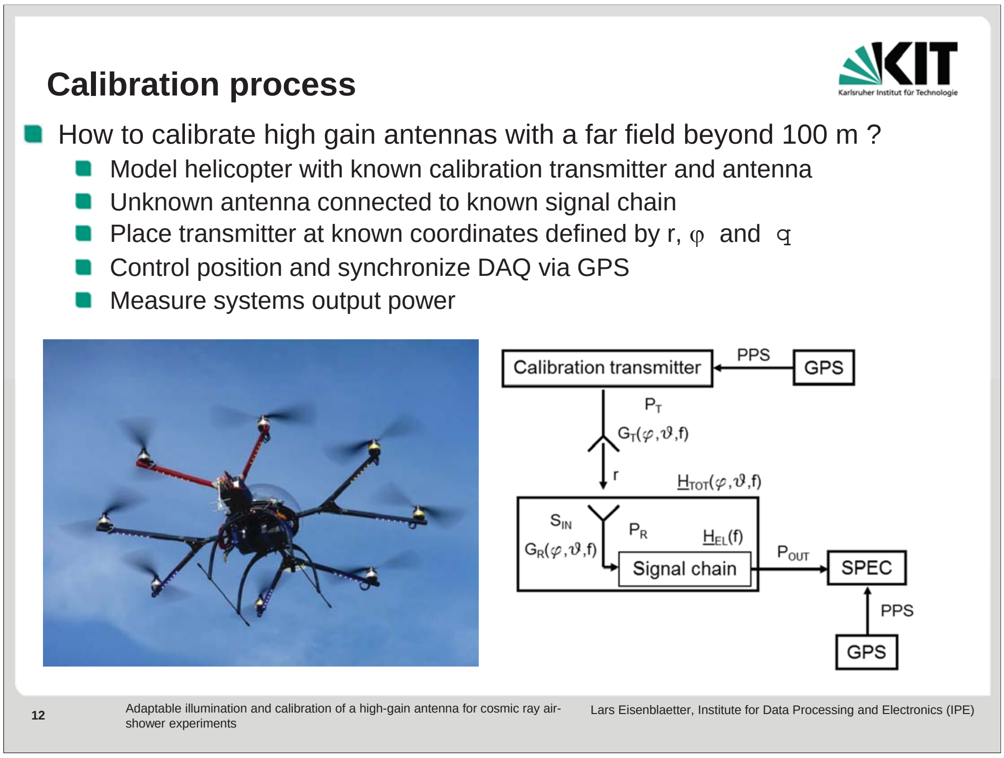


The Kumar Feed

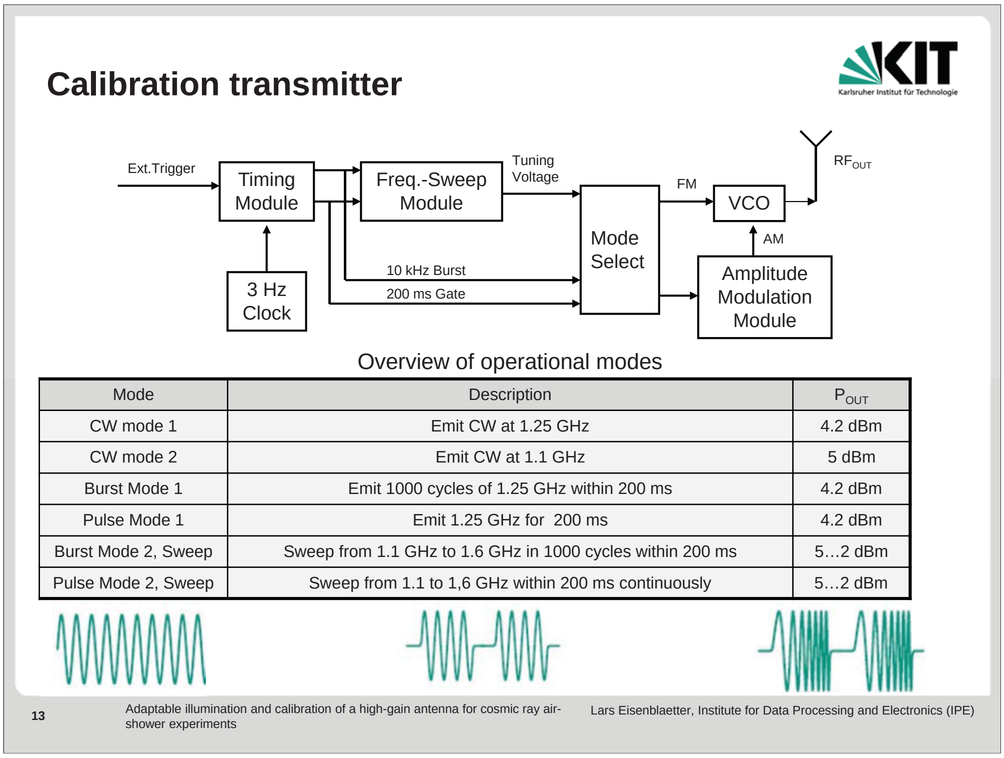
- Evaluation: anechoic chamber, -10 dB angle of beam



Calibration process

- How to calibrate high gain antennas with a far field beyond 100 m ?
  - Model helicopter with known calibration transmitter and antenna
  - Unknown antenna connected to known signal chain
  - Place transmitter at known coordinates defined by r, φ and q
  - Control position and synchronize DAQ via GPS
  - Measure systems output power

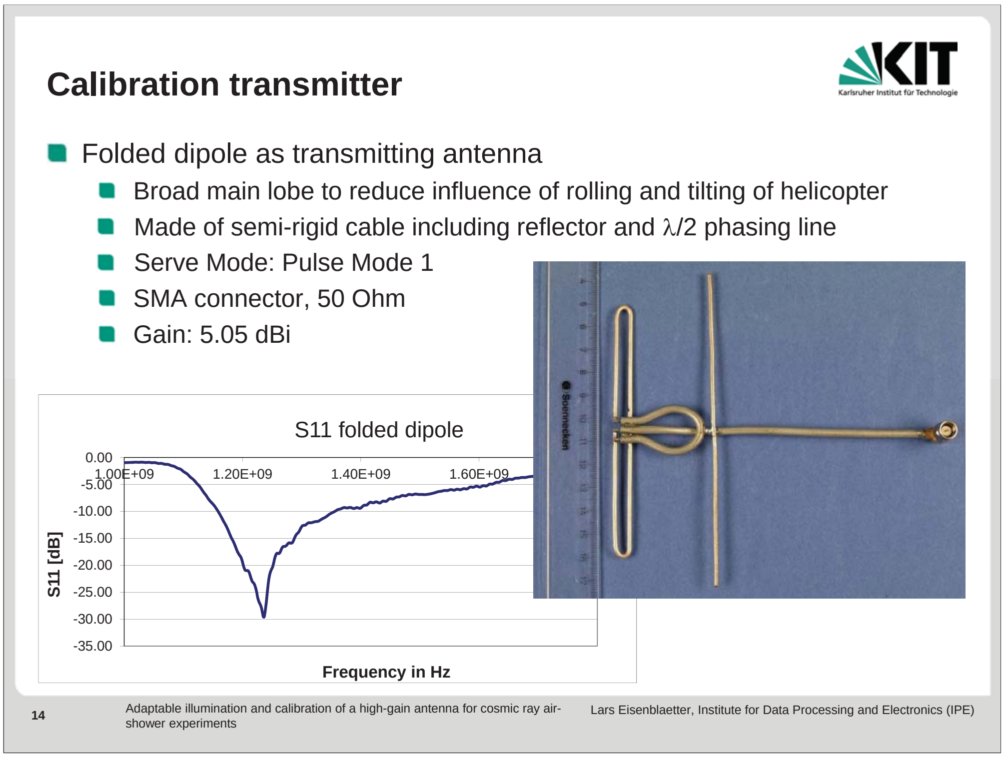
Calibration transmitter
PPS
GPS
P_T
$G_T(\varphi,\vartheta,f)$
r
$\underline{H}_{TOT}(\varphi,\vartheta,f)$
S_{IN}
$G_R(\varphi,\vartheta,f)$
P_R
$\underline{H}_{EL}(f)$
Signal chain
P_{OUT}
SPEC
PPS
GPS



Calibration transmitter

Overview of operational modes

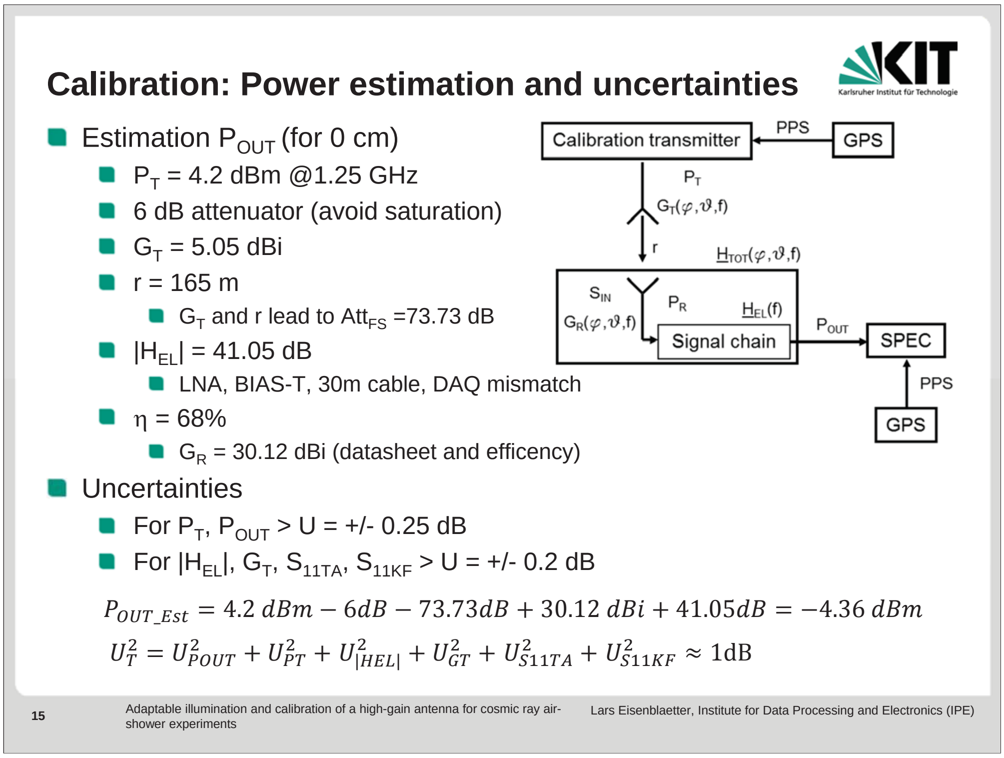
Mode	Description	P_{OUT}
CW mode 1	Emit CW at 1.25 GHz	4.2 dBm
CW mode 2	Emit CW at 1.1 GHz	5 dBm
Burst Mode 1	Emit 1000 cycles of 1.25 GHz within 200 ms	4.2 dBm
Pulse Mode 1	Emit 1.25 GHz for 200 ms	4.2 dBm
Burst Mode 2, Sweep	Sweep from 1.1 GHz to 1.6 GHz in 1000 cycles within 200 ms	5…2 dBm
Pulse Mode 2, Sweep	Sweep from 1.1 to 1,6 GHz within 200 ms continuously	5…2 dBm



Calibration transmitter

- Folded dipole as transmitting antenna
  - Broad main lobe to reduce influence of rolling and tilting of helicopter
  - Made of semi-rigid cable including reflector and λ/2 phasing line
  - Serve Mode: Pulse Mode 1
  - SMA connector, 50 Ohm
  - Gain: 5.05 dBi

S11 folded dipole

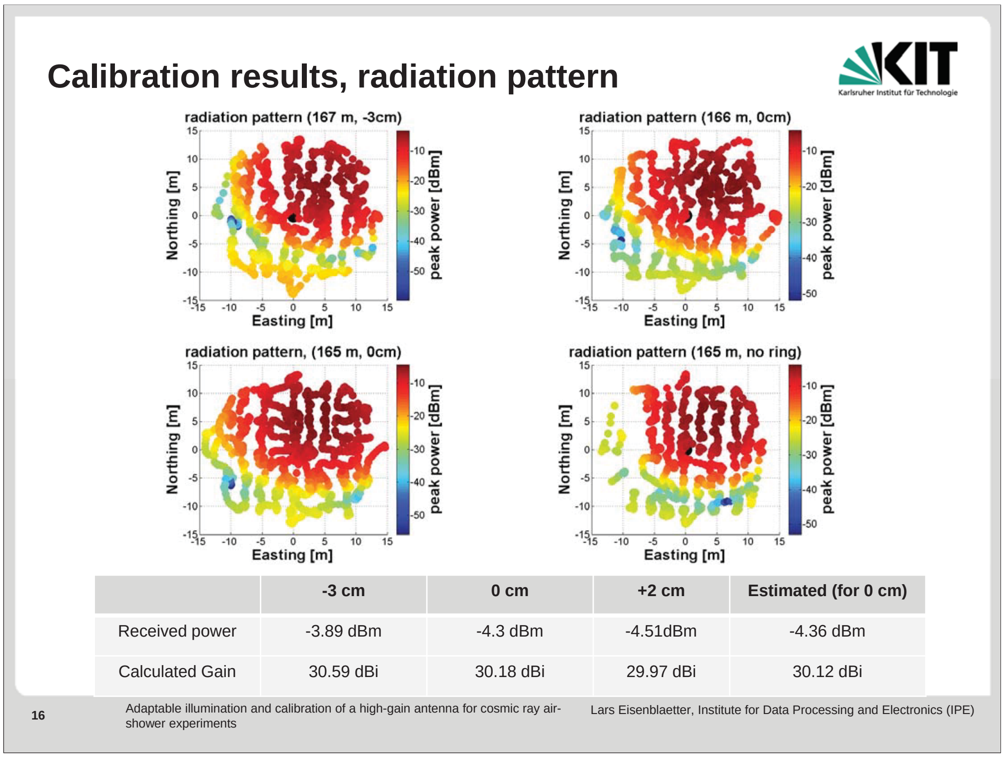


Calibration: Power estimation and uncertainties

- Estimation P_{OUT} (for 0 cm)
  - P_T = 4.2 dBm @1.25 GHz
  - 6 dB attenuator (avoid saturation)
  - G_T = 5.05 dBi
  - r = 165 m
    - G_T and r lead to Att_{FS} =73.73 dB
  - $|H_{EL}|$ = 41.05 dB
    - LNA, BIAS-T, 30m cable, DAQ mismatch
  - η = 68%
    - G_R = 30.12 dBi (datasheet and efficency)
- Uncertainties
  - For P_T, P_{OUT} > U = +/- 0.25 dB
  - For $|H_{EL}|$, G_T, S_{11TA}, S_{11KF} > U = +/- 0.2 dB

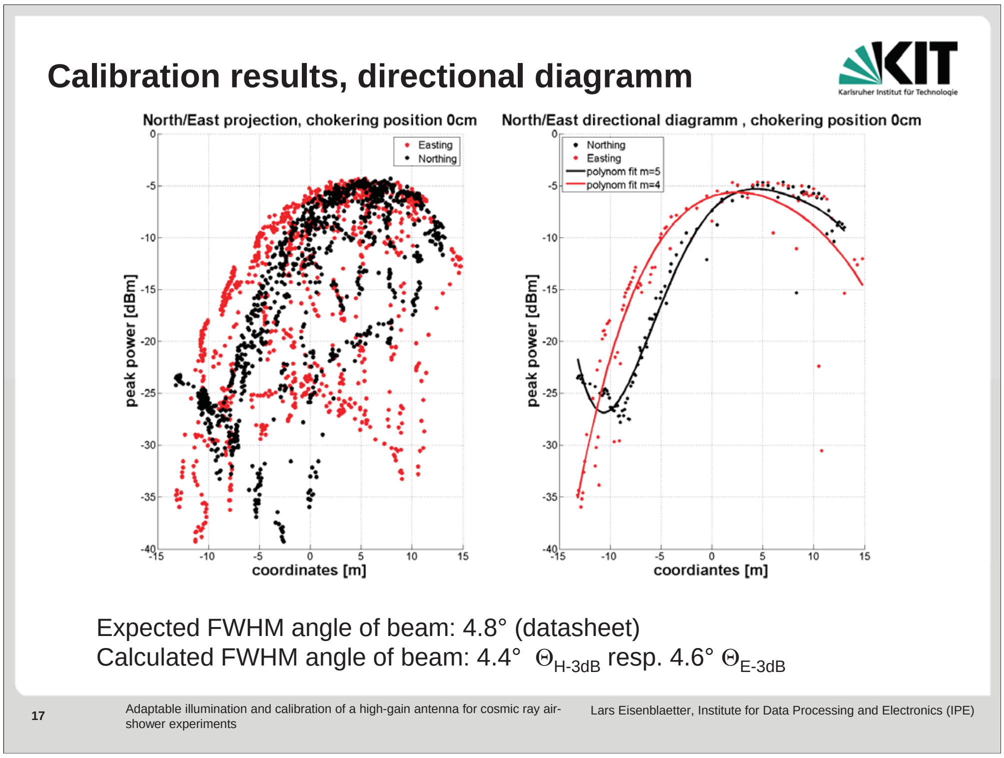
$$P_{OUT\_Est} = 4.2\ dBm - 6dB - 73.73dB + 30.12\ dBi + 41.05dB = -4.36\ dBm$$

$$U_T^2 = U_{POUT}^2 + U_{PT}^2 + U_{|HEL|}^2 + U_{GT}^2 + U_{S11TA}^2 + U_{S11KF}^2 \approx 1\mathrm{dB}$$



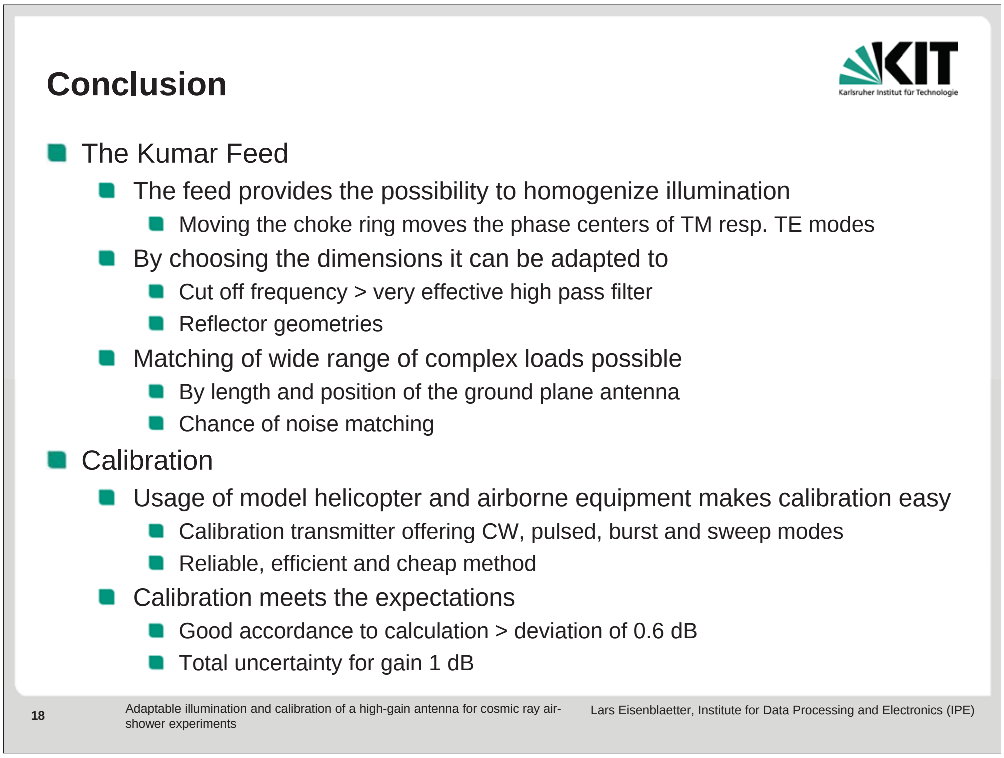
Calibration results, radiation pattern

	-3 cm	0 cm	+2 cm	Estimated (for 0 cm)
Received power	-3.89 dBm	-4.3 dBm	-4.51dBm	-4.36 dBm
Calculated Gain	30.59 dBi	30.18 dBi	29.97 dBi	30.12 dBi



Calibration results, directional diagramm

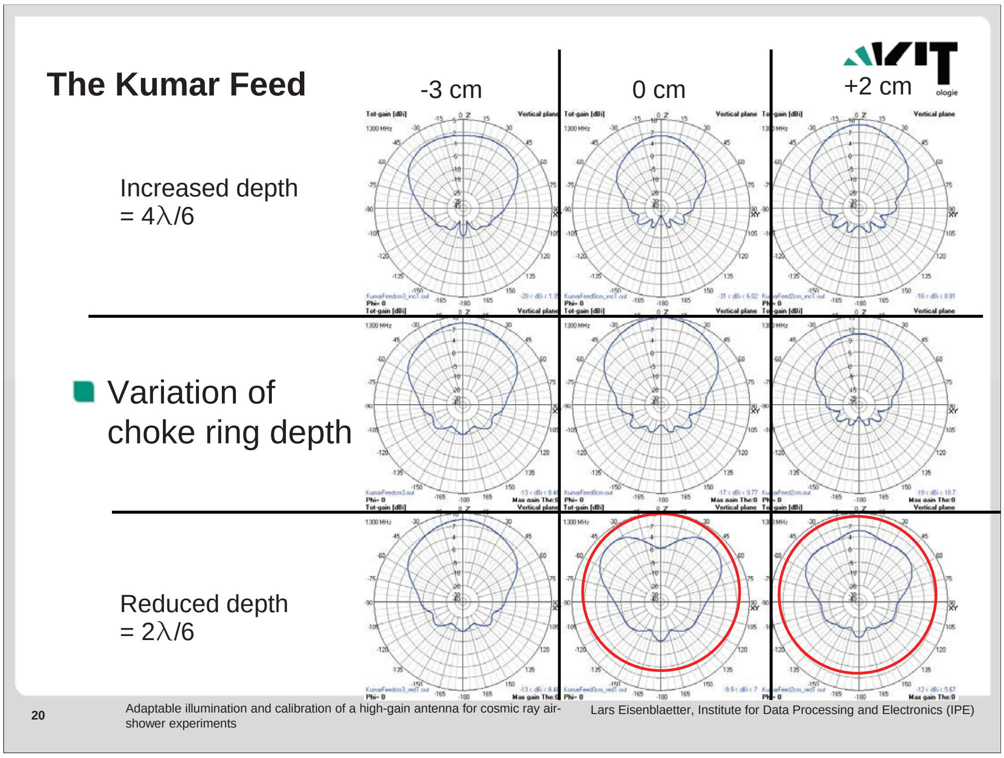
Expected FWHM angle of beam: 4.8° (datasheet)
Calculated FWHM angle of beam: 4.4° $\Theta_{H\text{-}3dB}$ resp. 4.6° $\Theta_{E\text{-}3dB}$



Conclusion

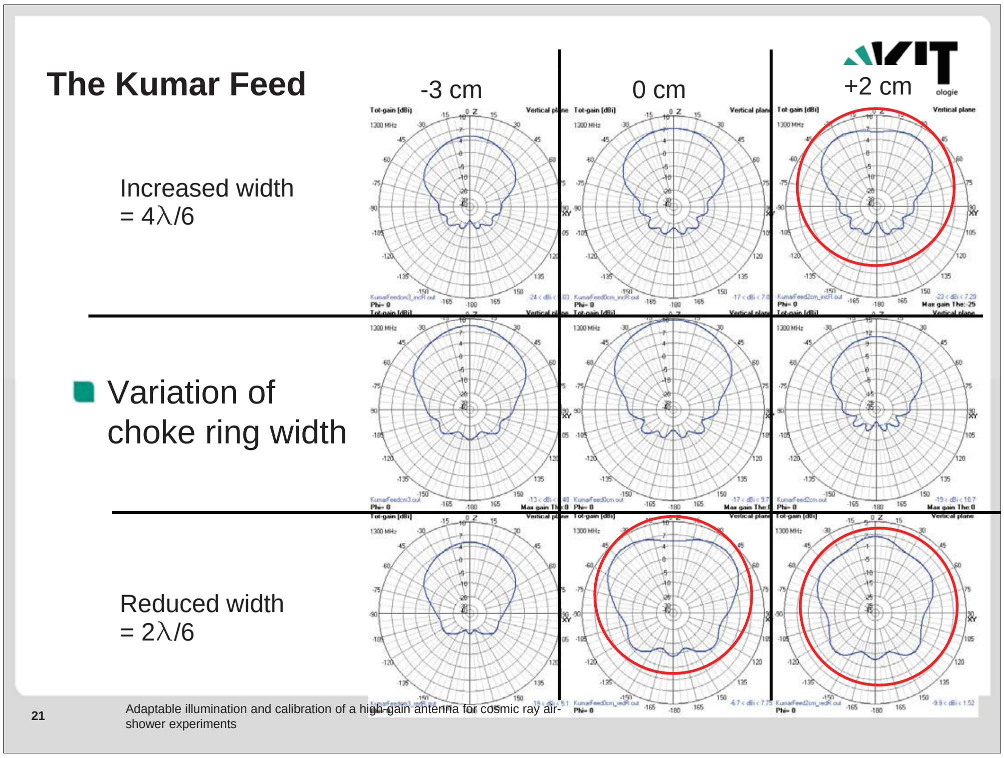
- The Kumar Feed
  - The feed provides the possibility to homogenize illumination
    - Moving the choke ring moves the phase centers of TM resp. TE modes
  - By choosing the dimensions it can be adapted to
    - Cut off frequency > very effective high pass filter
    - Reflector geometries
  - Matching of wide range of complex loads possible
    - By length and position of the ground plane antenna
    - Chance of noise matching
- Calibration
  - Usage of model helicopter and airborne equipment makes calibration easy
    - Calibration transmitter offering CW, pulsed, burst and sweep modes
    - Reliable, efficient and cheap method
  - Calibration meets the expectations
    - Good accordance to calculation > deviation of 0.6 dB
    - Total uncertainty for gain 1 dB

Thanks for your attention



The Kumar Feed

	-3 cm	0 cm	+2 cm
Increased depth = 4λ/6			
- Variation of choke ring depth			
Reduced depth = 2λ/6			



The Kumar Feed

-3 cm | 0 cm | +2 cm

Increased width
= 4λ/6

- Variation of choke ring width

Reduced width
= 2λ/6

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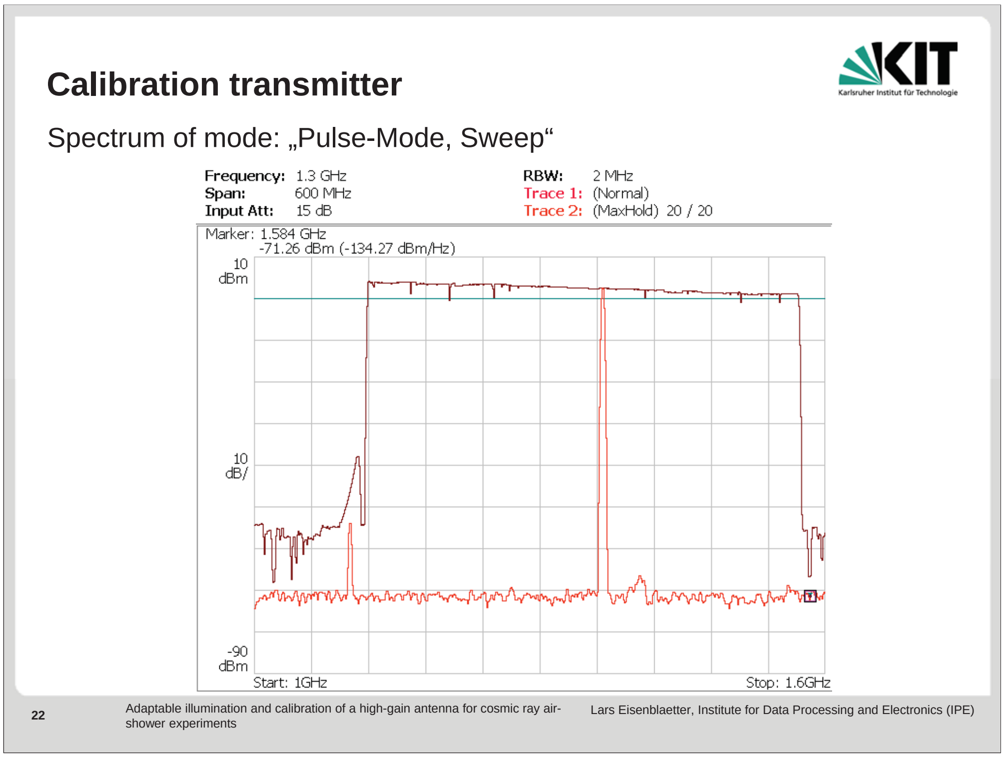
Adaptable illumination and calibration of a high-gain antenna for cosmic ray air-shower experiments



Calibration transmitter

Spectrum of mode: „Pulse-Mode, Sweep“

Frequency: 1.3 GHz
Span: 600 MHz
Input Att: 15 dB
RBW: 2 MHz
Trace 1: (Normal)
Trace 2: (MaxHold) 20 / 20

Marker: 1.584 GHz
-71.26 dBm (-134.27 dBm/Hz)

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Adaptable illumination and calibration of a high-gain antenna for cosmic ray air-shower experiments

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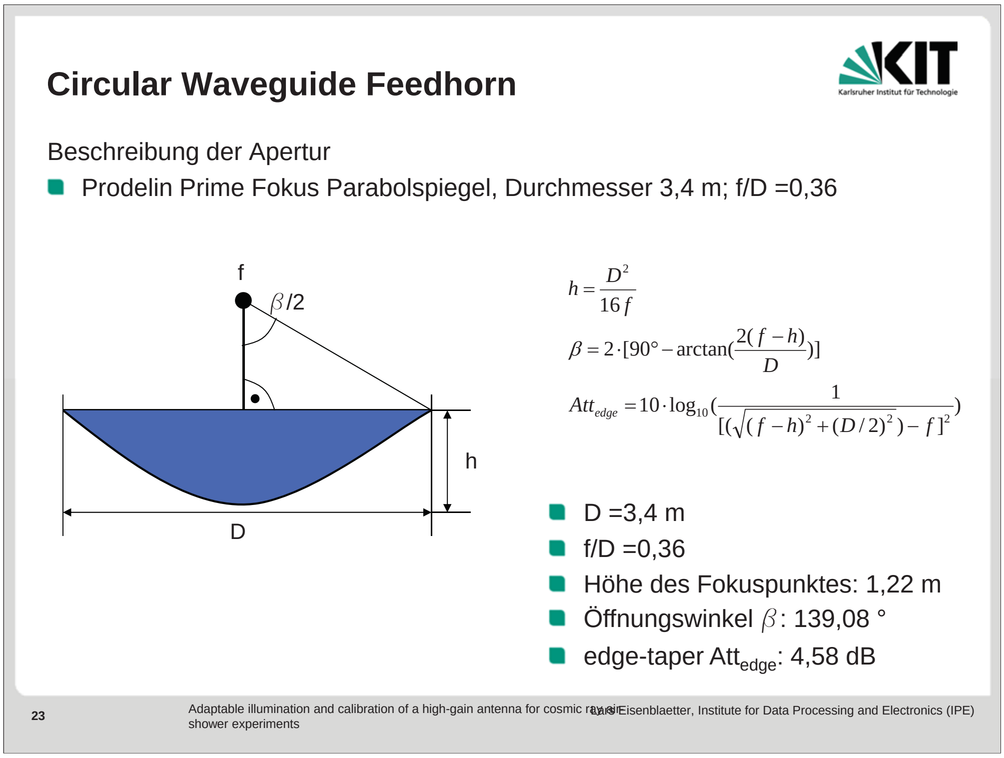


Circular Waveguide Feedhorn

Beschreibung der Apertur

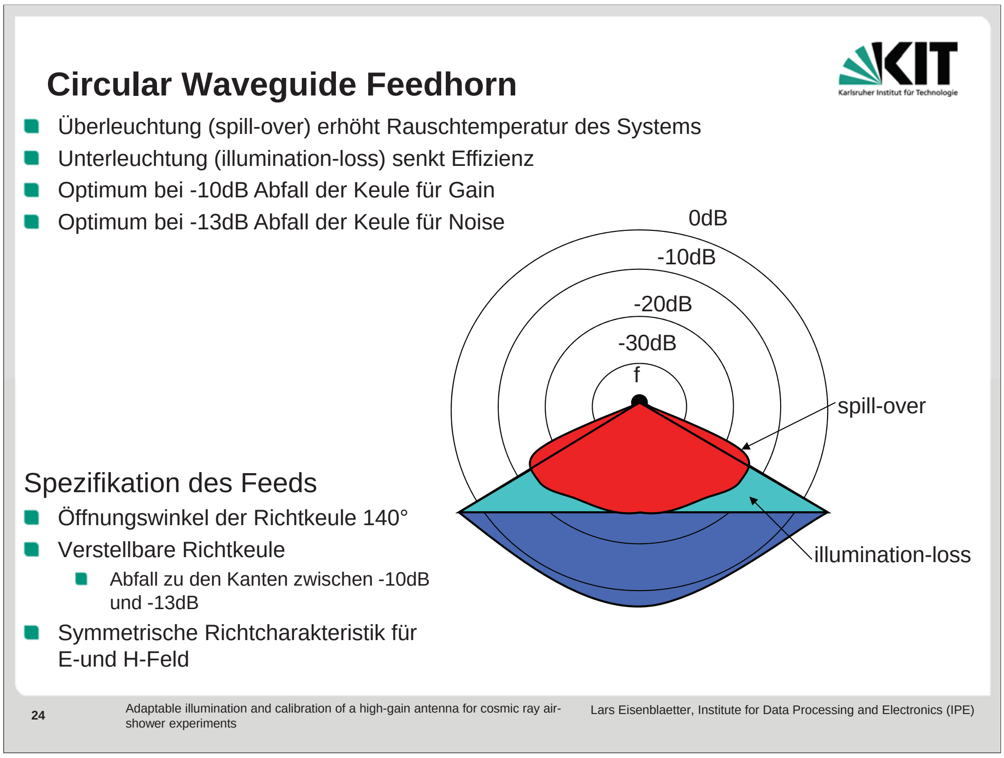
- Prodelin Prime Fokus Parabolspiegel, Durchmesser 3,4 m; f/D =0,36

$$h = \frac{D^2}{16f}$$

$$\beta = 2 \cdot [90° - \arctan(\frac{2(f-h)}{D})]$$

$$Att_{edge} = 10 \cdot \log_{10}(\frac{1}{[(\sqrt{(f-h)^2 + (D/2)^2}) - f]^2})$$

- D =3,4 m
- f/D =0,36
- Höhe des Fokuspunktes: 1,22 m
- Öffnungswinkel β: 139,08 °
- edge-taper Att$_{edge}$: 4,58 dB



Circular Waveguide Feedhorn

- Überleuchtung (spill-over) erhöht Rauschtemperatur des Systems
- Unterleuchtung (illumination-loss) senkt Effizienz
- Optimum bei -10dB Abfall der Keule für Gain
- Optimum bei -13dB Abfall der Keule für Noise

Spezifikation des Feeds

- Öffnungswinkel der Richtkeule 140°
- Verstellbare Richtkeule
  - Abfall zu den Kanten zwischen -10dB und -13dB
- Symmetrische Richtcharakteristik für E-und H-Feld

Kurzzusammenfassung zum SEI Workshop 2016 über Kontrollsysteme

DTS Plattform

Peter Kaever, HZDR

Die seit Februar 2016 begonnenen Aktivitäten um die DTS-Plattform zielen auf eine zentrenübergreifende Zusammenarbeit im Bereich von FPGA's und DAQ-Computing. Technische Basis sind Schnittstellen zur Frontend-Elektronik im FPGA, FPGA-Mikrocontroller samt deren Software, Bussysteme und performante Datenübertragung zum DAQ-Computing (inklusive Linux-Treiber) wie PCIe und Ethernet. Frühes Austauschen und Testen von Modulen soll zu einer hohen Reife der Komponenten führen – dazu arbeiten auch Zentren mit, die nicht in der PoF eingebunden sind. Aufgrund des generischen Ansatzes steht der für das jeweilige Experiment benötigte Komponentenmix im Vordergrund – implementiert auf der vorgesehenen Hardware. Zur Verbesserung der Vergleichbarkeit wurde MTCA.4 als zentrenübergreifend verfügbares Zielsystem für eine Verifikation auf Hardware vorgesehen und dafür die Entwicklung von Board support packages angestrebt.

Profinet Slave Entwicklung

Wolfram Sorge, HZDR

Im Vordergrund dieses Vortrags steht die Einbindung experimentspezifischer Elektronik in Siemens Kontrollsysteme in Form von Profinet Slave Devices. Hierzu wurde die Hardware NIC 50-RE von Hilscher verwendet, die in der Lage ist, auf der Feldbusseite verschiedene Protokolle (Ethernet, Modbus, EtherNet/IP, Ethernet Powerlink, Profinet, Sercos, Varan) zu fahren und die I/O-Peripherie mit SPI oder UART anzubinden. Die entwicklungsseitige Konfiguration erfolgt über einen USB-Anschluss. Zu Testzwecken kann zunächst z.B. mit Modbus die Hardwareintegration getestet und dann auf den Ziel-Feldbus umkonfiguriert werden. Die entsprechende Gerätestammdatei, XML-Datei,… ist für den jeweiligen Feldbus zusätzlich zu erstellen – meist von Hand. Die Physische Schnittstelle ist 10/100 Mb/s Ethernet. Im HZDR wurde mit pymodbus/PyQt (Stack+GUI) vorgetestet und dann die finale Feldbuskopplungsfirmware eingespielt.

Kontrollsysteme im JCNS

Harald Kleines, FZJ

Nach einer Grobpositionierung verschiedener Ansätze (SCADA, DCS) und deren regionaler Verbreitung im Bereich der Beschleunigeranlagen wird die Situation in Jülich vorgestellt, die durch Experimentsysteme geprägt ist. Know-How findet sich dort maßgeblich bei Systemen auf Basis von S7 und GUI's mit WinCC (SCADA) oder Labview bzw. auf der andern Seite in Systemen, die TACO (seit ca. 1990) oder TANGO (objektorientiert, seit ca. 2000) einsetzen. Während S7 das Paradigma verteilter Hardware und des Austausches von Prozessvariablen verfolgt, nutzen TACO&TANGO eine verteilte Client/Server-Architektur mit remote procedure calls und einer Konfigurations- & Parameterdatenbank. Durch das TANGO-interne Threading ergibt sich bei funktionaler Weiterentwicklung zur Konsistenzsicherung (Threading, Events, Startmechanismus, Datacaching) und Verbesserungen bei Logging/Archiv/Alarm/GUI eine erhöhte Komplexität und gegenüber TACO reduzierte Performance (die für slow control ausreicht). Die Projektierungsumgebung weist eine Reihe spezifischer Werkzeuge auf, die im Rahmen des mehrstufigen Entwicklungsvorganges zu nutzen sind. PCS7 wird als umfangreiches und mächtiges System aus dem Hause Siemens vorgestellt, das vor allem prozeßorientiert ist, Projektierung favorisiert und umfangreiche Einarbeitung bzw. Schulung voraussetzt.

EPICS

Peter Zumbruch, GSI

EPICS wird in einer Vielzahl von Beschleunigeranlagen eingesetzt und besitzt eine aktive Kollaboration mit Open Source Zugang. Architektur und Kommunikation (channel access protocol mit hinterlegten Rollen) basieren auf Multi-Client/Multi-Server-Ansätzen, die auch publish / subscriber-Modelle unterstützen. Für die Projektierung sind eine Reihe von Softwaretools verfügbar. Im Zentrum steht der Austausch von Prozeßvariablen mit dazu konsistenten Attributen wie Timestamp, Alarme, Limits, Engineering units,… . Für die Konzipierung eines Systems stehen records als Strukturen zur Verfügung, die in einer Datenbank abgelegt/projektiert werden. Transaktionen zwischen verschiedenen Teilnehmern können Aktivitäten auslösen; diese werden ebenfalls über die Datenbank konfiguriert. Auf der Client-Seite steht das Control System Studio für die Entwicklung von GUI's zur Verfügung. Die Entwicklung wird kontinuierlich fortgeführt, aktuell entsteht EPICS4 mit objektorientierten Ansätzen.

LabVIEW Holger Brand, GSI

Experimentsteuerung mit LabVIEW ist in vielen Zentren fester Bestandteil bei der Instrumentierung kleiner und mittlerer Experimente. Die Funktionalität deckt alle relevanten Bereiche ab: Echtzeitsysteme, FPGA, Data Logging & Supervisory Control (DSC), Vision, Database Connectivity, Control (PID, Fuzzy) & Simulation, Virtual Instruments-Analyzer, Unit-Test, Application-Builder, Debugging (auch für RT), GUI-Werkzeuge (z.B. DIAdem), Testgeneratoren. Die verfügbaren Werkzeuge sind auf industriellem Niveau sehr ausgereift und umfangreich. Mittlerweile werden auch objektorientierte Ansätze stärker unterstützt – beispielsweise durch die Möglichkeit, das Einhalten bestimmter Konstrukte zu erzwingen. Das Befolgen der LabVIEW-spezifischen Paradigmen wie z.B. Datenflussorientierung und Verzicht auf lokale Daten ist die Grundlage für eine erfolgreiche Arbeit.

Zusammengefasst durch Peter Kaever, HZDR

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