HELMHOLTZ
SPITZENFORSCHUNG FÜR
GROSSE HERAUSFORDERUNGEN

Studiengruppe für
Elektronische Instrumentierung
der Helmholtz-Zentren

110. Tagung der Studiengruppe elektronische Instrumentierung im Frühjahr 2019

in Jülich
vom 8. April - 10. April 2019
am

des

Editor: Peter Göttlicher (DESY)
Verlag Deutsches Elektronen-Synchrotron

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110. Tagung der Studiengruppe elektronische Instrumentierung im Frühjahr 2019
8.-10. April 2019, FZJ-ZEA2, Jülich, Deutschland

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110. Tagung der Studiengruppe elektronische Instrumentierung im Frühjahr 2019

SEI - Studiengruppe elektronische Instrumentierung
der Helmholtz-Zentren
HZDR (FZJ - Jülich, ZEA-2), 8. April - 10. April 2019

Inhaltsverzeichnis

Peter Göttlicher
DESY-FEB
10. November 2019

Eröffnung

Elektronik und Firm-/Software wird mit spezialisierten Anforderungen in vielen Forschungsprojekten benötigt. So haben viele Forschungszentren und auch Universitäten Entwicklungsgruppen, die sich diesen Aufgaben stellen. Auch gibt es Industriebetriebe, die spezialisierte Beiträge beisteuern. Mit der Idee, dass man in diesem Umfeld von einander profitieren und zusammenarbeiten kann, treffen sich jedes Jahr einmal Techniker/-innen, Ingenieure/-innen und Wissenschaftler/-innen, um sich mit Vorträgen, einer Ausstellung und Gesprächen auszutauschen. Organisiert wird die Tagung von den Helmholtz-Zentren, offen für andere Vortragende und Teilnehmer/innen. Dieses Jahr war das ZEA-2, Systemhaus für die Forschung, am Forschungszentrum FZJ in Jülich der Gastgeber.

Es waren sechs Helmholtz-Zentren, DESY, FZJ, GSI, HZG, HZDR und KIT, vertreten. Daneben nutzten Universitätsvertreter/innen die Gelegenheit des Austausches. Die Industrie präsentierte auf High-End Anwendungen spezialisierte Geräte und waren für viele Fachgespräche offen.

Die Thematiken der Tagung umfassten:
- Schnelle Datenaufnahme, -verarbeitung und -übertragung
- ASIC's zu Datenübertragung und spezifischer Messsignalaufbereitung.
- Kontrolle von Aktoren und Auslese langsamerer Sensoren
- Fertigung von Elektronik und Geräten mit Elektronik
- Kooperation zu Entwicklungen mit der Industrie
- Wie testet man Elektronik und Firm-/Software?

An einem halben Tag wurde ein Technikbetrieb zur Papierverarbeitung besichtigt. Auch da wurde gezeigt, dass die Steuerung von Maschinen anspruchsvoll ist und teils ähnliche Aspekte wie die Steuerung der Forschungsanlage aufweist.

Das Tagungsprogramm ist auf dem Internet einzusehen:
https://indico.desy.de/indico/event/22503/ oder
https://indico.desy.de//event/SEI_2019
Die Homepage der Studiengruppe ist auf http://sei.desy.de/ zu finden.

Ein Workshop über "Testen" diente dem Austausch, wie man sich zum einen der Vielfalt der spezialisierten Geräte effizient stellt und spezifische Eigenschaften im Test erfasst, und zum anderen doch von Wiederverwendbarkeit und Standards profitiert.

Ausblick

Die nächste Tagung wird für das Frühjahr 2020 am HZG Geestacht geplant.

Teilnehmer der SEI-Tagung 2019. Quelle: FZJ-ZEA-2

Tagungsprogramm

Mon 08/04

12:00

Kleinigkeiten zur Begrüßung

13:00

FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 12:15 - 13:15

Eröffnung *Dr. Peter GOETTLICHER*

FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 13:15 - 13:25

ZEA-2 - System House for Research *Prof. Stefan VAN WAASEN*

14:00

FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 13:25 - 14:25

Das FLASH Forward Kontrollsystem *Mr. Sven KARSTENSEN*

FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 14:25 - 14:45

Instrumentsteuerung am MLZ: Lösungsansatz auf der PLC-Ebene *Dr. Enrico FAULHABER*

15:00

FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 14:50 - 15:10

Kaffeepause - Montag

FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 15:20 - 15:50

Qualitätssicherung im Servicezentrum Elektronik am DESY Hamburg *Dr. Otto-Christian ZEIDES*

16:00

FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 15:50 - 16:10

Simulation durch Auslese - Modellierung von Kernspulen zur Schaltungsberechnung *Dr. Wolfram SORGE*

FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 16:15 - 16:35

Niederfrequente Magnetfelder an Schaltkästen *Mr. Joerg BURMESTER*

FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 16:40 - 17:00

17:00

Averaging: Was hilft's? *Dr. Andree BÜCHNER*

FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 17:05 - 17:25

Tue 09/04

08:00

09:00

Netzteile mit integrierter Intelligenz — *Mr. Christoph VIEF*
FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 08:55 - 09:15

MTCA and MTCA.4 Developments for Large Scale European Accelerators — *Dr. Matthias KIRSCH*
FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 09:20 - 09:40

Foto-Termin
FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 09:45 - 10:00

10:00

Stromver-sorgung - Elektronik fuer Experimente - CAEN – Costruzioni Apparecchiature Elettroniche Nucleari S.p.A

Netzteile für die Automati-sierung und Messtechnik - Kniel System-Electronic GmbH

MTCA und MTCA.4 Baugruppen - Struck Innovative Systeme GmbH

Messgeräte für Elektronik-Baugruppen von Tektronix GmbH und Calplus GmbH

Oszilloskope, MTCA Digitizer und Generatoren, innovative Messtechnik von Teledyne LeCroy / Teledyne SP Devices

Stromver-sorgung für die Forschung - WIENER Power Electronics GmbH

Kaffee - Di

11:00

12:00

13:00

Besichtigung einer Papierfabrik

14:00

15:00

16:00

Wed 10/04

08:00

Temperature drift correction in a rigid-boom electromagnetic induction geophysical instrument — *Mrs. Xihe TAN*

09:00

Development of a simple ion-chamber based dosemeter system — *Dr. Jonny BIRKHAN*
FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 08:55 - 09:15

Development of a Scintillation Neutron Detector Prototype using Digital SiPMs — *Dr. Matthias HERZKAMP*
FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 09:20 - 09:40

MTCA.4 based Wire Scanner System for the European-XFEL — *Mr. Timmy LENSCH*

10:00

FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 09:45 - 10:05

Developments for the CMS Phase-2 Track Finding System — *Mr. Luis ARDILA*
FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 10:10 - 10:30

Kaffeepause-Mi

11:00

FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 10:40 - 11:10

Gigabit Serial Interfaces — *Mr. Georg SCHARDT*
FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 11:10 - 11:30

Anwendung des 10G Base-R Ethernet UDP/IP Systems im Projekt BrainPET — *Mr. Sebastian VÖLKEL*
FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 11:35 - 11:55

12:00

Generic Data Processing board development leveraging a modular approach based on SoM and SoCs — *Mr. Simone FARINA*

The application of heterogeneous FPGA architectures in physics experiments — *Dr. Oliver SANDER*
FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 12:25 - 12:45

Abschluss und Ausblick — *Dr. Peter GOETTLICHER*
FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 12:50 - 13:00

13:00

Mittagspause - Mi
FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2) 13:00 - 14:00

14:00

Arbeitstreffen - DRAFT: Prüfen: Produktion, Prototypen, Programmierung
FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2)

17:00

FLASHForward

FLASHForward Control System

- ÜBERSICHT -

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Was ist FLASHForward ?

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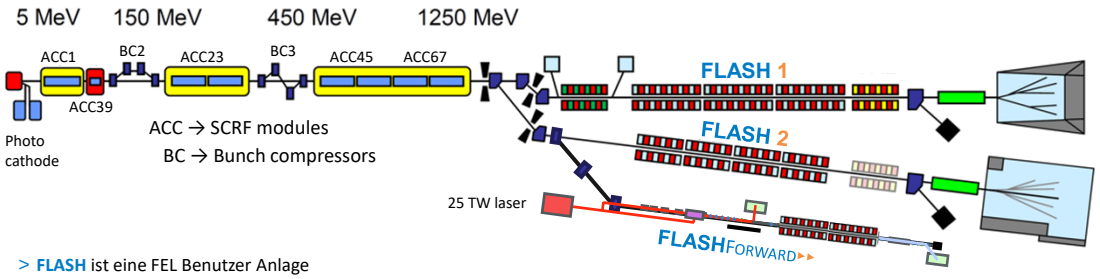
Image Landsat / Copernicus
Image IBCAO
Data SIO, NOAA, U.S. Navy, NGA, GEBCO
Image U.S. Geological Survey
Google E


FLASH Forward
FLASHForward
PWFA research
FLASH
1.25 GeV
→ 315 m
Image Landsat / Copernicus
Google E

FLASHForward ▸▸

FLASHFORWARD▸▸

THE FACILITY FOR HIGH-QUALITY, HIGH-PRECISION, HIGH-AVERAGE-POWER BEAM-DRIVEN PWFA SCIENCE



> **FLASH** ist eine FEL Benutzer Anlage
  - 10% Der Strahlzeit (750 h / year) ist für Beschleuniger-Forschung

> **FLASH**Forward▸▸ ist ein Strahl für PWFA Forschung

> Beide Anlagen teilen sich den Strahl auf Basis der ILC/XFEL Technologie. Typische e-Stahl Parameter sind:
  - ≲ 1.25 GeV Energie mit ein paar 100 pC at ~100 fs rms Bunch Dauer
  - ~2 µm trans. norm. emittance
  - Exzellente Stabilität, timing, und Reproduzierbarkeit durch FEL-Standard feedback Systeme

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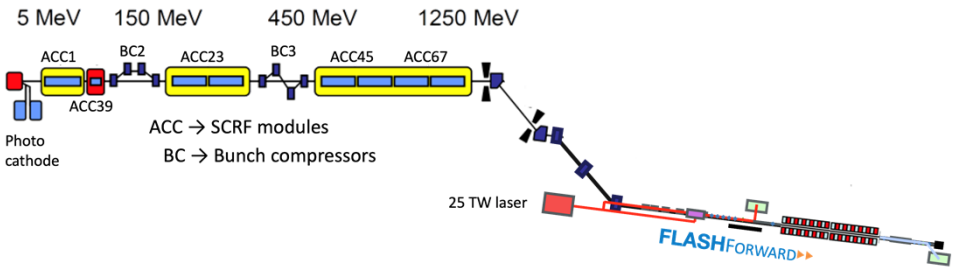
FLASHForward ▸▸

FLASHFORWARD▸▸

THE FACILITY FOR HIGH-QUALITY, HIGH-PRECISION, HIGH-AVERAGE-POWER BEAM-DRIVEN PWFA SCIENCE



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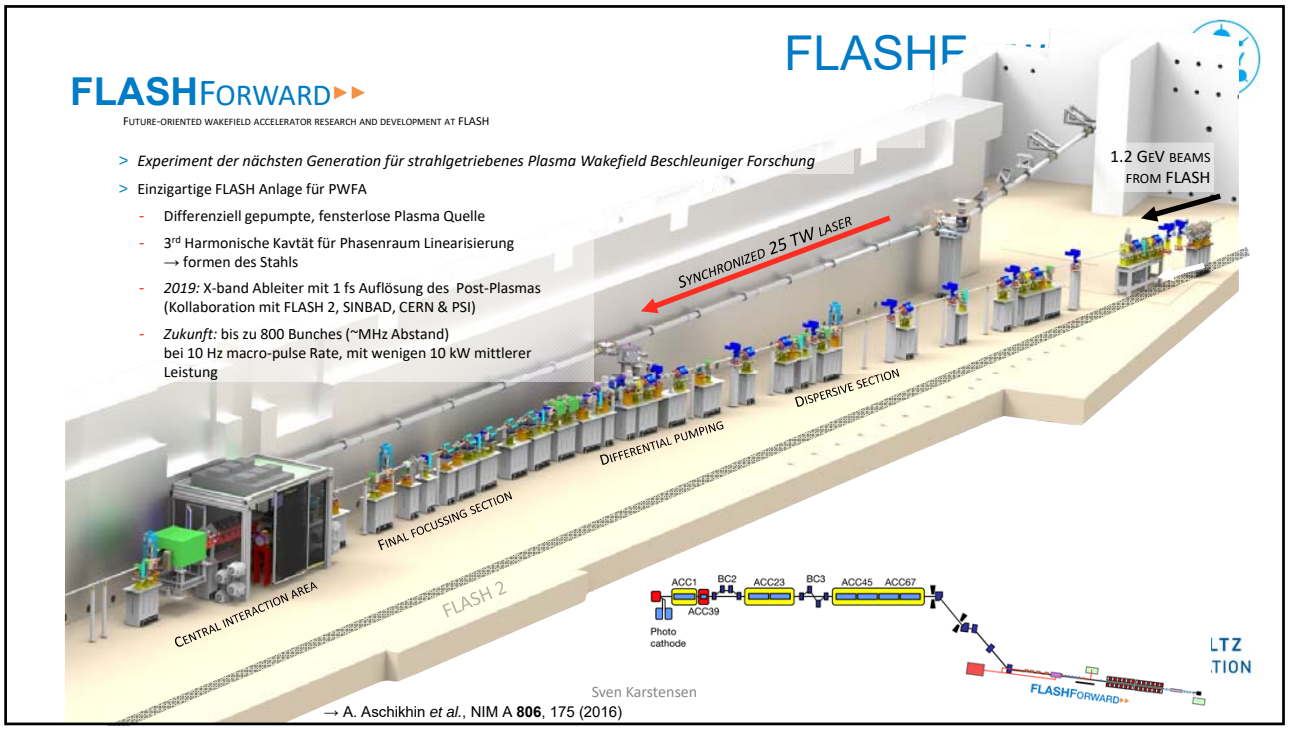
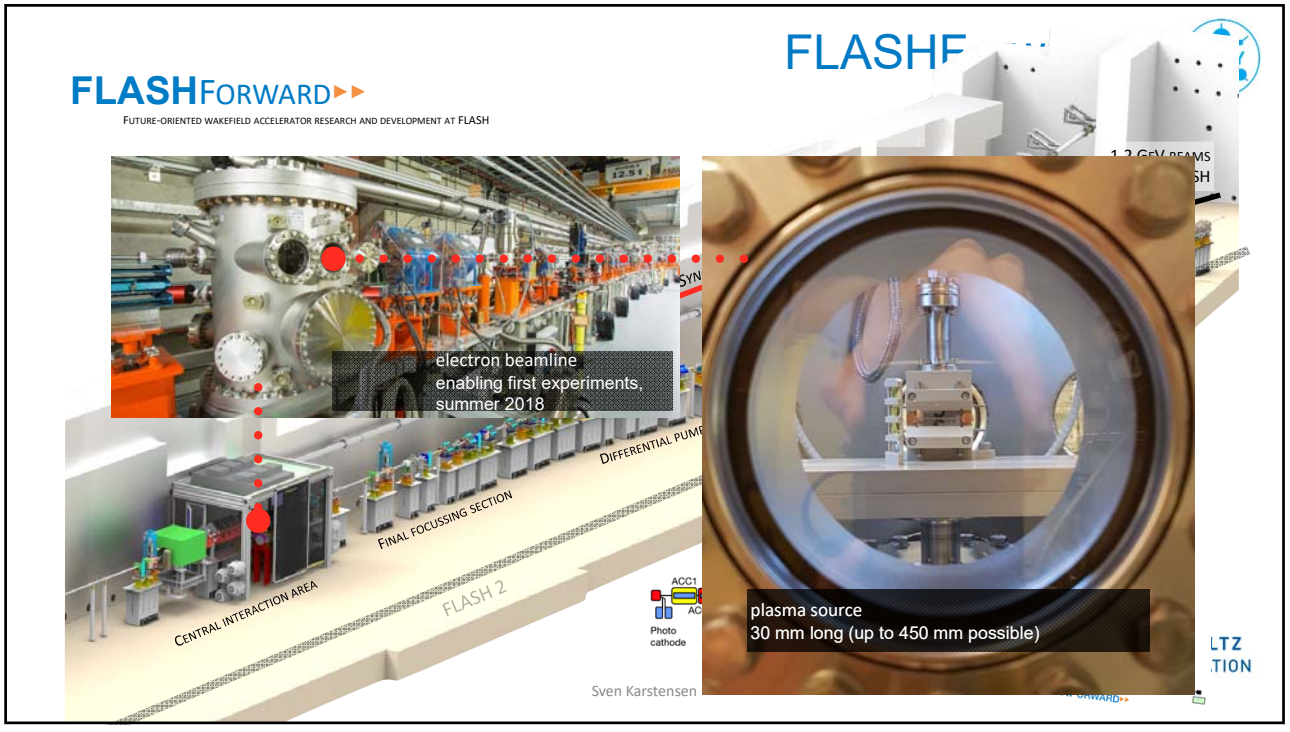


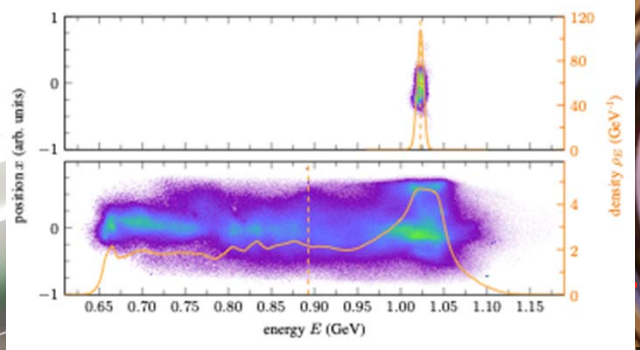
→ A. Aschikhin *et al.*, NIM A **806**, 175 (2016)



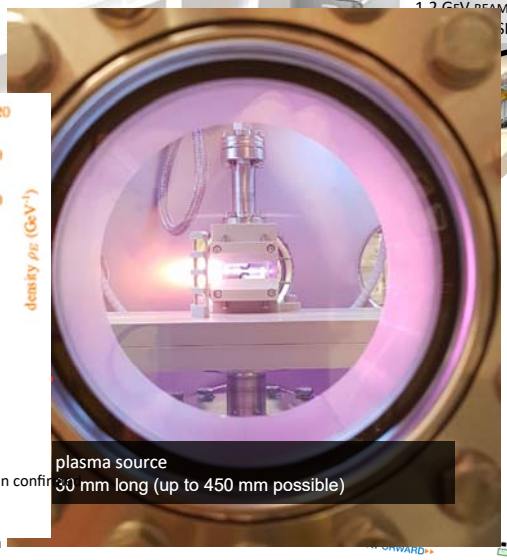
FLASHFORWARD

FUTURE-ORIENTED WAKEFIELD ACCELERATOR RESEARCH AND DEVELOPMENT AT FLASH

> erste PWFA beam-plasma Interaktion am 19. June 2018
> Aufbau erfolgreich abgeschlossen am 30. June 2018
> Installation ferig für externe Experimente seit 15. July 2018



> (12.3 ± 1.7) GV/m wakefield generated in 30 mm plasma cell
→ plasma cell scale length ~100 mm for GeV energy gain confir
> 12.7% total energy loss to plasma wakefield



Sven Karstensen

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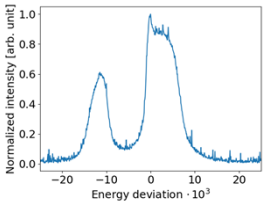
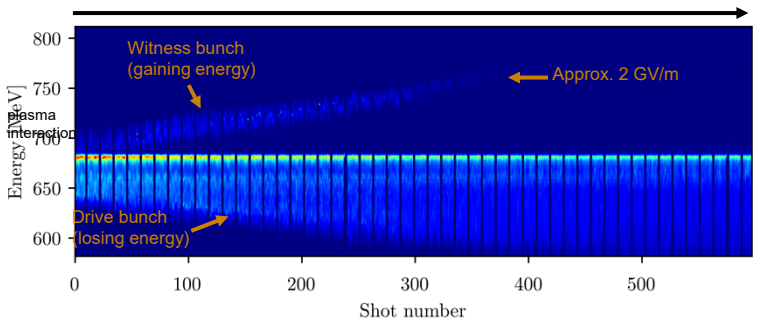
Core study: a plasma-based energy booster module

EXPERIMENTAL PLASMA INTERACTION, HIGH GRADIENT ENERGY BOOSTING, AND STABILITY STUDIES

Driver/witness creation using a wedge-shaped scraper in a dispersive section



Plasma density increases (beam–discharge delay decreases)



Double-bunch plasma interaction

> Indirect proof: first observation of witness acceleration with GV/m fields
(parameters: 1 kA driver peak current, 30 mm plasma cell, 10^{15} - 10^{16} cm^{-3} plasma density)
> *in summer 2019:* 20 cm plasma cell → multi-100 MeV energy gain + drive depletion;
beam loading control → explore energy spread and emittance conservation

> No shot selection or preferential ordering
> Excellent stability over short and long term (multiple hours) thanks to stability of the SCRF cavities and FEL-quality feedback systems

Sven Karstensen

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Technische Details

FLASHForward

Besonderheiten im Technischen Bereich

- Gruppenübergreifendes Arbeiten
- Große Anlage mit wenig Manpower
- Vor Neuentwicklung -> suche nach existierenden Komponenten
- Nur nicht-vorhandene Software wurde neu entwickelt

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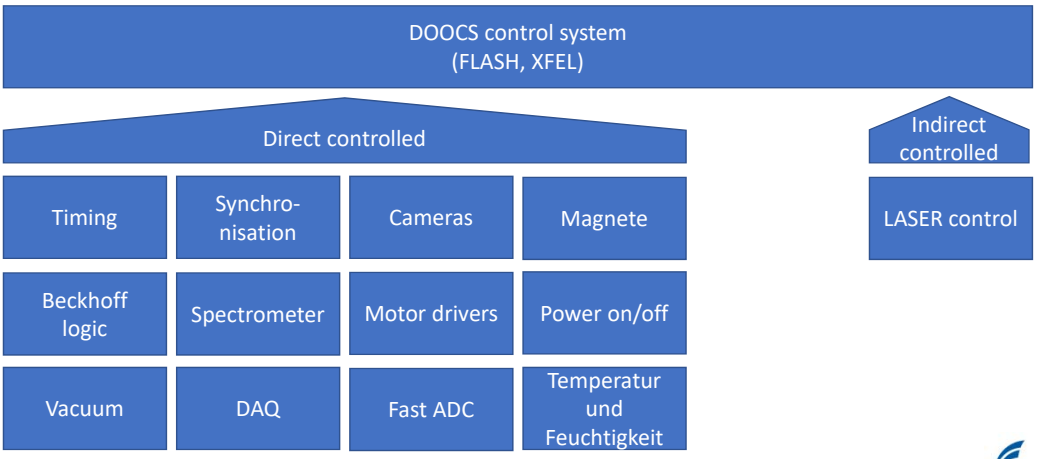
Overall FFWD Control System



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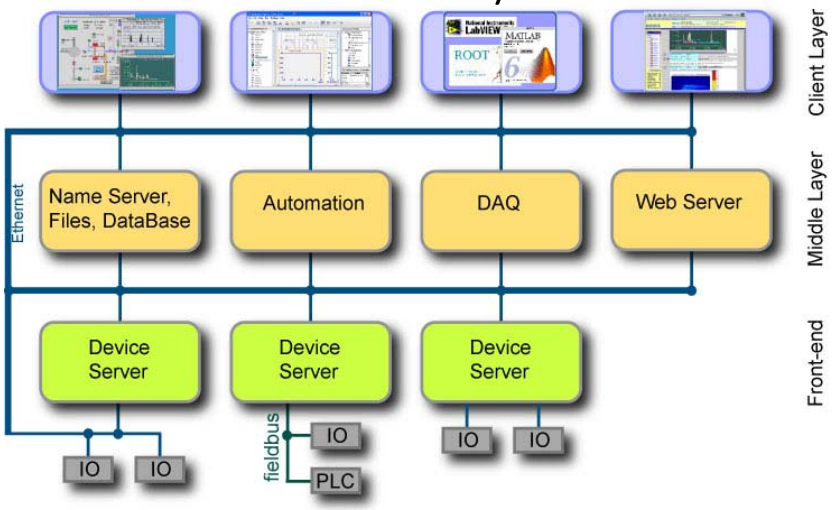
DOOCS Control System



DOOCS, das Distributed Object Oriented Control System wurde für FLASH entwickelt und erfolgreich bei FLASHForward eingesetzt

Ausserdem wird/wurde es für den XFEL Beschleuniger (3,2 km , ca 5km total) erweitert

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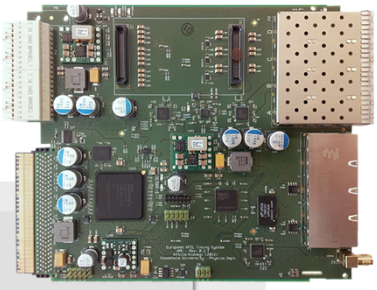
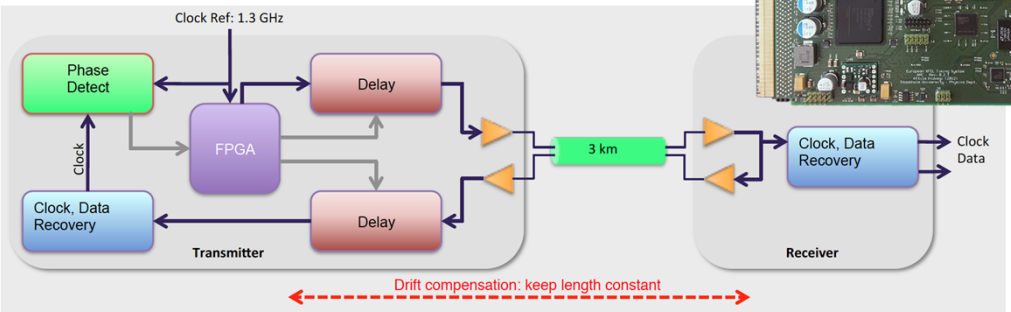
FLASH timing





Property: MCS4 group

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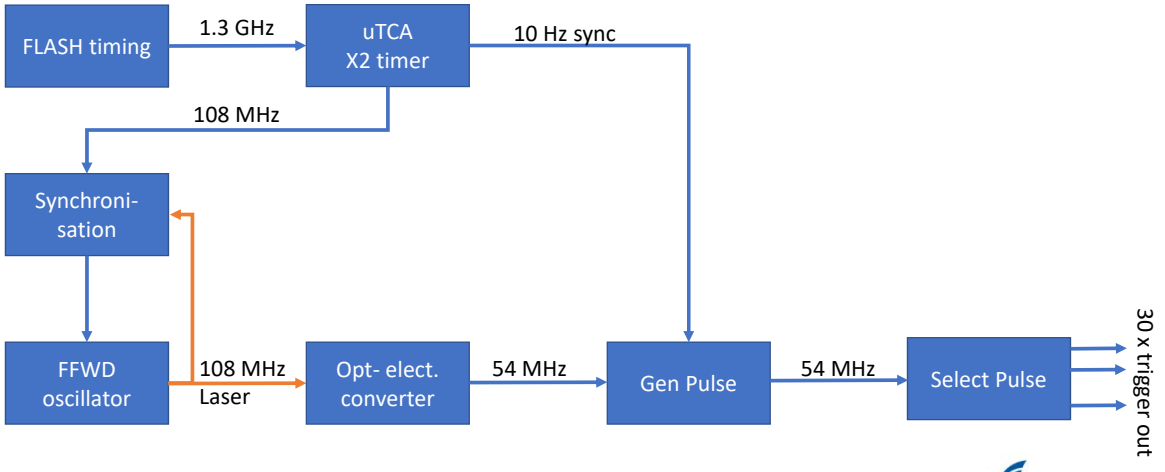
Synchronisation mit FLASH



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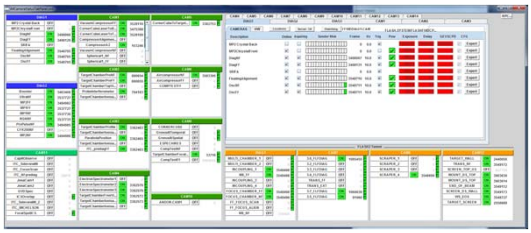
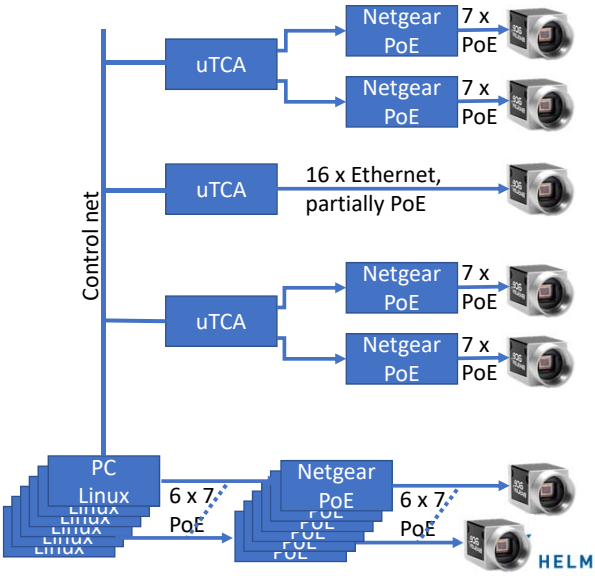
Camera Controls

- Kombination von Ethernet und PoE Geräten
- Direct Link für extrem hohe Auflösung
- Shared Link für geringere Auflösung (bis zu 2 Mpixel)
- Integriert in DOOCS
- Über 80 Kameras





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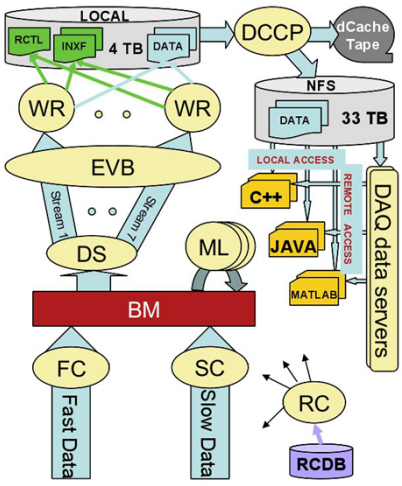
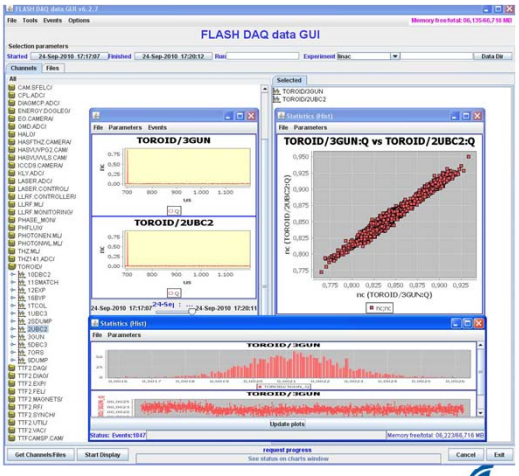
DAQ – Data Acquisition



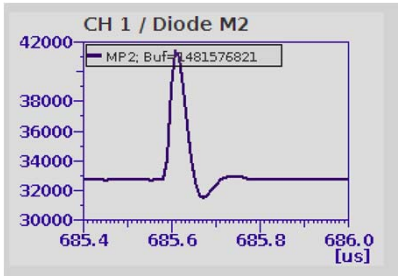


Property of V. Rybnikov

FLASHForward

ADC & Photo Diodes

- MTCA.4 (µTCA for Physics Implementation)
- 4 Kanal PCI Express Verbindungen
- 10 Kanäle mit 125 MS/s 16-bit ADC
- 10 MS/s bis 125 MS/s Sampling Speed pro Kanal
- AC und DC Eingänge



Thorlabs
PDA 63 A
Switchable Gain Detecto
350-1100 nm,
10 MHz BW,
13 mm2, 8-32 Taps

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Ein paar Zahlen

- 59 Computers
- 80+ Cameras
- 54 Schritt Motoren
- 92 Piezo Motoren
- 8 Spectrometer
- 10Hz Wiederholrate
- 10 Gbit Ethernet

- Control System Staff: 2

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Rechnersysteme

Computing hardware

- uTCA
- DELL Power Edge R330
- Standard PC
- Raspberry Pi
- Beckhoff

Operating Systems

- Mac
- Windows
- Linux

Computing software

- C++
- Python
- Matlab
- Labview

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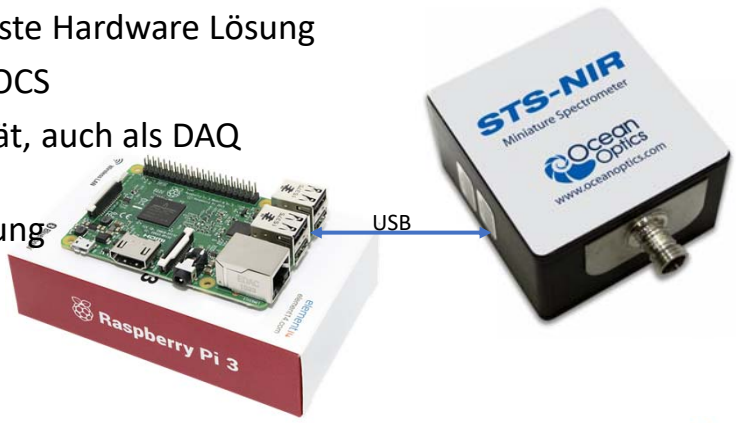
Raspberry Pi und Spectrometer

- Beste und günstigste Hardware Lösung
- Integration in DOOCS
- Volle Funktionalität, auch als DAQ Komponente
- Plug and play Lösung



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Vacuum

- Remote gesteuerte TCPIP und RS232 Geräte
- Fully integrated in control system

Agilent
Turbo V-551 HT

Ethernet

RS232

Agilent TwisTorr 84
FS-AG rack controller

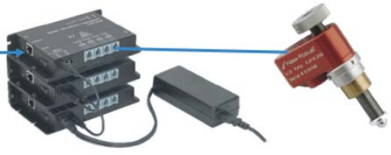
MOXA
Nport 5410

Edwards SCU-800

FLASHForward

Movement

Ethernet



Newport Pico Motors

PI Hexapod

Stepper motors

Piezo motors

PI Hexapods are more Versatile than Conventional Positioners

FLASHForward ▸▸ DESY

Generelle Probleme und Lösungen

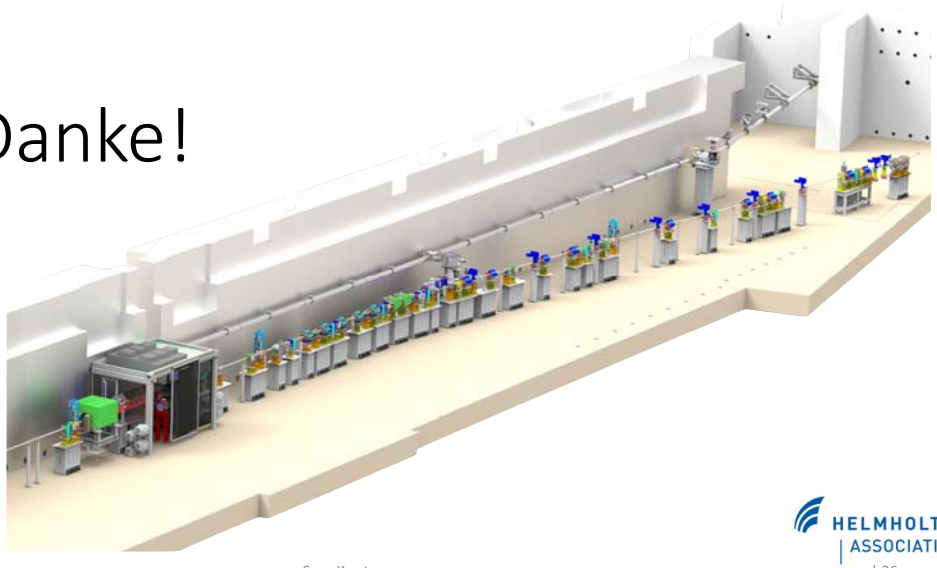
- Datenmenge
- Datensicherung
- Geschwindigkeit
- Übermotivierte junge Physiker

Lösungen:

- Dickes Fell und viel erklären
- High speed ethernet (10GBit)
- Lokale DAQ
- Extrem schnelle und leistungsfähige Computer

FLASHForward ▸▸ DESY

Danke!



Instrument control at MLZ
-
PLC Interface Layer Standardisation

Dr. Enrico Faulhaber
Instrumentsteuerung (FRM2)

MLZ is a cooperation between:

JÜLICH Forschungszentrum | Helmholtz-Zentrum Geesthacht Zentrum für Material- und Küstenforschung | Technical University of Munich

MLZ: quick intro

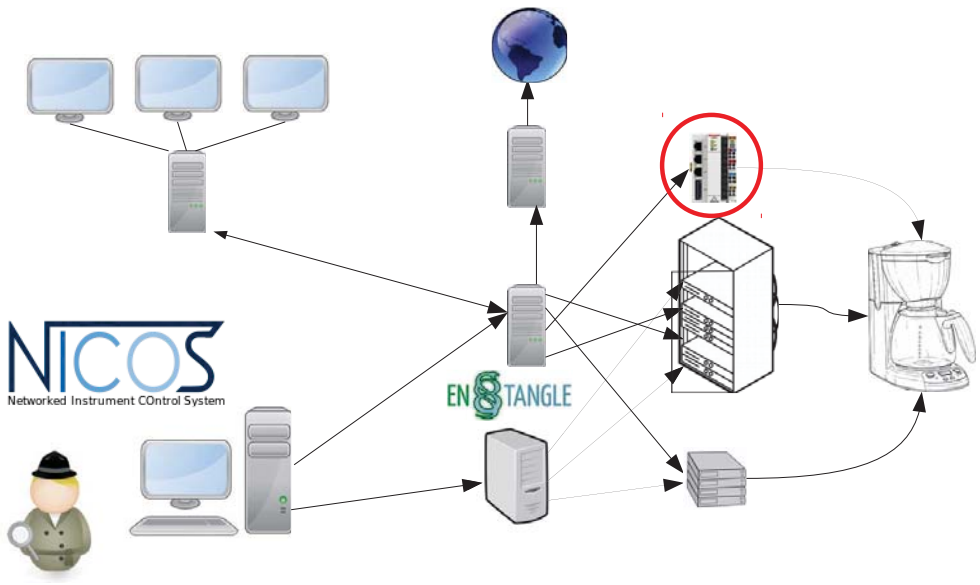
- neutron research facility
- cooperation between several partners:
  FRM2 (TUM), JCNS (FZJ), HZG,…
- located in Garching
- 25 well running instruments, still adding more
- continuous source, 60 day cycles
- experiments take between 6h and 21d
- big international communities

→ high pressure to have working instruments

Overview

- Instrument control
- The Problem
- How to Solve
- Solution
- Demo

Instrumentcontrol – quick overview



The problem

- broad range of needs, capabilites, used hardware
- each instrument subsystem is developed independently
- distinct requirements → distinct solutions
- individual conventions → individual solutions
- interacting with dozens of distinct, individual systems

→ nightmare

How to solve

- standardisation:
  - define transport layer
  - give meaning to data → information
  - provide metadata

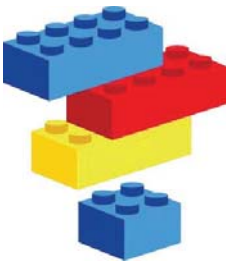
classical PLC based solutions

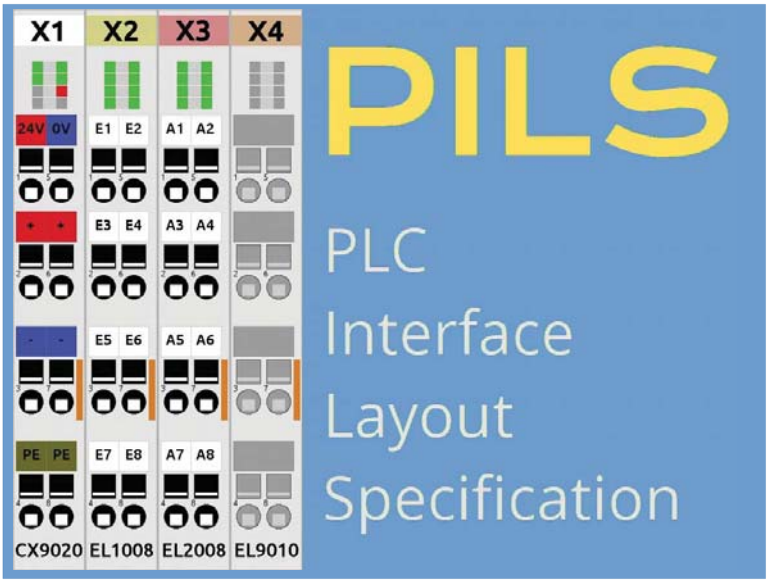
- inputs + outputs of various types
- cyclic execution of a task/program (every 1..100ms)
- special (programming) languages, even graphical ones
- data exchange via several protocols
- normally programmed using 'Bits and Bytes'
- remote control needs another configuration:
  'which Bit/Byte means what'

  → duplication of work!
  → error prone

standardisation goals

- transport layer well documented or open source
- detection of conformity
- 'catalog' of meaningful metadata
- definition of core functionalities → devices
- abstraction of devices:
  - main values: accessible at high speed
  - other values accessible in defined way
  - clear definition of a 'state' (only few states!)
  - support additional parameters & commands
- easy access via generic debug aids





https://forge.frm2.tum.de/public/doc/plc/master/html/

realization – transport layer

- providing access to a common range of indexable Bytes
- Beckhoff: ADS or ModbusTCP
  (well documented → easy to implement)
- using the flag area („Merkerbereich“) for data exchange

realization – metadata

- transferred by „Indexer“
- addressable by mailbox register
- various types of information:
  - name
  - unit
  - limits
  - identification of interface structure
  - parameters/commands
  - …

realization – metadata

- Example:

Byte index	7	6
N	AC K	Inf
N + 1	Device numb	
N + 2	DATA byte 0	
...	...	
N + M-1	DATA byte M	

DATA byte	
0	Type code, see Type codes - special, simple and normal devices, or 0
2	Device size or Indexer size
4	Device address or Indexer offset
6	Device unit or 0
8	Device flags or Indexer flags
10	
12	Absolute minimum of device value or 0
14	
16	Absolute maximum of device value or 0
18	
20	Device name or name of the PLC

realization – detection of conformity

- Bytes 0..3: MAGIC number
- Bytes 4..5: Indexer offset
- several more consistency checks:
  - information queried from Indexer
  - validity of type codes
  - consistency of memory layout
  - …

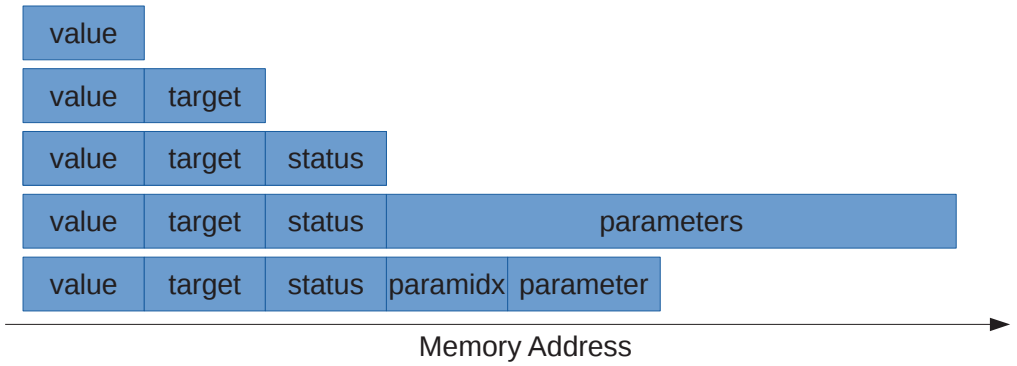
realization – detection of conformity

- Example:

```
0001 VAR_GLOBAL
0002     (* persistent stuff up to %MB64 *)
0003     fMagic          AT %MB0    : REAL := 2015.02;
0004     iOffset         AT %MB4    : WORD := 64;
0005
0006
0007     stIndexer       AT %MB64   : ST_Indexer;
0008
0009     if_Temperature1 AT %MB100  : ST_FlatInput2;
0010     if_Temperature2 AT %MB116  : ST_FlatInput2;
0011     if_Temperature3 AT %MB132  : ST_FlatInput2;
0012     if_Temperature4 AT %MB148  : ST_FlatInput2;
0013     if_Enable       AT %MB164  : ST_DiscreteOutput;
0014     if_Polarity     AT %MB172  : ST_DiscreteOutput;
0015     if_Symmetric    AT %MB180  : ST_DiscreteOutput;
0016     if_U_Monitor    AT %MB188  : ST_AnalogInput;
0017     if_I_Monitor    AT %MB196  : ST_AnalogInput;
0018     if_I            AT %MB204  : ST_FlatOutput1;
0019     if_Unipolar     AT %MB220  : ST_FlatOutput1;
0020     (* next free is at %MB236 *)
0021
```

realization – abstraction

- several datatypes: int16, int32, int64, float, double
- optimised for quick access to 'value', 'target', 'status'
- access to parameters either direct or via indexed access
- access to commands only via indexed access



realization – abstraction

- Example:

```
0001 TYPE ST_ParamOutput64 :
0002 STRUCT
0003     value:      LREAL;
0004     target:     LREAL;
0005     extStatus:  DWORD;
0006     nErrId:     WORD;
0007     parmCtl:    WORD;
0008     paramValue: LREAL;
0009 END_STRUCT
0010 END_TYPE
0011
```

realization – abstraction

- Statuscode:

31..28	27..24	23..16	15..8	7..0
Status code	Reason	AUX bits 23..16	AUX bits 15..8	AUX bits 7..0

Status code	Meaning

Reason	Meaning
0b0001	Inhibit active ("Static problem")
0b0010	Timeout ("Dynamic problem")
0b0100	negative Limit
0b1000	positive Limit

0b0110	BUSY
0b0111	STOP
0b1000	ERROR
other	*Reserved*

realization – helpers

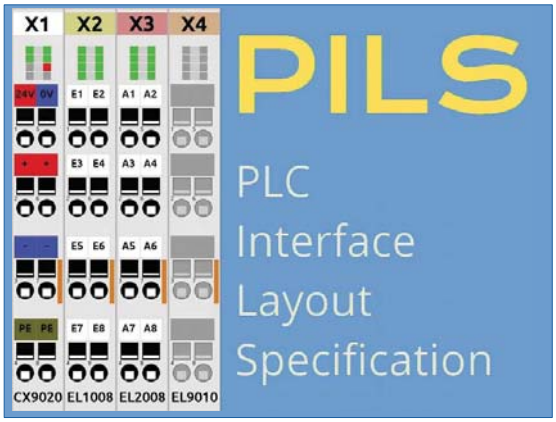
- Pluto – The **PL**C deb**ug** **To**ol
- read & display metadata from conforming PLC
- access to individual devices
- generate a minimal code skeleton
- natively python + PyQt, *.exe available:

https://forge.frm2.tum.de/public/pluto/

realization – impressions

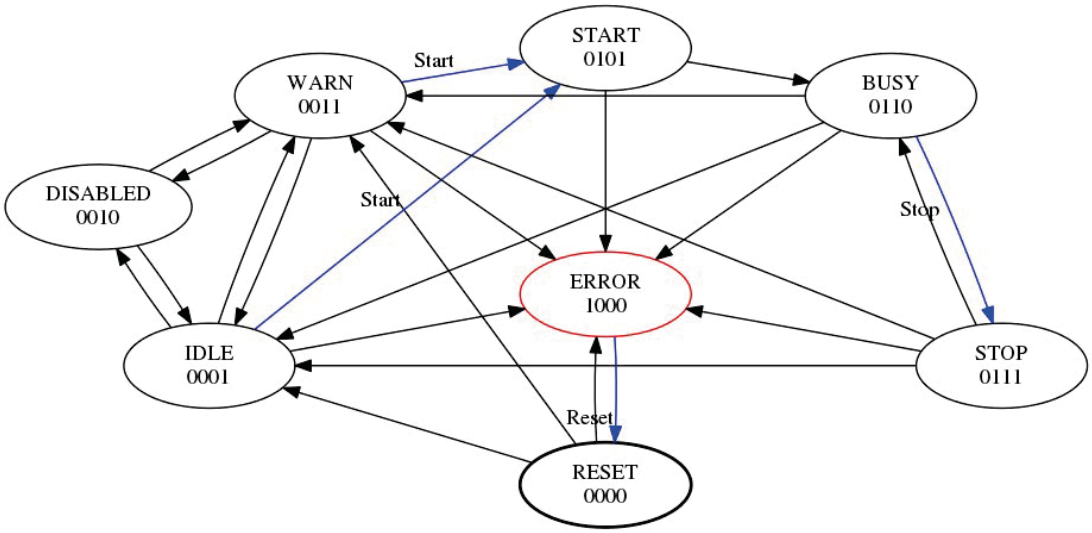
- Pluto – The **PL**C debu**g** **To**ol – live demo (if time permits)

Many thanks for your attention!



https://forge.frm2.tum.de/public/doc/plc/master/html/

details



8/4/19 Dr. Enrico Faulhaber 21

SEI-Frühjahrstagung 2019, Forschungszentrum Jülich

Qualitätssicherung Elektronik-Fertigung für DESY Hamburg

Dr.-Ing. Otto-Christian Zeides
Leiter Servicezentrum Elektronik DESY Hamburg

SEI-Tagung, 8.4. – 10.4.2019, FZ Jülich

HELMHOLTZ GEMEINSCHAFT

DESY.

Tätigkeitsschwerpunkte am DESY in Hamburg

- Weiterentwicklung der Teilchenbeschleuniger-Technologien
- Forschung auf dem Gebiet der Synchrotronstrahlung und der Nutzung dieser in verschiedenen Wissenschaftsdisziplinen
- Entwicklung auf dem Gebiet der Detektoren für Teilchenbeschleuniger
- Entwicklung auf dem Gebiet der Signalverarbeitung und –auswertung beim Betrieb von Teilchenbeschleunigern
- Forschung auf dem Gebiet der Teilchenphysik (theoretisch, experimentell)
- Ausbau und Betrieb der Teilchenbeschleuniger PETRA III, FLASH II und XFEL sowie LHC am CERN und KEK in Japan
- Betrieb eines Testbeams für Entwicklung

DESY.

Elektronik-Bedarf zur Erfüllung der Aufgaben von DESY

Für den Betrieb, die Steuerung und die Überwachung von Teilchenbeschleunigern sowie für die Signalerfassung, -auswertung und –speicherung wird ein breites Spektrum von Spezialelektronik aus Gebieten wie z.B. :

- Leistungselektronik
- HF-Technik
- Steuerungstechnik
- Sicherheitstechnik
- analoge und digitale Hochgeschwindigkeits-Signalverarbeitung
- Detektor-Frontend-Elektronik u.a.

benötigt.

Diese muss in der Regel individuell entwickelt und gefertigt werden.

Elektronik-Entwicklung für DESY in Hamburg

Wo findet diese Elektronik-Entwicklung bei DESY statt ?

DESY ist in verschiedene Forschungsbereiche aufgeteilt:

- **M** Teilchenbeschleuniger (Maschine)
- **FS** Forschung mit Photonen (Synchrotronstrahlung)
- **FH** Hochenergiephysik (Teilchenphysik)
- **AP** Astroteilchenphysik

Diese Bereiche sind wieder in viele einzelne Gruppen aufgeteilt.

Die Elektronik-Entwicklung findet einmal in den einzelnen Gruppen entsprechend ihres Schwerpunktes statt.

Darüber hinaus existiert eine eigenständige Elektronik-Entwicklungs-Gruppe **FE**, die im Auftrag anderer Gruppen DESY-weit Elektronik-Entwicklung betreibt.

Als eigenständige Gruppe existiert das Servicezentrum Elektronik **ZE**. Diese fungiert als interner EMS-Dienstleister.

Qualitätssicherung Elektronik-Fertigung für DESY

Qualitätssicherung beginnt mit der Elektronik-Entwicklung !!!

- Es werden 3 E-CAD Systeme Altium, EAGLE, Mentor Expedition verwendet.
- Weitere werden nicht zugelassen werden!
- Jedes System besitzt seine eigene Library. Werden von untersch. Gruppen gepflegt.
- Zusätzlich besitzt die **Z**entrale **E**lektronik in einem ERP System eine Artikel-Datenbank, basierend auf Herstellern und Hersteller-Artikel-Nummern.
- Die Bibliotheken der E-CAD Systeme sind mit der ERP-System Artikel-Datenbank verknüpft (über eindeutige Artikel-Nummern, z.B. Z012345).
- Durch das ERP-System ist eine Rückverfolgbarkeit der eingesetzten BE, LP, Baugruppen und Beschaffung gewährleistet.

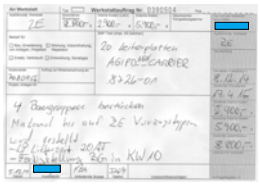
Qualitätssicherung Elektronik-Fertigung für DESY

Qualitätssicherung beginnt mit der Elektronik-Entwicklung !!!

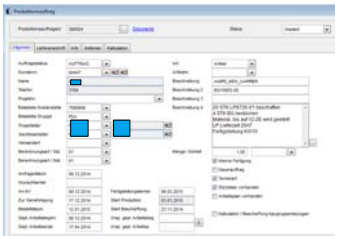
- Die **Z**entrale **E**lektronik berät alle Entwickler bei DESY zu:
  - Design for manufacturing DFM (Leiterplatten, LP-Bestückung, Gerätefertigung)
  - Design for testability DTM
  - Design unter Berücksichtigung der späteren Reparaturmöglichkeit
  - LP- und Gerätedesign unter EMV-Gesichtspunkten
- Die **Z**entrale **E**lektronik verwaltet die Gerber-Daten aller DESY-Leiterplatten und vergibt eindeutige Artikel-Nummern (mit Revisions-Nummern, im ERP-System generiert).
- Der LP-Entwickler ist das Bindeglied zwischen Entwicklung und Fertigung!
- Die **Z**entrale **E**lektronik kauft und prüft die unbestückten DESY-Leiterplatten.

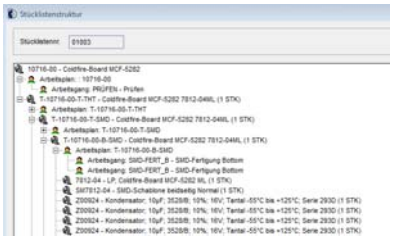
AV Projektsteuerung durch ERP-System orderbase

> Auftraggeber füllen einen Werkstattauftrag aus (wird ins ERP-System übernommen):



➢ Es werden Arbeitsgänge geplant sowie Material- und Fertigungskosten ermittelt und in das ERP-System eingetragen:



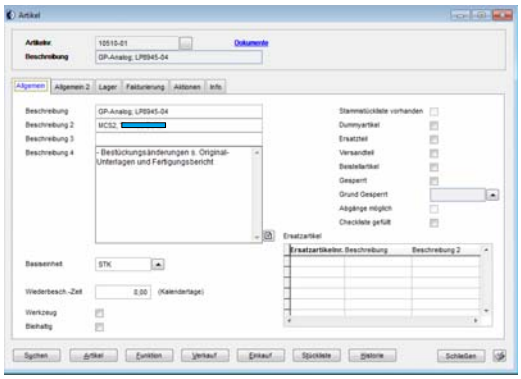


AV Checkliste für Werkstattauftrag

> Für jeden Werkstattauftrag wird eine Checkliste geführt, die mit dem Auftrag durch die einzelnen Arbeitsgänge mitläuft:

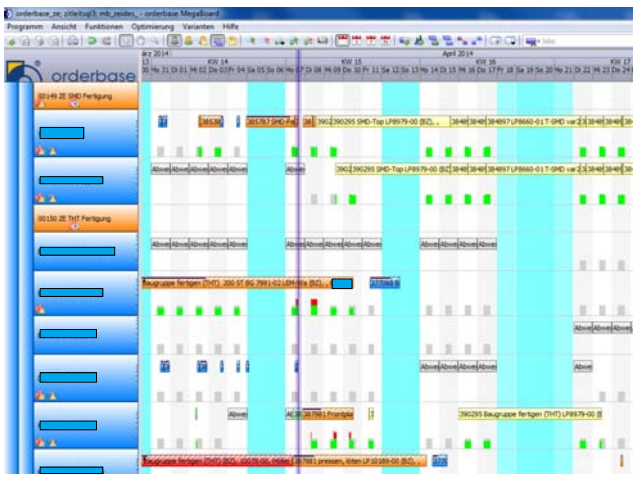
AV Artikel in ERP orderbase

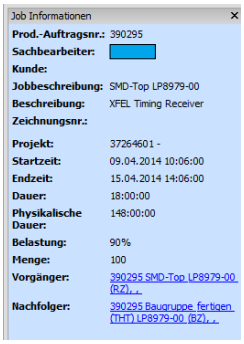
> Für jede LP, elektronisches BE, Baugruppe oder Gerät wird eine eindeutige Artikelnummer im ERP-System erzeugt:



> Alle für Einkauf, Fertigung und Prüfung relevanten Dokumente sind per Mausklick im Zugriff

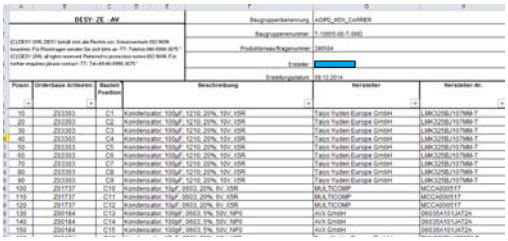
AV Werkstattsteuerung durch ERP-System orderbase





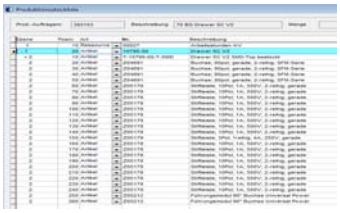
AV Artikelverwaltung in ERP-System orderbase

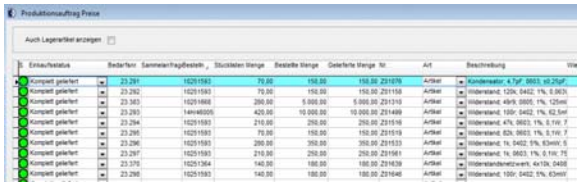
> Auftraggeber liefern Stücklisten als Excel-Datei:



überwiegend schon automatisch generiert
durch Entwicklungssysteme (EAGLE,Mentor,Altium)

> Diese werden in ERP-System in Stückliste des Artikels importiert:





SMD Qualitätssicherung im SMD-Lotpasten-Auftrag

- DESY verwendet einen Lotpasten-Schablonendrucker.
- Die Schablonen werden von der **Z**entralen **E**lektronik designt, da sie den Fertigungsprozess am besten kennen.
- Es ist bekannt, dass die häufigsten Fehler an einer Baugruppe ihre Ursache im fehlerhaften Lotpasten-Auftrag haben.
- **-->** Der Drucker wurde mit einem Kamera-System und Auswertesoftware nachgerüstet. (Leider nur 2D-SPI)

SMD-Lotpasten Schablonendrucker

SMD Qualitätssicherung im SMD-Bestückungsprozess

- Um Bestückungsfehler auszuschließen, sind die notwendigen Dokumente (Stücklisten, Pick&Place-Datei, Bestückungsdruck) auf Vollständigkeit und Eindeutigkeit in der Arbeitsvorbereitung zu prüfen und zu korrigieren.
- Die verschiedenen E-CAD-Systeme erzeugen unterschiedliche Dateiformate (EXCEL-Dateien, Text-Dateien, CSV-Dateien).
- Die **Z**entrale **E**lektronik hat dazu Tools entwickelt, die diese Dateien in einheitliche Zielformate wandeln.
- Dabei werden Inkonsistenzen zwischen Stücklisten und Pick&Place-Dateien schon vor Beginn der Bestückung erkannt.
- Klimatisierung der SMD-Werkstatt sorgt für Prozesssicherheit während des Bestückungsprozesses (Zustand der Lotpaste).
- Die Bestückungsautomaten melden Fehler im Bestückungsprozess.
- Vor dem Reflow-Löten erfolgt eine manuelle optische Kontrolle auf Bestückungsfehler.

SMD Qualitätssicherung im SMD-Bestückungsprozes

- Es kommt ein hochpräziser SMD-Bestückungsautomat zum Einsatz.
- Implementiert sind vielfältige Überwachungsfunktionen z.B. Höhenkontrolle, Anpressdruckkontrolle.

SMD-Bestückungsautomat

SMD Qualitätssicherung im SMD-Reflow-Lötprozess

- DESY verwendet einen Dampfphasen-Lötofen.
- Prinzip bedingt ist damit eine Überschreitung der Peak Temperatur ausgeschlossen.
- Lötprofile können programmiert werden und werden durch einen Regelkreis wiederholbar abgefahren.
- Zusammen mit der Klimatisierung des Raumes ist damit die Prozesssicherheit hergestellt.
- Lötprofile werden im Artikel festgehalten.

Dampfphasen-Lötofen

SMD Automatisches optisches 2D-Inspektions-System

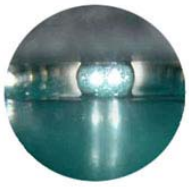
> Prüfung der Qualität von SMD-Lötverbindungen nach Reflow-Prozeß:

2D-AOI-System

SMD Qualitätssicherung in SMD-Fertigung

- Für manuelle Begutachtung stehen Mikroskope zur Verfügung.
- Werden neue Bauelemente-Generationen (z.B. neue BGAs) erstmalig eingesetzt wird im Zweifelsfall bei einem Dienstleister eine Röntgenuntersuchung (AXI) in Auftrag gegeben.

BGA-Inspektion



THT Einsatz einer Selektivlötwelle

- Für reproduzierbare THT-Lötverbindungen wird in der **Z**entralen **E**lektronik eine moderne Selektivlötwelle eingesetzt
- Sie besitzt eine programmierbare Fluxereinheit sowie eine geregelte Vorheizung (Ober-Unterhitze)
- 2 Tiegel erlauben den Einsatz von 2 verschieden großen Düsen in einem Durchlauf
- Eine Höhenkontrolle (Durchbiegung der LP) und Wellenhöhenerkennung sowie Düsenreinigung erlauben eine reproduzierbare Lötqualität

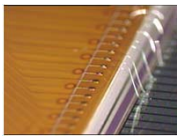
SMD/THT/Prüffeld Fertigungsbericht

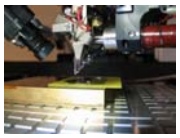
- Für jeden Artikel wird ein Fertigungsbericht im Artikel-Ordner gepflegt.
- Fehler, Auffälligkeiten, Verbesserungsvorschläge werden dort festgehalten.
- Der Fertigungsbericht wird am Ende eines Produktionsauftrages zusammen mit allen Fertigungsdokumenten in einer Abschlussdokumentation an den Auftraggeber übergeben.

Fertigungsbericht	Bezeichnung: Modifikation BG Getterpumpen Analog			
Baugruppen-Nr.: 10510-01	Anzahl: 31	WA396982		
LP-Nummer: 8954-04	Arbeitsvorbereiter: [redacted]		Datum der letzten Speicherung: 08.03.2018	
Der Fertigungsbericht wird fortlaufend weiter geschrieben. Das gilt auch wenn der Artikel für unterschiedliche WA's gefertigt wird.				
Mitarbeiter / Datum	**Beschreibung**	**Lösungsvorschlag**	**Durchgeführte Maßnahmen**	**Erledigt von / am**
Zei, 7.3.18	Lotbrücken J1, J2 und J3 setzen		wurde gelötet	[redacted] 07.03.18
Zei, 7.3.18	Widerstände R14,15,16,17,18,19 auf 240 k ändern	Z00858 einlöten	wurden getauscht	SMD-Fertigung 07.03.18
Prüfen/Julia 07.03.18	alles in Ordnung!			

Bonden Qualitätssicherung im Bondlabor

Automatischer Dünndrahtbonder Serie DELVOTEC G5
für Single- und Multichip Dünndraht



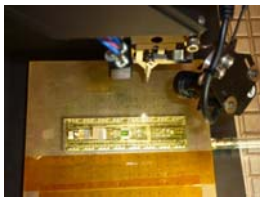


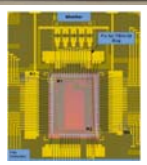
Pulltester XYZTEC

Bildanalyse-System ZEISS Axiotech 25 H mit Axio Vision 3.0
Vergrößerung von 50X bis 500X
Erstellen von Bildarchiven und Berichten

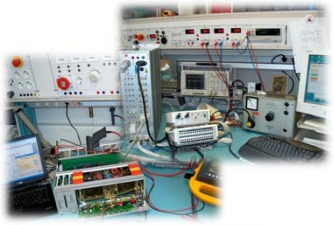
Beispiel ausgeführter Bondarbeiten:

CMS HDI Pixel-Detektor upgrade

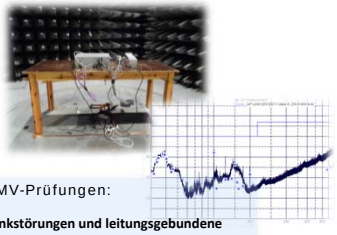




Prüffeld Leistungen



Durchführung von Funktionstests:
Es werden alle Ein- und Ausgänge sowie Funktionen - in Absprache mit dem Anwender - im Normal- und Störbetrieb überprüft. Konstruktionsfehler werden behoben, Unterlagen werden entsprechend geändert. Verbesserungsvorschläge werden nach Absprache eingearbeitet und umgesetzt.



EMV-Prüfungen:

Funkstörungen und leitungsgebundene Beeinflussung

Störfestigkeit und Störaussendung

****Zusammenarbeit mit zertifizierten Laboren****

Gerätesicherheits-Prüfungen:

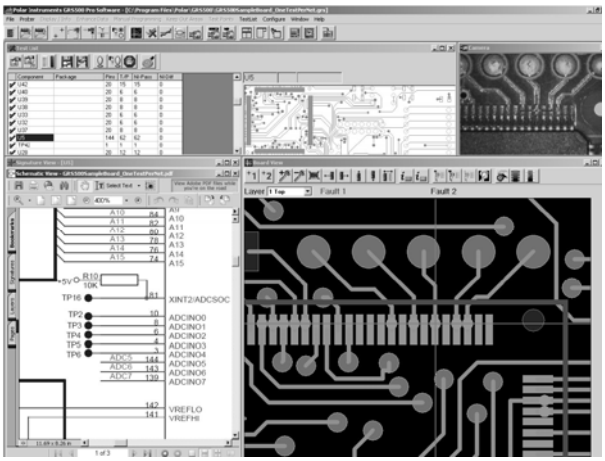
VDE-Test

Prüfung nach Niederspannungsrichtlinie

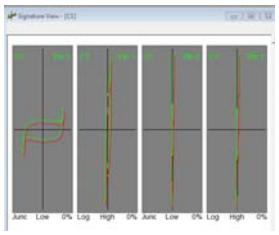
Flying Probe Tester

Prüffeld Flying Probe Tester

> Knotenimpedanzmessung:



Bedienoberfläche der PC-Software



Ausgewählte Signaturen

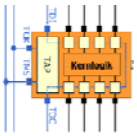
Flying Probe Tester Polar Instruments

Erkennung von Bestückungsfehlern (BE-Typ, Wert, Polarität, Unterbrechung, Kurzschluss, LP-Fehler nach Lötprozess).

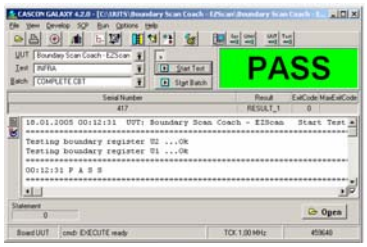
Prüffeld JTAG Boundary Scan Prüfplatz

Komplexer Prüfaufbau inklusive aller I/O-Leitungen

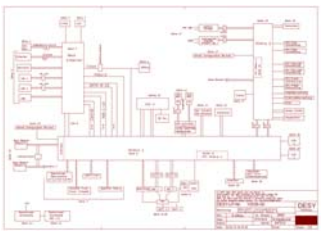
Prüfling Reglerbaugruppe für Korrekturnetzteil



BSCAN fähiges BE

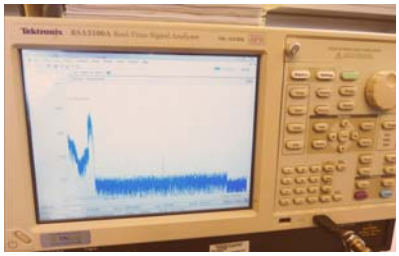


Bedienoberfläche PC-Software



Blockschaltbild Prüfling

Prüffeld EMV-Prüftechnik für leitungsgebundene Störungen



Spektrumanalysator

HF Generator 9 kHz – 400 MHz (IEC 61000-4-6)

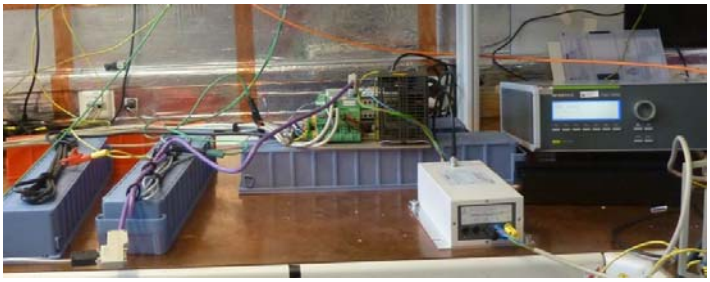
ESD, Burst, Surge, Spannungseinbrüche Generator Kombigerät (IEC 61000-4-2/4/5/8/9/11)

Koppelzange

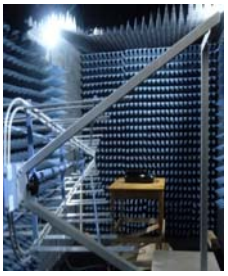
Scope

Feldsonden

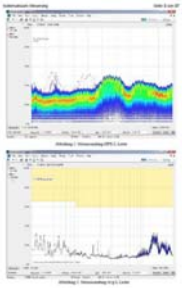
Prüffeld — EMV-Prüftechnik für leitungsgebundene Störungen



Prüfaufbau im Prüffeld bei DESY



EMV-Messungen an der HAW



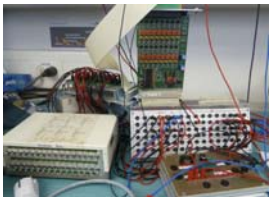
EMV-Messprotokoll,
Generiert von der LabView-Applikation,
Erstellt bei DESY

Prüffeld — Konventionelle Prüfverfahren

DESY Kabeltester

Die Prüfgeräte sind in der Lage die Verbindungen eines Mustergerätes selbst lernend (teach-in) zu erkennen
(max. 192 Verbindungen).

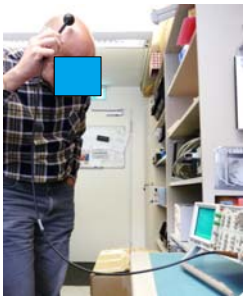
Getestet wird auf Unterbrechungen, Kurzschlüsse und Vertauschungen.



Natürlich auch noch universelle und gerätespezifische konventionelle Prüfeinrichtungen.

Qualitätssicherung Elektronik-Fertigung für DESY

- ✓ Qualitätssicherung beginnt mit der Elektronik-Entwicklung !!!
- ✓ Ganz wichtig ist die enge Verbindung zwischen Entwickler, Layouter, LP-Hersteller, Bestücker und deren Rückkopplung.



Vielen Dank für die Aufmerksamkeit.

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Simulation durch Auslese

— Modellierung von Kernspulen zur Schaltungsberechnung —

Wolfram Sorge

08. April 2019

HZDR

HELMHOLTZ ZENTRUM DRESDEN ROSSENDORF

2020-02-17 15:58

Inhalt

HZDR Forschungstechnik

2020-02-17 15:58

Zum Thema

Auslese in technischen Anwendungen

Versuchs- und Verwurfsmethoden anwenden, wenn:

- Einfluß von Parametern schwer einzuschätzen ist.
- Systeme sich stark verändern.

Benötigt werden:

- ein wenig Intelligenz:
  - Bisher ermittelte Werte von Parametern.
  - Ziel der Berechnung und Vergleichskriterium.
- wirklichkeitstreue Modelle des Gegenstands
- Algorithmen, die Parameterwerte erzeugen.

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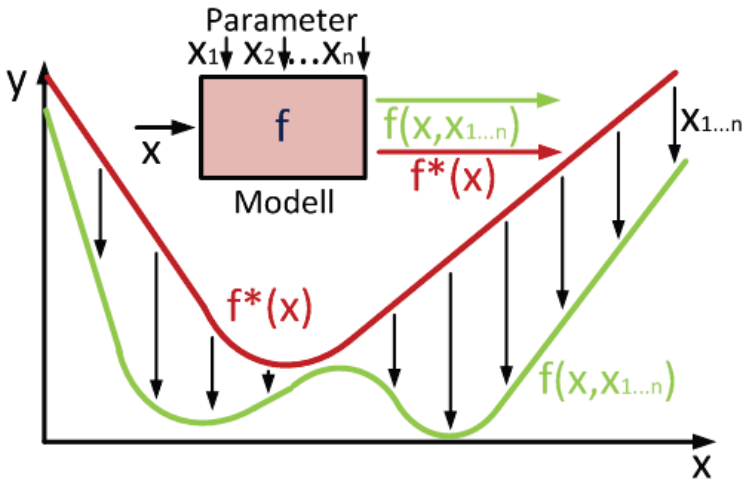
Zum Thema

Ergebnisse anpassen



- System/Modell in Grundstruktur vorhanden
- Parameter $x_1 \ldots x_n$ verändern Ergebnis
- Angleichen der Transferkennlinie an eine Vorgabe

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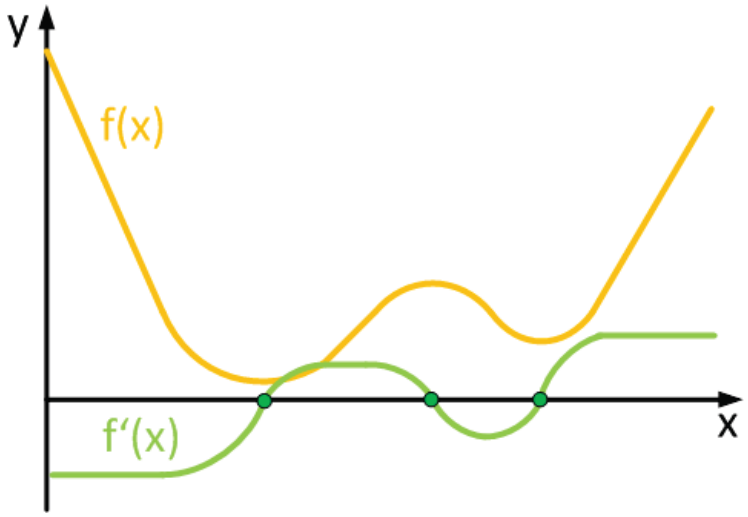
Zum Thema

Andere Verfahren



Gradientenverfahren:

- Z. B. Newtonverfahren, neuronale Netze usw.
- Kenntnis über Ergebnisverläufe und deren Ableitungen nötig.

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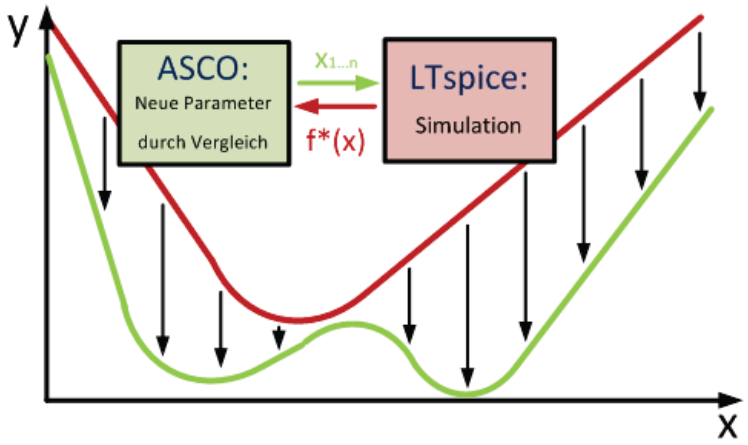
Optimieren und Anpassen

Simulation und Optimierung



Gesucht wird:

- Prozedur zum Finden geeigneter Parameter

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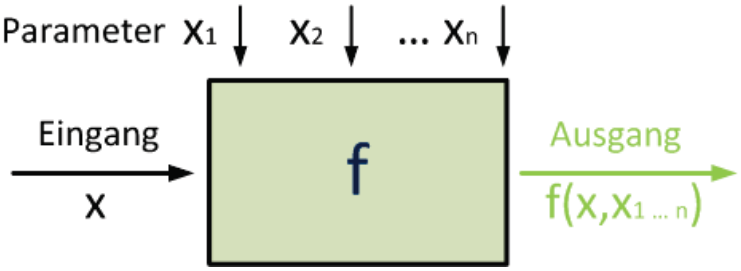
Optimieren und Anpassen

Evolutionäre Parameter- und Kurvenanpassung

Differential Evolution (DE):

- Anwendung auch auf nichtdifferenzierbare Funktionen
- Betrachten äußerer Systemeigenschaften (Black Box): Bewerten eines Ergebnis' mit seinen Parametern
- Bei n Parametern Lösung eines n-dimensionalen Problems



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Optimieren und Anpassen

Ein kurzer Blick auf ASCO

ASCO:

- A SPICE Circuit Optimizer nutzt DE-Algorithmen [AS410]

Mutation:

- Neuer Parametervektor durch Addition einer gewichteten Differenz zwischen zwei mutierten Vektoren zu einem vorhandenen Vektor:

$$\mathbf{v}_{i,G+1} = \mathbf{x}_{r_1,G} + F \cdot (\mathbf{x}_{r_2,G} - \mathbf{x}_{r_3,G})$$

Kombination:

- Neue Vektoren durch Tausch der Elemente aus vorhandenen Vektoren:

$$\begin{pmatrix} \mathbf{x}_{r_1,G} \\ \mathbf{x}_{r_2,G} \\ \vdots \\ \mathbf{x}_{r_n,G} \end{pmatrix} = \begin{pmatrix} B_S^1 & B_R^1 & H_C^1 \\ B_S^2 & B_R^2 & H_C^2 \\ & \vdots & \\ B_S^n & B_R^n & H_C^n \end{pmatrix}$$

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Optimieren und Anpassen

Mutation und Auslese

Ausgang: Menge möglicher Werte eines Parameters

1. Iteration: Auswahl von geeigneten Werten daraus

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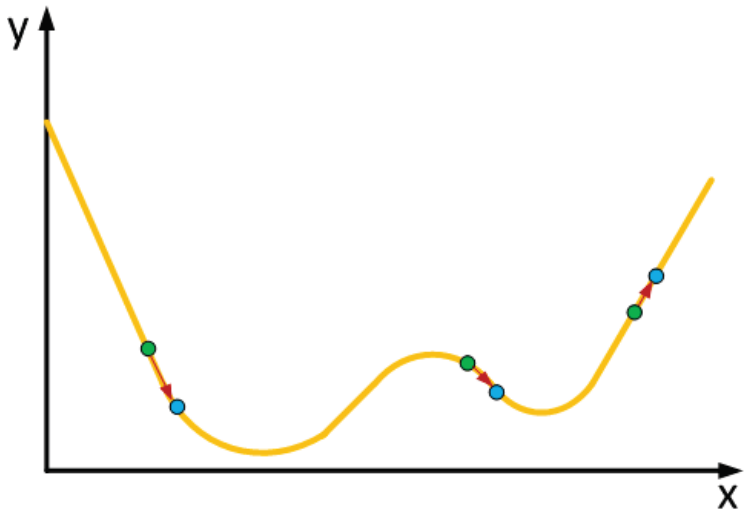
Optimieren und Anpassen

Mutation und Auslese



2. Iteration: Alte und neue mögliche Werte eines Parameters

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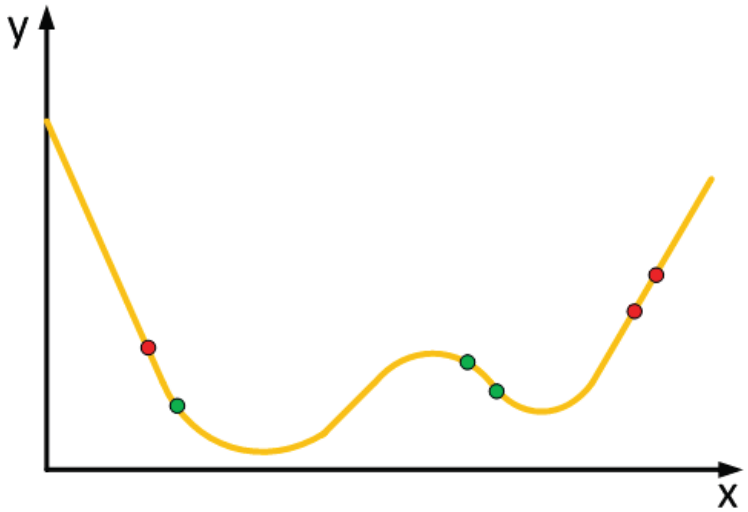
Optimieren und Anpassen

Mutation und Auslese



2. Iteration: Auswahl von geeigneten Werten daraus

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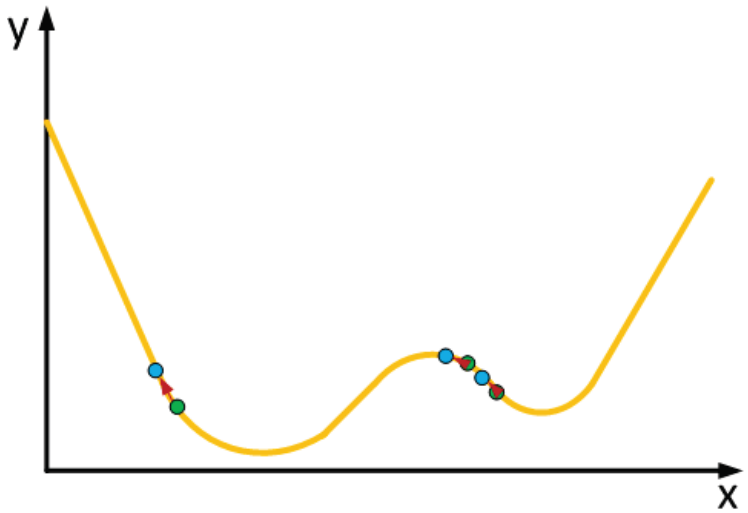
Optimieren und Anpassen

Mutation und Auslese



3. Iteration: Alte und neue mögliche Werte eines Parameters

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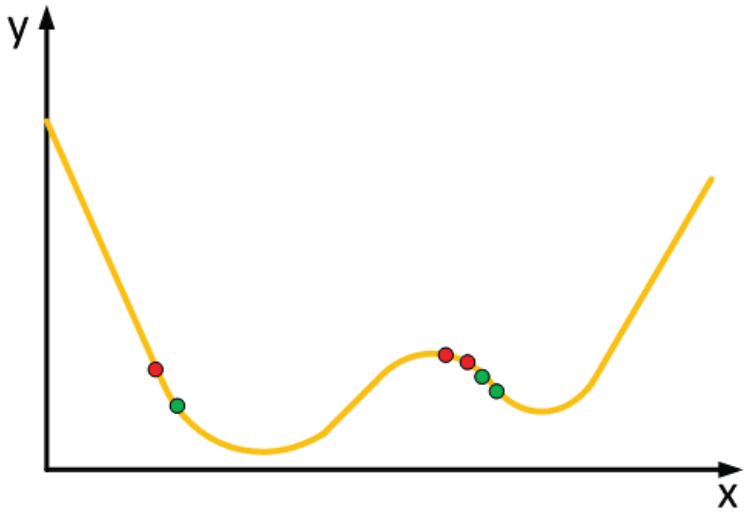
Optimieren und Anpassen

Mutation und Auslese



3. Iteration: Auswahl von geeigneten Werten daraus

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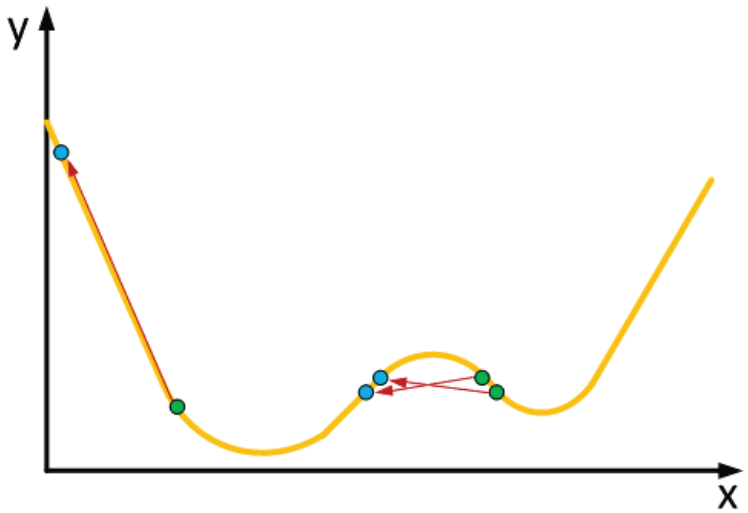
Optimieren und Anpassen

Mutation und Auslese



4. Iteration: Alte und neue mögliche Werte eines Parameters

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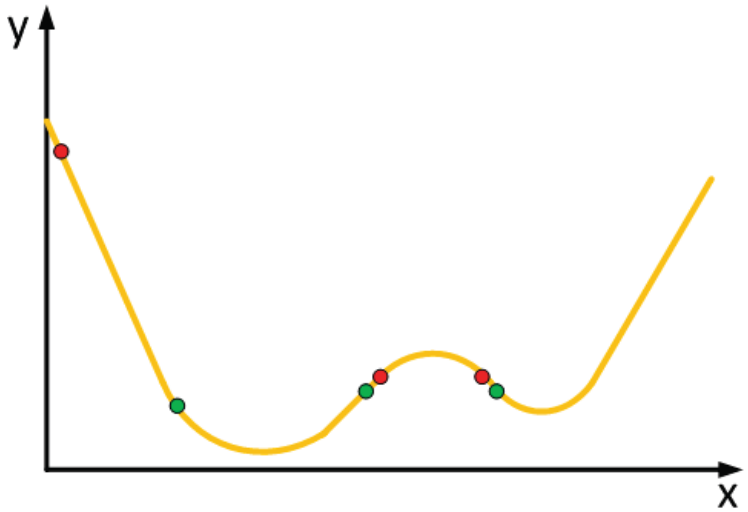
Optimieren und Anpassen

Mutation und Auslese



4. Iteration: Auswahl von geeigneten Werten daraus

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Optimieren und Anpassen

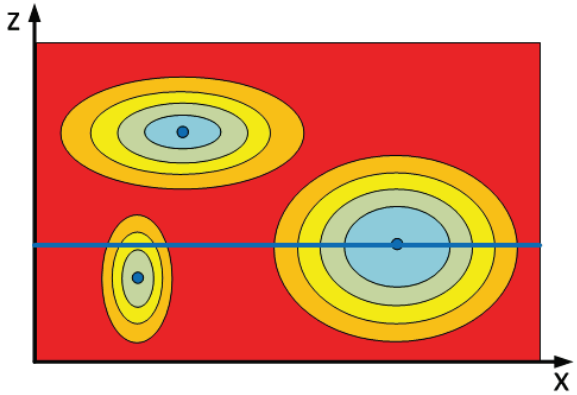
Mehrere Parameter

Dimension der Optimierung (Freiheitsgrad):

Freie Parameter bilden Basis für ein Abweichen vom Optimum.

Einschränken von Freiheitsgraden:

- Geringere Zahl von Minima bei der Optimierung.
- Meiden nichtoptimaler lokaler Minima.
- Kürzerer Optimierungsweg.



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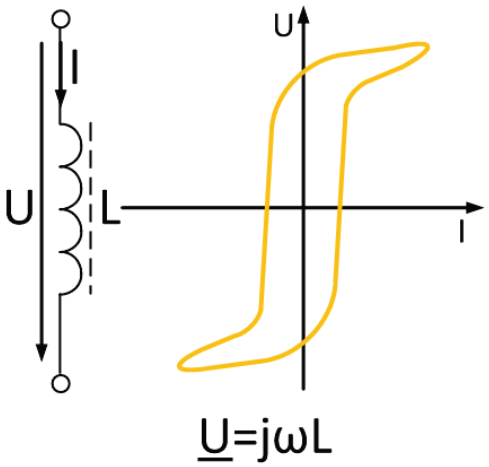
Modellierung

Kennlinie eines realen Bauelements

Beispiel: U-I-Kurve einer mit Wechselstrom durchflossenen Spule



Nichtlineares Verhalten:

- Wirkung von Parametern schwer einzuschätzen.
- Wenig Angaben von Herstellern

Wirkung in Kernspulen:

- Magnetische Sättigung im Kern mindert Impedanz.

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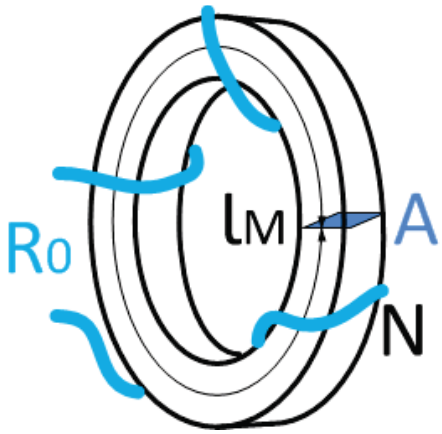
Modellierung

Magnetische Parameter einer Ringkerndrossel



Drosselparameter gemessen oder angegeben:

Größe	Symbol
Nenninduktivität	L_N
Gleichstromwid.	R_0
weitere	C_p, R_p
Kernquerschnitt	A
Kernquerlänge	ℓ_M
Spaltlänge	ℓ_G
Windungszahl	N

Grundmodell aus LTspice (vgl. [LTS17])

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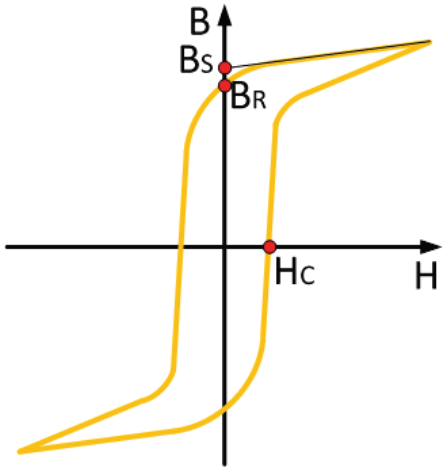
Modellierung

Magnetische Parameter einer Ringkerndrossel



Drosselparameter zu bestimmen:

Größe	Symbol
Sättigungsflußdichte	B_S
Remanenzflußdichte	B_R
Koerzitivfeldstärke	H_C

Modellparameter nach dem Grundmodell aus LTspice [LTS17]

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Anwendung

Ringkerndrossel als Bauelement

Typ: WE 7447010

[WE010]

Größen aus dem Datenblatt:

Größe	Wert
Induktivität:	470 µH ±20 %
Nennstrom:	1,6 A

Gemessene Größen:

Größe	Wert
Gleichstromwid.:	205 mΩ
Kernquerschnitt:	27 mm^2
Kernlänge:	38 mm
Windungszahl:	88

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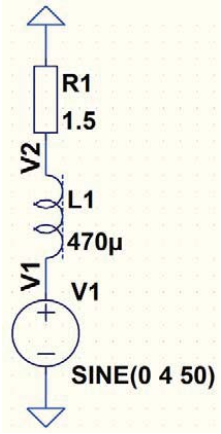
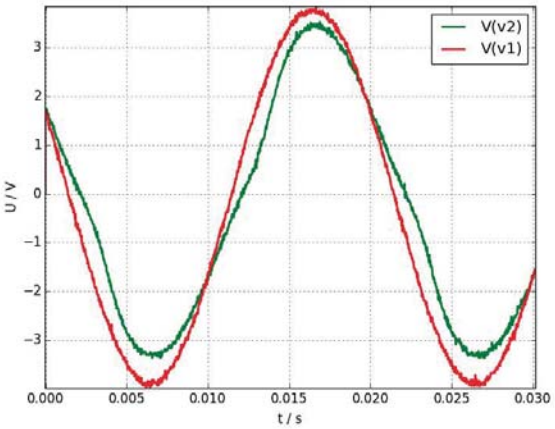
Anwendung

Verlauf des Spannungsabfalls über realem Bauelement





Erkenntnis:

Magnetische Eigenschaften des Drosselkerns verformen Spannungssignal.

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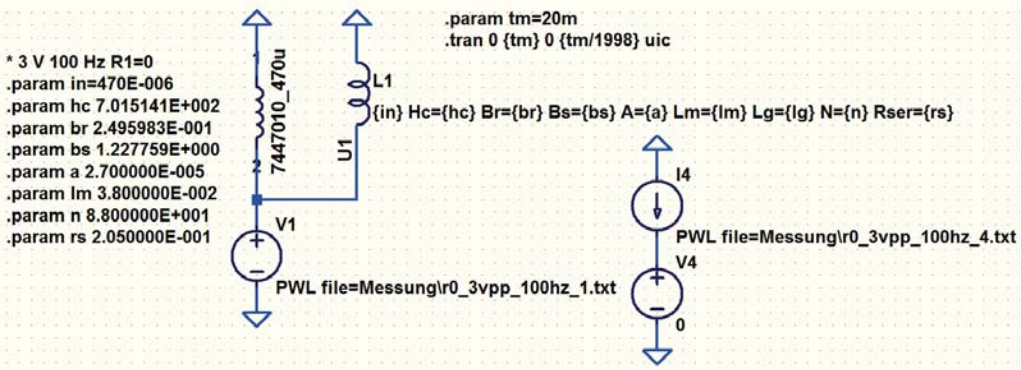
Anwendung

Annähern des Simulationsergebnis' an die Messung



links: Simulation des Stromflusses durch die Spulen

rechts: Einbinden gemessener Signale

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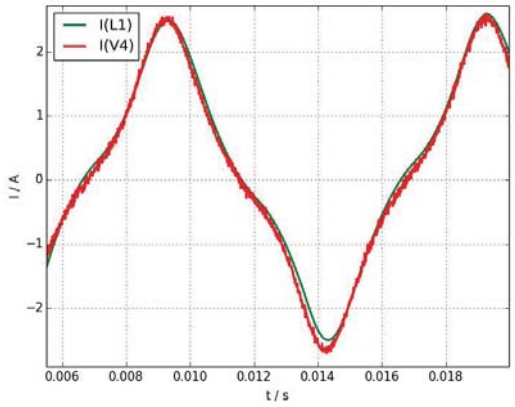
Anwendung

Annähern des Simulationsergebnis' an die Messung



Evolutionär ermittelt (Kombination aus ASCO und LTspice):

Größe	Wert
H_C	701 A/m
B_R	0,25 T
B_S	1,22 T

- Spulenmodell in LTspice ermöglicht Anpassung (hier bei 100 Hz)
- Signalverformung (erhöhter Strom) durch Erreichen der Sättigungsgrenze

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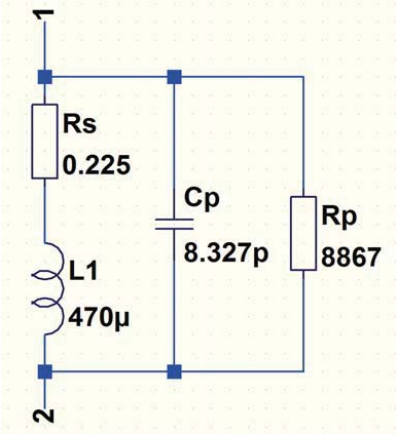
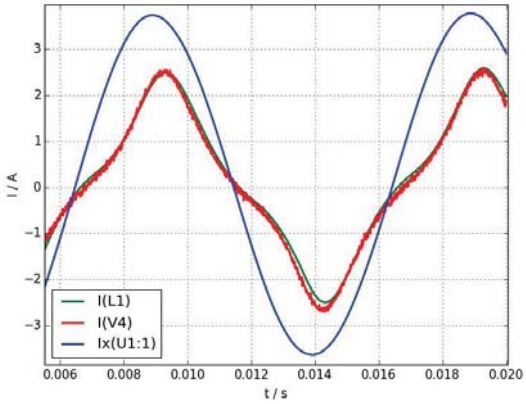
Anwendung

Vergleich mit Herstellermodell



Herstellermodell:



- großzügig
- keine Signalverformung

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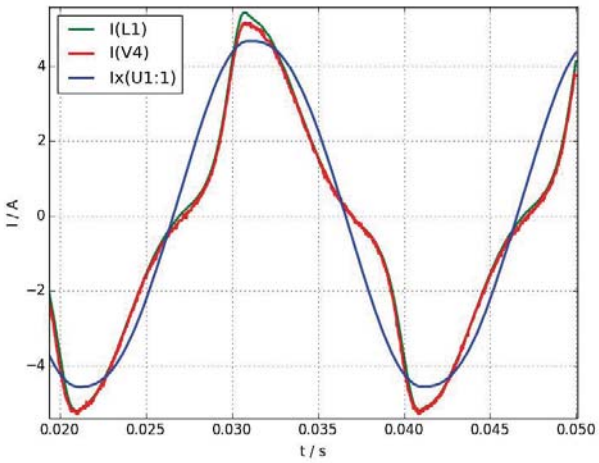
Anwendung

Frequenzänderung mit ermittelten Parametern

- Frequenz: 50 Hz
- Kaum Abweichungen der Stromkurve im optimierten Modell



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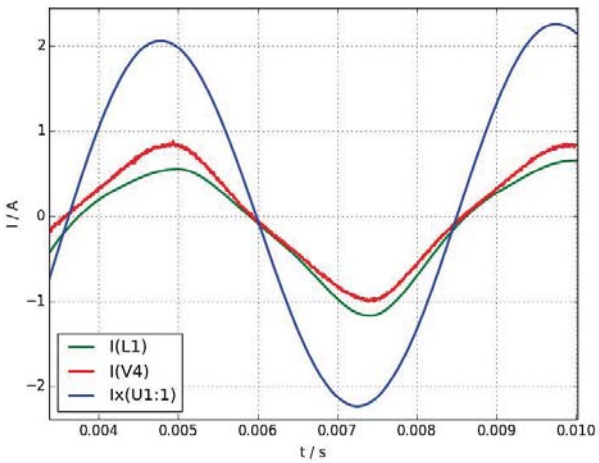
Anwendung

Frequenzänderung mit ermittelten Parametern

- Frequenz: 200 Hz
- Leichte Abweichungen der Stromkurve im optimierten Modell



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Zusammenfassung

Evolutionäre Algorithmen in der Simulation

Probieralgorithmen mit Auslese:

Vorteile:
- Mittel zur rechnergestützten Simulation
- Geeignet in komplexen Systemen
- Behandlung auch unstetiger Verläufe.

Nachteile:
- hoher algorithmischer Aufwand.
- Verwurf von geeigneten Ergebnissen möglich

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Referenzen

João Ramos
ASCO A SPICE Circuit Optimizer
Companion to version 0.4.10

LTspice XVII - Hilfe
1998-2018 Analog Devices Corporation

Datenblatt
WE-FI Leaded Toroidal Line Choke, Ord. No. 7447010
Würth Elektronik eiSos GmbH & Co. KG Waldenburg 2017

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Ende
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Vielen Dank.
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Forschungstechnik
Seite 28/28
Mitglied der Helmholtz-Gemeinschaft
Dr.-Ing. Wolfram Sorge | HZDR - Zentralabteilung Forschungstechnik | http://www.hzdr.de

NIEDERFREQUENTE-MAGNETFELDER AN SCHALTKÄSTEN



Jörg Burmester

Elektronikabteilung TKE

Technische Infrastruktur

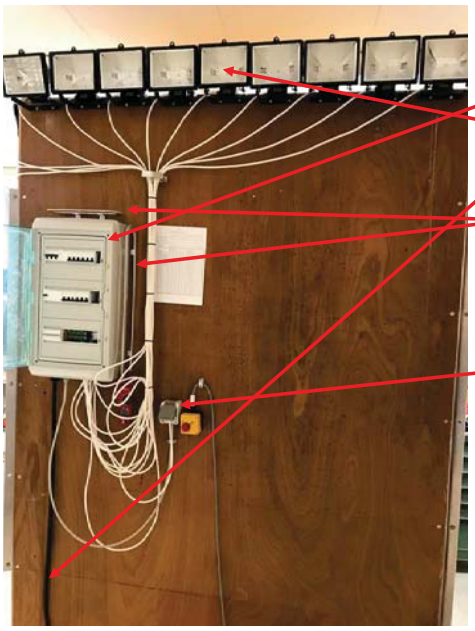
Jülich 8.04.2019

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

AUFBAU

Gleicher Aufbau für 3P+N System und klassischer Verteilung

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung



- Sicherungskasten
- Lasten
- Einspeisung
- Spulen
  - Schaltschranktraverse „Simulation“ vertikal
  - Schaltschranktraverse „Simulation“ horizontal
- Schukosteckdose für Frequenzumformer

AUFBAU KLASSISCH

Sicherungskasten 3P mit getrennter Leiterführung

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

- Einpolige LS-Schalter
- Fliegende Verdrahtung
- N-Schiene getrennt
- PE-Schiene getrennt

TKE 2019

3

AUFBAU KLASSISCH

Sicherungskasten 3P mit getrennter Leiterführung

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

- Zweipolige LS-Schalter
- Verdrillte Leiterführung L+N
- **N dicht bei L**
- PE-Schiene getrennt

TKE 2019

4

INDUZIERTE STRÖME

Schaltschrank Traversen

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Klassisch

2,7 mA

3P+N

0,8 mA

TKE 2019

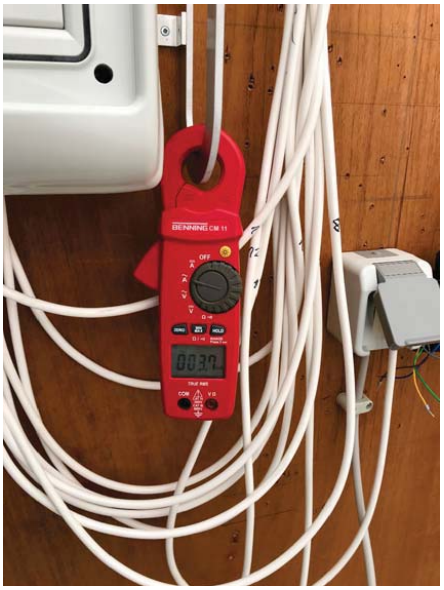
5

INDUZIERTE STRÖME

Schaltschrank Traversen

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Klassisch



3,7 mA

3P+N

1,8 mA

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INDUZIERTE STRÖME

Schaltschrank Traversen

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Klassisch

46,4 mA

3P+N

18,3 mA

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INDUZIERTE STRÖME

Schaltschrank Traversen

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Klassisch

37,9 mA

3P+N

30,2 mA

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INDUZIERTE STRÖME

Schaltschrank Traversen

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Schlecht aufgebaute Niederspannungshauptverteilung

4.48 A

2,46 A

Wo fließen diese Ströme hin?

Diese Störströme müssen vermieden werden!

LEITUNGSGEBUNDENE STÖRUNGEN

Netznachbildung

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Messung der leitungsgebundenen Störungen

- Messung von L1, L2, L3 and N
- Frequenzbereich 150kHz – 30 MHz

150kHz-30MHz

LEITUNGSGEBUNDENE STÖRUNGEN

Messung an L1

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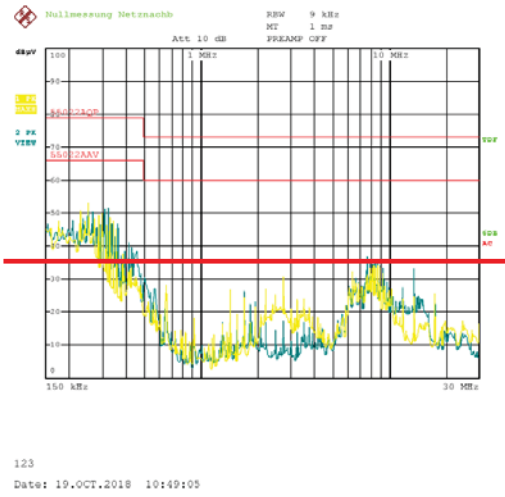
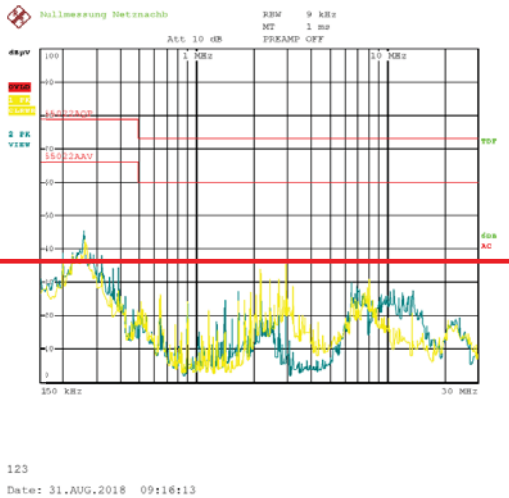
Zentrum für Material- und Küstenforschung

Klassisch



3P+N



150kHz-30MHz

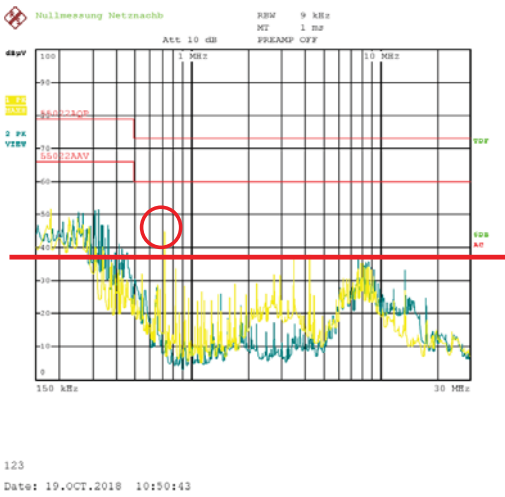
- Grün: Nullmessung
- Gelb: Alle Verbraucher eingeschaltet

LEITUNGSGEBUNDENE STÖRUNGEN

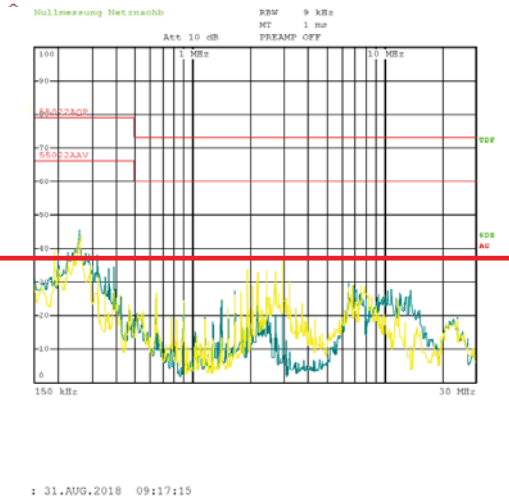
Messung an L2

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Klassisch



3P+N



150kHz-30MHz

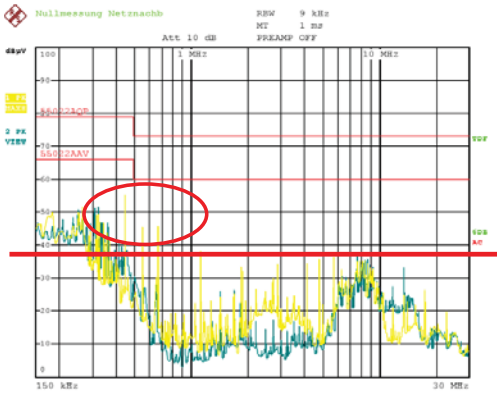
- Grün: Nullmessung
- Gelb: Alle Verbraucher eingeschaltet

LEITUNGSGEBUNDENE STÖRUNGEN

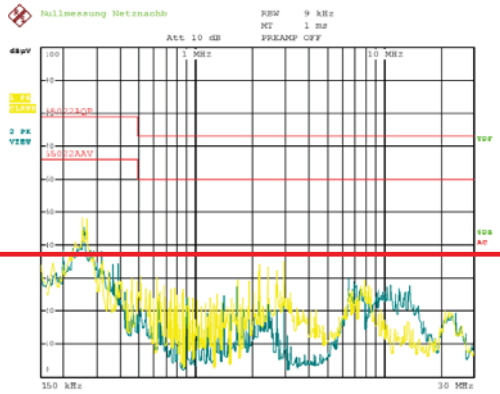
Messung an L3

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Klassisch



3P+N



150kHz-30MHz

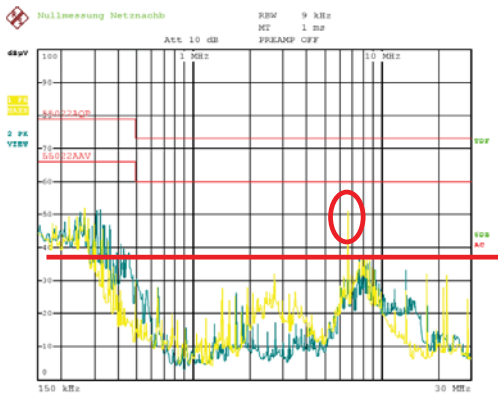
- Grün: Nullmessung
- Gelb: Alle Verbraucher eingeschaltet

LEITUNGSGEBUNDENE STÖRUNGEN

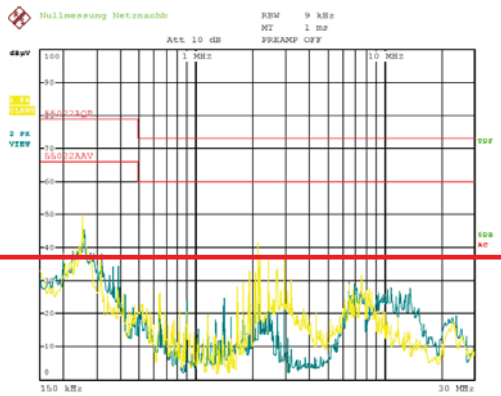
Messung an N

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Klassisch



3P+N



150kHz-30MHz

- Grün: Nullmessung
- Gelb: Alle Verbraucher eingeschaltet

MAGNETFELDMESSUNG

Messequipment

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Aaronia Spectran NF5035

0Hz-30MHz

- Grün: Nullmessung
- Gelb: Alle Verbraucher eingeschaltet

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MAGNETFELD ÜBER ZULEITUNG

Alle Verbraucher eingeschaltet

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Frequenzbereich 50-2000Hz

klassische: 9000nT Startwert

hohe Oberwellen

3P+N: 3750nT Startwert

niedrige Oberwellen

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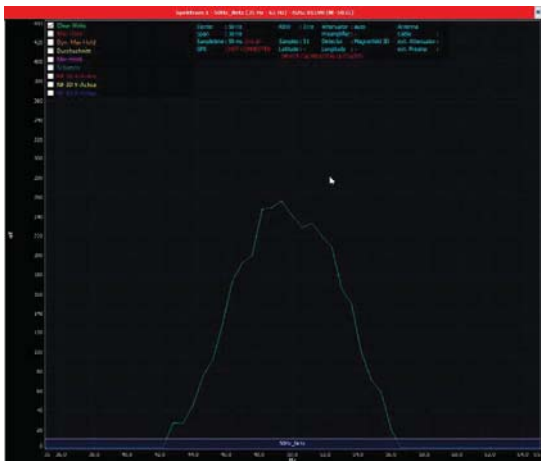
MAGNETFELD NACH HAUPTSCHALTER

Alle Verbraucher eingeschaltet

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Frequenzbereich 35-65Hz



klassische260nT Maximum

3P+N: 130nT Maximum

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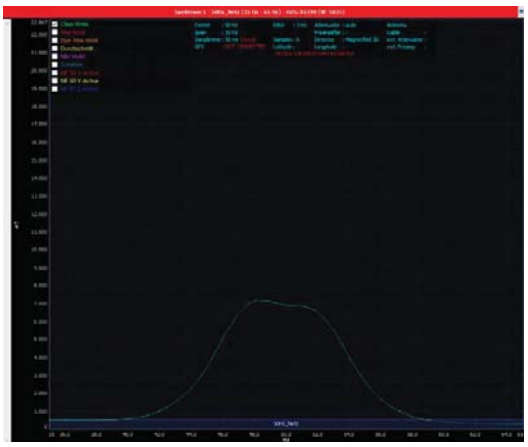
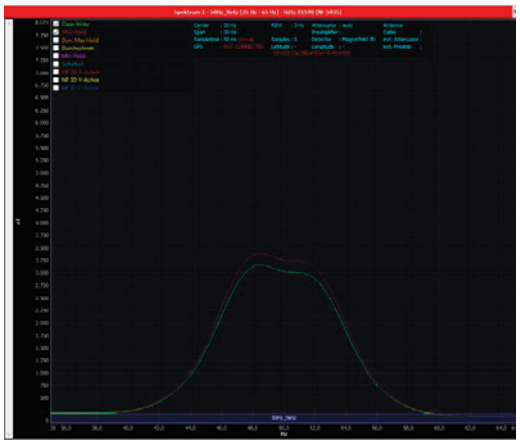
MAGNETFELD NACH RCD1

Alle Verbraucher eingeschaltet

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Frequenzbereich 35-65Hz





klassisch 7000nT Maximum

3P+N: 3250nT Maximum

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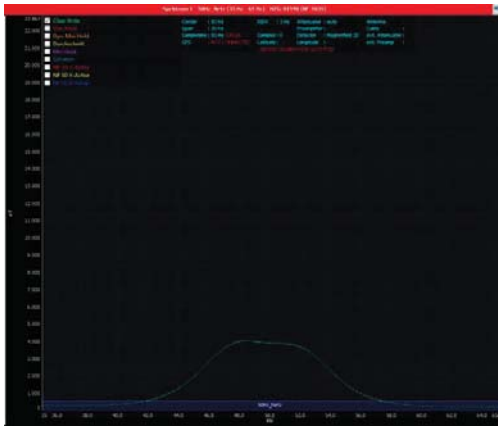
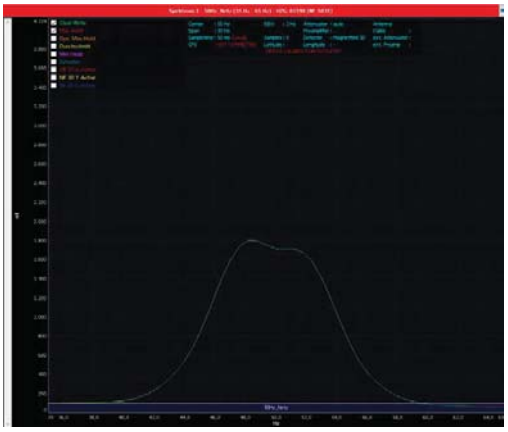
MAGNETFELD NACH LAST 1

Alle Verbraucher eingeschaltet

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Frequenzbereich 35-65Hz





klassisch 4000nT Maximum

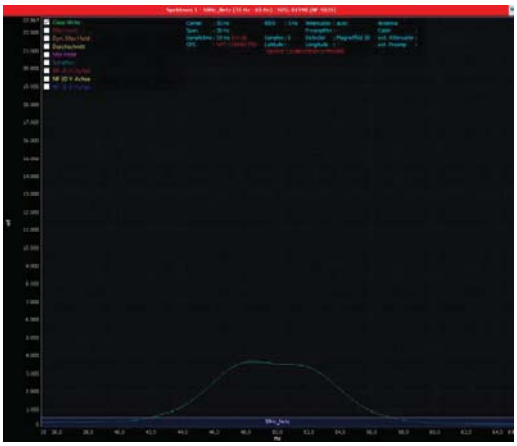
3P+N: 1800nT Maximum

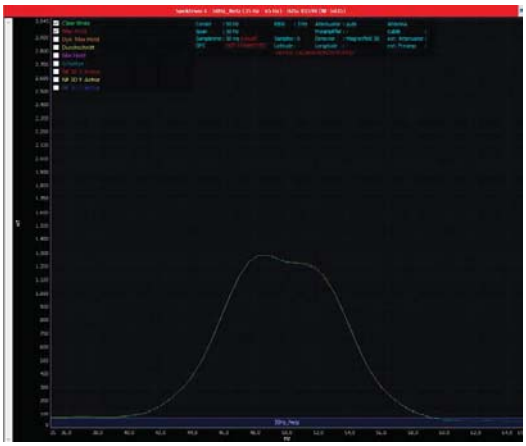
MAGNETFELD NACH LAST 2

Alle Verbraucher eingeschaltet

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Frequenzbereich 35-65Hz





klassisch 3700nT Maximum

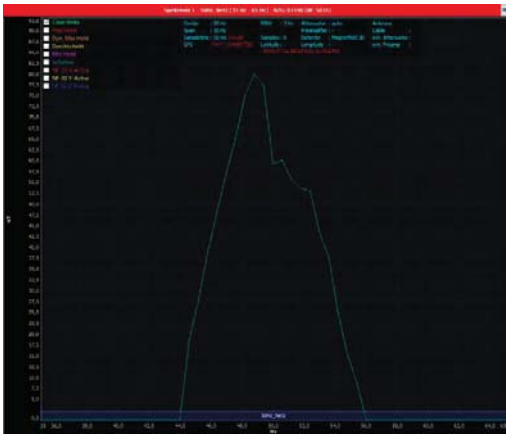
3P+N: 1280nT Maximum

MAGNETFELD RECHTS ABSTAND 0,5M

Alle Verbraucher eingeschaltet

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Frequenzbereich 35-65Hz



klassisch 80nT Maximum

3P+N: 35nT Maximum

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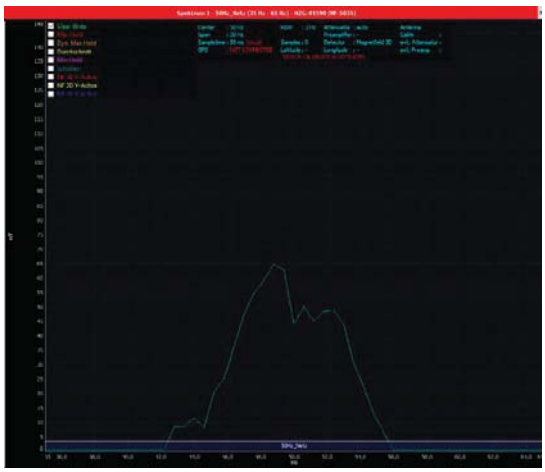
MAGNETFELD LINKS ABSTAND 0,5M

Alle Verbraucher eingeschaltet

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Frequenzbereich 35-65Hz



klassisch 65nT Maximum

3P+N: 30nT Maximum

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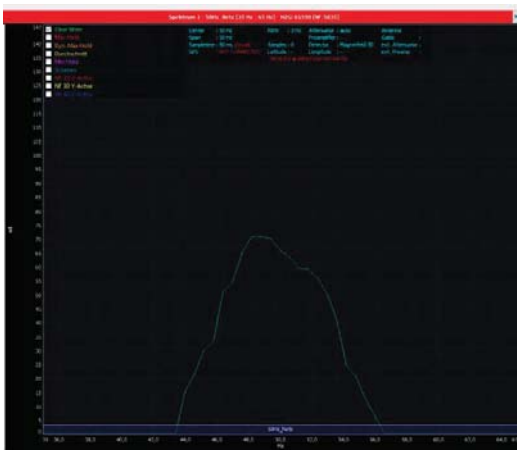
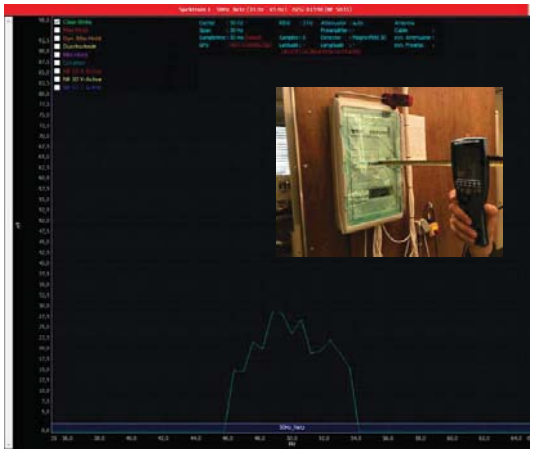
MAGNETFELD VORNE ABSTAND 1M

Alle Verbraucher eingeschaltet

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

Frequenzbereich 35-65Hz





klassisch 70nT Maximum

3P+N: 27nT Maximum

VERSCHIEDENE LASTEN

Messung über Sicherung

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

klassisch

Last: FU

402,9µT

Last: Lampe

5,53µT

3P+N

Last: FU

285,8µT

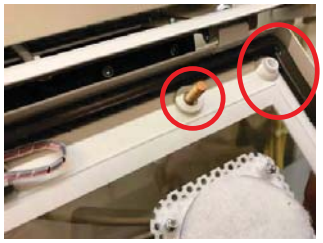
Last: Lampe

2,891µT

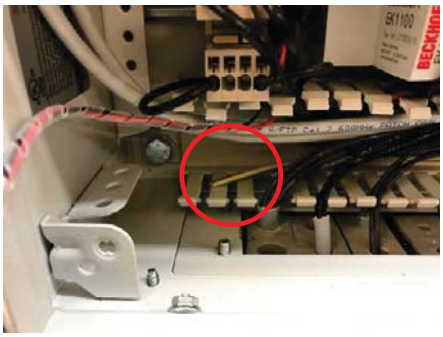
SCHALTSCHRANKAUFBAU

Fehler die gemacht werden (warum auch immer)

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung



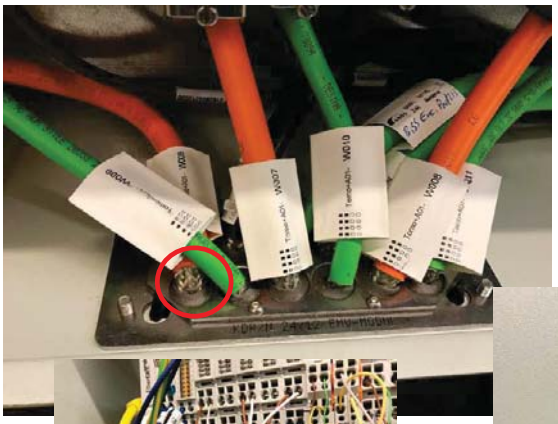
- Kein EMV-Schaltschrank
- Fenster nicht in EMV-Ausführung
- Keine EMV-Durchführungen
- Schirm nicht angeschlossen
- Erdungsschrauben nicht benutzt
- PE nicht angschlossen

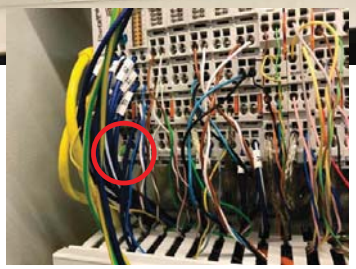


SCHALTSCHRANKAUFBAU

Es geht auch anders und vorbildlich

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung





- EMV-Schaltschrank
- kein Fenster
- EMV-Durchführungen
- Schirm angeschlossen
- Erdungsschrauben benutzt
- PE angeschlossen

LEITERFÜHRUNG

L und N sehr dicht beieinander

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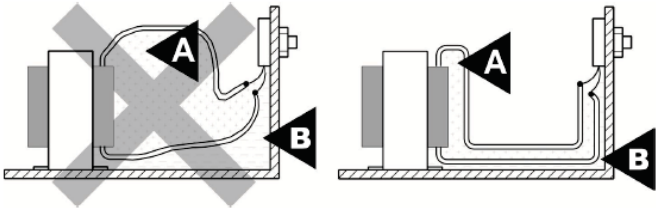
3P+N Stromschiene

3P+N Vertikale Phasenschiene



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NETZFILTER

Netzrückwirkung

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Zentrum für Material- und Küstenforschung

Richtige Montage

- Flächiger Kontakt zum Gehäuse
- Kurze geschirmte Zuleitung
- Schirm mit Filtergehäuse verbunden, flächig
- Richtigen Filter wählen
- Nach N filtern
- PE sauber halten

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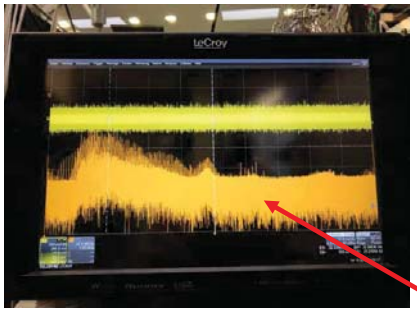
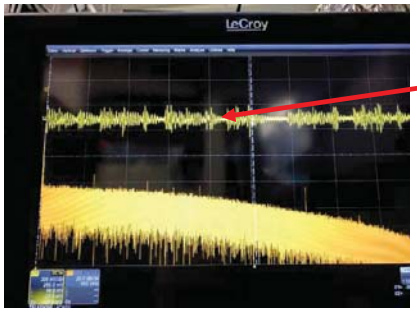
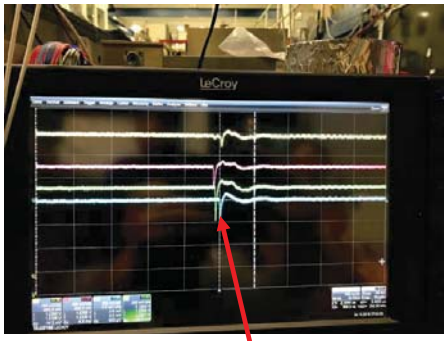
SENSITIVE MESSELEKTRONIK

Störungen

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung







- Störungen
- So sollte es eigentlich aussehen
- Störquelle und –senke dicht zusammen

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INFOS

EMV

Helmholtz-Zentrum Geesthacht
Zentrum für Material- und Küstenforschung

- DEMVT https://www.demvt.de
- Sachverständige https://www.sv-otto.de/
- Diverse Leitfäden im Netz (Firmen)
- VDE
- emv_pocket_guide
  ZVEI Zentr

Störquellen schon im Ansatz eleminieren

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KONSEQUENTER EMV GERECHTER AUFBAU

Störungen werden erheblich minimiert

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Wichtig:

- Störungen minimieren
  - L+N dicht beieinander führen
  - Verdrillen (Magnetfelder kompensieren sich)
  - Konsequent und richtig schirmen
  - EMV-Schränke verwenden
  - PE-anschließen
  - Erdschleifen vermeiden
  - …

Vielen Dank für ihre Aufmerksamkeit

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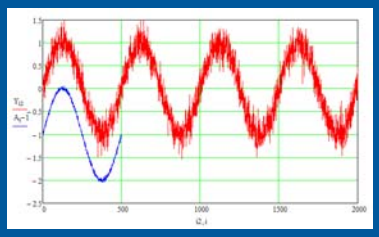
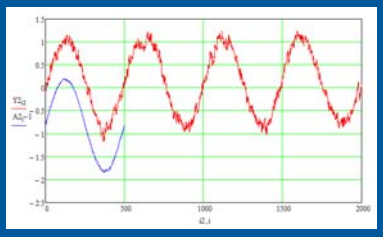
Averaging: Was hilft‘s?





HZDR
HELMHOLTZ ZENTRUM DRESDEN ROSSENDORF

Averaging: Was hilft’s?

Häufiges Problem: die Signale sind verrauscht bzw. die Meßwerte „zappeln“
Schnelle Lösung, die jedem sofort einfällt: „Wir müssen mitteln“

Annahme:
Noise ~ $\frac{1}{\sqrt{N}}$ bzw. SNR ~ $\sqrt{N}$ mit der Anzahl N der Meßwerte;

Was sind die Voraussetzungen?
- Das Rauschen ist zufällig, so dass sein arithmetisches Mittel im betrachteten Frequenzbereich Null ist (weißes Rauschen).

Für Wechselsignale gilt noch:
- Signal und Rauschen sind unkorreliert
- Das Nutzsignal wiederholt sich und läßt sich zeitlich synchronisieren

DRESDEN concept HZDR

Gerade bei langen Meßzeiten bzw. tiefen Frequenzen ist die erste Voraussetzung, ein gleichmäßiges Störspektrum, oft nicht erfüllt. Bei tiefen Frequenzen ist ein 1/f-Rauschspektrum häufig anzutreffen.

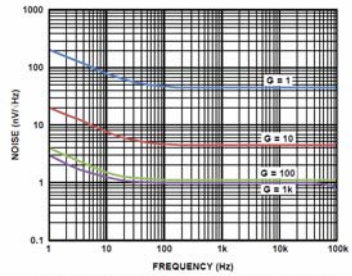


Figure 26. RTI Voltage Noise Spectral Density vs. Frequency

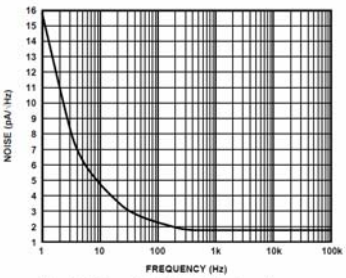


Figure 28. Current Noise Spectral Density vs. Frequency

Rauschspektren vom Instrumentationsverstärker AD8429

$$U = \sqrt{4 \bullet k_b \bullet T \bullet B \bullet R}$$ Thermische Leerlauf-Rauschspannung

weniger bekannt: NI als Noise Index für zusätzliches 1/f-Rauschen

- ist abhängig von der am Widerstand angelegten Gleichspannung U
- ist definiert in dB pro µV Rauschspannung über eine Frequenzdekade pro Volt Gleichspannung
- gute Werte liegen bei < -30 dB

$$\int_{f_1}^{10 \bullet f_1} \frac{C}{f}\, df = C \bullet \ln(10)$$ ist unabhängig von der absoluten Frequenz f_1

$$NI_L = 10^{\frac{NI}{20 \bullet dB}} \bullet \frac{\mu V}{V}$$ linearer Rauschindex

daraus ergeben sich folgende Formeln:

$$P_I = \int \frac{K_I}{f} \bullet P_{DC}\, df$$

Rauschleistung vom 1/f-Rauschen mit

$$K_I = \frac{NI_L{}^2}{\ln(10)} \qquad P_{DC} = \frac{U^2}{R}$$

$$u_N = \sqrt{4 \bullet k_b \bullet T \bullet R \bullet \left(f_2 - f_1\right) + K_I \bullet U^2 \bullet \ln\left(\frac{f_2}{f_1}\right)}$$

gesamte Leerlauf-Rauschspannung

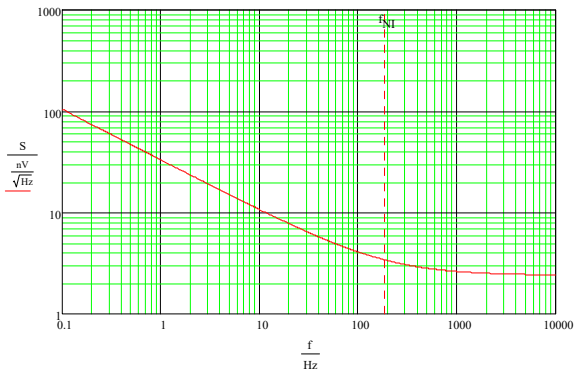
$$f_{NI} = \frac{K_I \bullet P_{DC}}{4 \bullet k_b \bullet T}$$

3 dB-Frequenz vom 1/f-Rauschen

$$u_N = \sqrt{4 \bullet k_b \bullet T \bullet R \bullet \int_{f_1}^{f_2} 1 + \frac{f_{NI}}{f}\, df}$$

gesamte Leerlauf-Rauschspannung

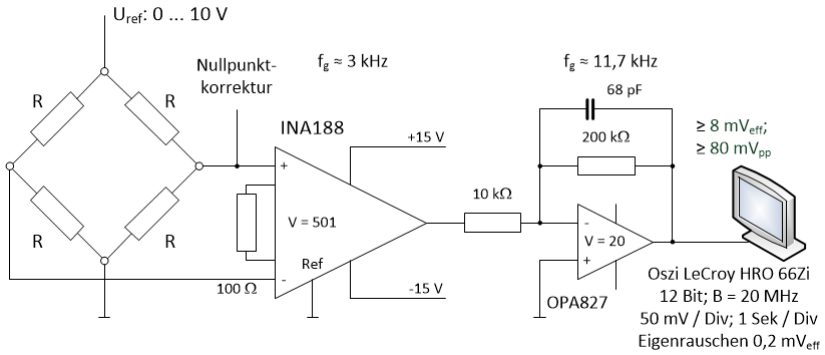
Rauschspannungsspektrum: $S(f) = \sqrt{4 \bullet k_b \bullet T \bullet R \bullet \left(1 + \frac{f_{NI}}{f}\right)}$



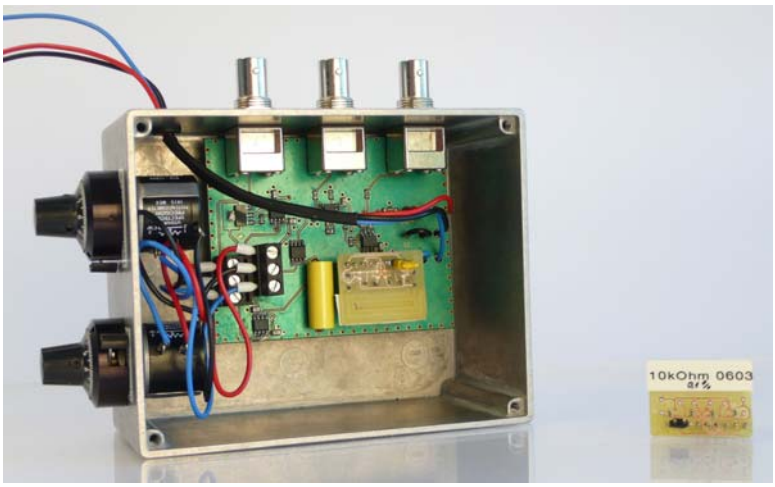
Beispiel für
NI = -40 dB;
U = 5 V und
R = 350 Ω

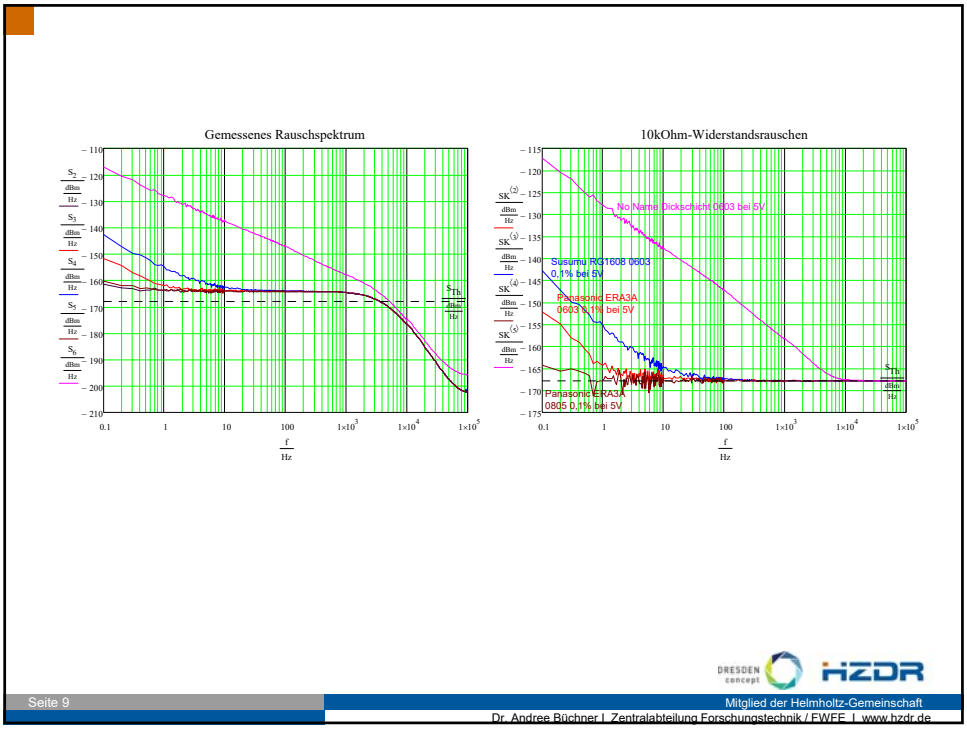
$f << f_{NI}$: $S(f) = U \bullet \sqrt{\frac{K_I}{f}}$ unabhängig vom Widerstand!

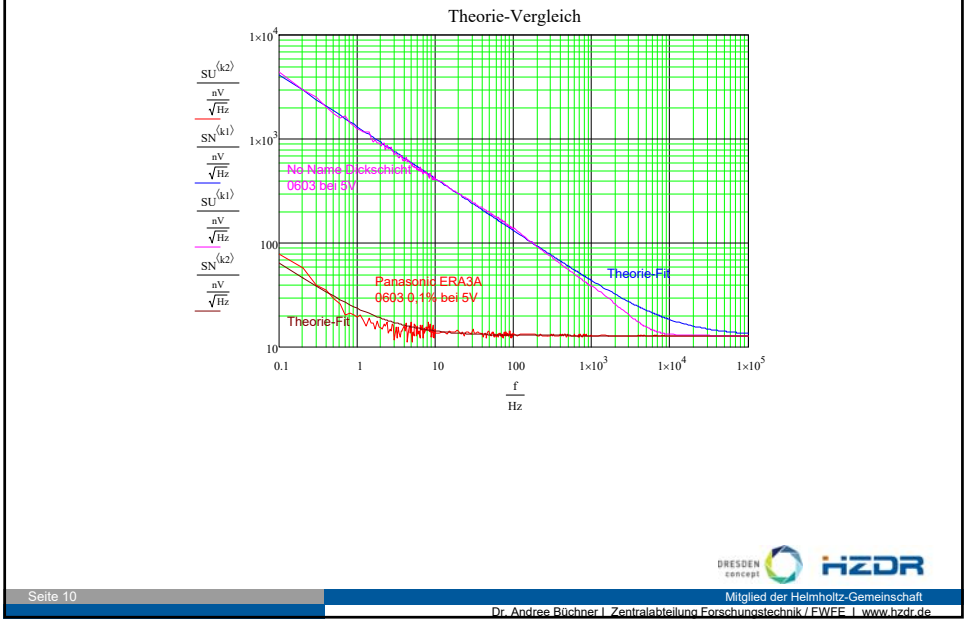
Meßschaltung für Widerstandsrauschen



- jeweils 200 Messungen mit 200 kSPS für 10 Sekunden
- danach Auswertung am PC (FFT und Averaging der Spektren)
- Subtraktion des Spektrums für U_{ref} = 0 V




Gemessenes Rauschspektrum
10kOhm-Widerstandsrauschen
No Name Dickschicht 0603 bei 5V
Susumu RG1608 0603 0,1% bei 5V
Panasonic ERA3A 0603 0,1% bei 5V
Panasonic ERA3A 0805 0,1% bei 5V
f / Hz


Theorie-Vergleich
No Name Dickschicht 0603 bei 5V
Panasonic ERA3A 0603 0,1% bei 5V
Theorie-Fit
Theorie-Fit
f / Hz

Serie	Widerstand	Spannung	P	f_{NI}	NI_L	NI
	[kΩ]	[V]	[mW]	[Hz]	[µV/V]	[dB]
Panasonic ERA3A 0603 0,1%	10	5	2,5	2,34	5,98E-03	-44,5
Susumu RG1608 0603 0,1%	10	5	2,5	18,53	1,68E-02	-35,5
Panasonic ERA3A 0805 0,1%	10	5	2,5	0,13	1,40E-03	-57,0
No Name Dickschicht 0603	10	5	2,5	10400	4,00E-01	-8,0
No Name Dickschicht 0603	10	0,5	0,025	98,82	3,90E-01	-8,2
Panasonic ERA3A 0603 0,1%	350	5	0,071	0,21	1,06E-02	-39,5
Panasonic ERA3A 0603 0,1%	0,2 + 0,15	5	71,4	6,72	1,90E-03	-54,4
Vishay SMR1D	0,35	5	71,4	--	--	--

Vishay SMR1D:
„High Precision Bulk Metal® Foil Molded Surface Mount Resistor“

- Temperature coefficient of resistance (TCR):
  ± 2 ppm°C typical (- 55 °C to + 125 °C, + 25 °C ref.)
- Tolerance: to ± 0.01 %
- Current noise: - 40 dB
- Voltage coefficient: < 0.1 ppm/V
- Load life stability: ± 0.005 % (70 °C, 2000 h at rated power)
- Power rating: to 600 mW at 70 °C

Achtung!

Der Einfluß der Temperatur ist erheblich und ist de facto nicht vom 1/f-Rauschen zu unterscheiden!
Bei konstantem Strom gilt $\Delta U = U_{DC} * \Delta\delta * TK$
Bsp.: U_{DC} = 5 V; $\Delta\delta$ = 0,1°C; TK = 2 ppm/K ➔ ΔU = 1 µV

Alle rauscharmen Widerstände haben auch einen kleinen TK!

Das Spektrum vom Temperaturverlauf soll auch eine 1/f-Form haben:
“A typical non controlled thermal environment (eg. a laboratory) may have the following temperature characteristics (taken from real data):

0.2K/√Hz at 10^{-3}Hz
0.07K/√Hz at 10^{-2}Hz
0.01K/√Hz at 10^{-1}Hz”

Averaging im Zeitbereich über T:

Frequenzgang $G(f) = \frac{\sin(\pi \bullet f \bullet T)}{\pi \bullet f \bullet T}$ mit $T = \frac{1}{f_1}$

$$\int_{f_1}^{f_2} \frac{1}{f} \bullet \left(\frac{\sin\left(\pi \bullet \frac{f}{f_1}\right)}{\pi \bullet \frac{f}{f_1}} \right)^2 df$$

Integral über 1/f und Averaging-Frequenzgang ist konstant - unabhängig von den Integrationsgrenzen f_1 und f_2!

$$\int_{f_1}^{f_2} \frac{\cos\left(2 \bullet \pi \bullet \frac{f}{f_1}\right)}{f} df$$

Vereinfachung für f_2 als ganzzahliges Vielfaches von f_1

Reales System mit weißem und 1/f-Rauschen

$$P_N(T) = \int_{\frac{1}{T}}^{f_2} \left(1 + \frac{f_N}{f}\right) df$$

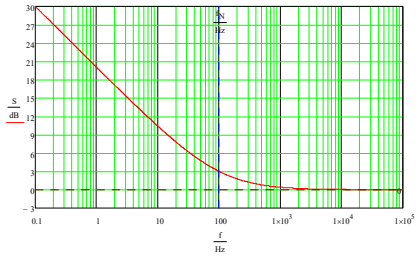
Rauschleistung ohne Averaging

$$P_{NA}(T) = \int_{\frac{1}{T}}^{f_2} \left(1 + \frac{f_N}{f}\right) \bullet \left(\frac{\sin(\pi \bullet f \bullet T)}{\pi \bullet f \bullet T}\right)^2 df$$

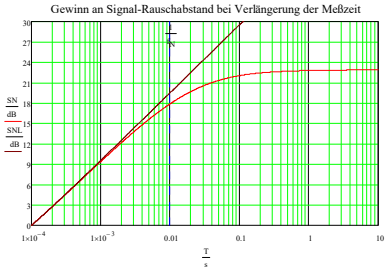
Rauschleistung mit Averaging

Beispielrechnungen für f_N = 100 Hz

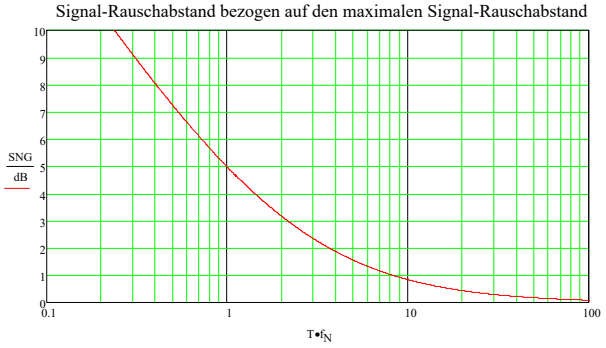
Rauschleistungsspektrum



Gewinn an Signal-Rauschabstand bei Verlängerung der Meßzeit



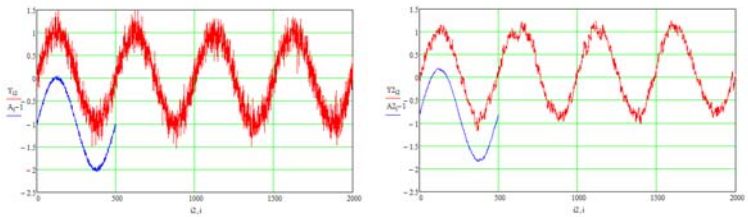
Signal-Rauschabstand bezogen auf den maximalen Signal-Rauschabstand



SN [dB]	10	9	8	7	6	5	4	3	2	1
T * f_N	0,24	0,31	0,40	0,53	0,72	0,99	1,42	2,15	3,67	8,22

Es macht wenig Sinn, länger als $5/f_N$ zu messen und zu mitteln!

Simulation: 64fache Mittelung



Weißes, gaußsches Rauschen 1/f-Rauschen

jeweils 5.000.000 Ausgangswerte, Mittelwert 0, Standardabweichung 0,2

Fehler vom gemittelten Signal gegenüber dem unverrauschten Signal:

RMS-Fehler:	0,026	0,120
AC-Fehler:	0,026	0,015
DC-Fehler:	$1{,}22*10^{-3}$	0,119

Rauschärmste Instrumentationsverstärker für tiefe Frequenzen (0,01 … 1 Hz)

(berechnet nach Datenblattwerten)

v = 501

R = 100 kΩ:	INA188	F = 3,61 dB	Parallelschaltung bringt nichts
R = 10 kΩ:	INA188	F = 3,35 dB	2*INA188: F = 2,47 dB
			3*INA188: F = 2,32 dB
R = 1 kΩ:	INA188	F = 10,59 dB	2*INA188: F = 7,95 dB
			3*INA188: F = 6,54 dB
			4*INA188: F = 5,63 dB
R = 100 Ω:	AD8429	F = 16,10 dB	2*AD8429: F = 14,99 dB

0,01 Hz … 10 Hz:

R = 100 kΩ:	AMP01	F = 1,35 dB	Parallelschaltung bringt nichts
R = 10 kΩ:	INA828	F = 1,88 dB	3*INA828: F = 1,27 dB
R = 1 kΩ:	AD8421	F = 5,01 dB	3*AD8421: F = 2,59 dB
			4*AD8421: F = 2,23 dB
R = 100 Ω:	AD8429	F = 8,69 dB	2*AD8429: F = 7,64 dB

Literatur:
„Signal- und Rauschanalyse mit Quellenverschiebung“; Zwick,A. et al.
ISBN 978 -3-642-54036-3

„Resistor Current Noise Measurements“; Seifert, F.
https://dcc.ligo.org/LIGO-T0900200/public

„Op-Amp Noise Test Results“; Hoyland, D.
https://dcc.ligo.org/LIGO-T1600206/public

IS 1/f NOISE INFINITE AT DC?

$$V_n = \sqrt{K \ln \frac{f_H}{f_L}}$$

$$V_{nA}\ (0.1\text{Hz to } 10\text{Hz}) = \sqrt{K \ln \frac{10}{0.1}}$$

$$V_{nB}\ (10^{-18}\text{Hz to } 10\text{Hz}) = \sqrt{K \ln \frac{10}{10^{-18}}}$$

$$\frac{1}{\text{Age Of The Universe}}\Bigg\} \quad \frac{V_{nB}}{V_{nA}} = \frac{\sqrt{K \ln 10^{19}}}{\sqrt{K \ln 10^{2}}} = 3.08!!$$

∴If you wait forever, the noise is only 3 times more.

MAXIM

What does “1/f” say about noise at very low frequencies, like DC? Does noise reach infinity as f approaches 0? Not quite, as the equations for V_n show. The ratio between noise in a 0.1Hz to 10Hz band and a 10^{-18}Hz to 10Hz band is compared. 10^{-18}Hz is chosen as the reciprocal of the age of the universe, i.e. 1/forever. As can be seen the noise in the “forever” band is only 3.08 times large, and is not infinite.

Kniel macht den Unterschied

KNIEL

Stromversorgungen

Netzteile mit integrierter Intelligenz

Firmenvorstellung

KNIEL

Seit 44 Jahren Kniel

- Wo kommen wir her?
- Was können wir?
- Wer sind unsere Kunden ?

Kniel Vorteile

- Garantie
- Ausfallrate
- EMV
- Kundenspezifisch
- Nah am Kunden
- …

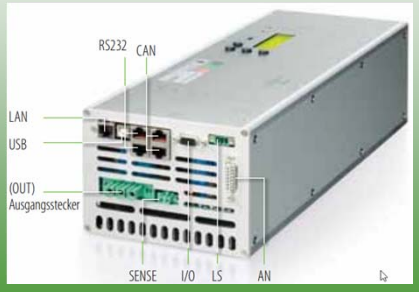
Custom solutions

Produktspektrum

- Schaltungstopologien
- Festspannung
- Programmierbar Analog/Digital
- Montagearten

- Kundenspezifisch

Energy Digital

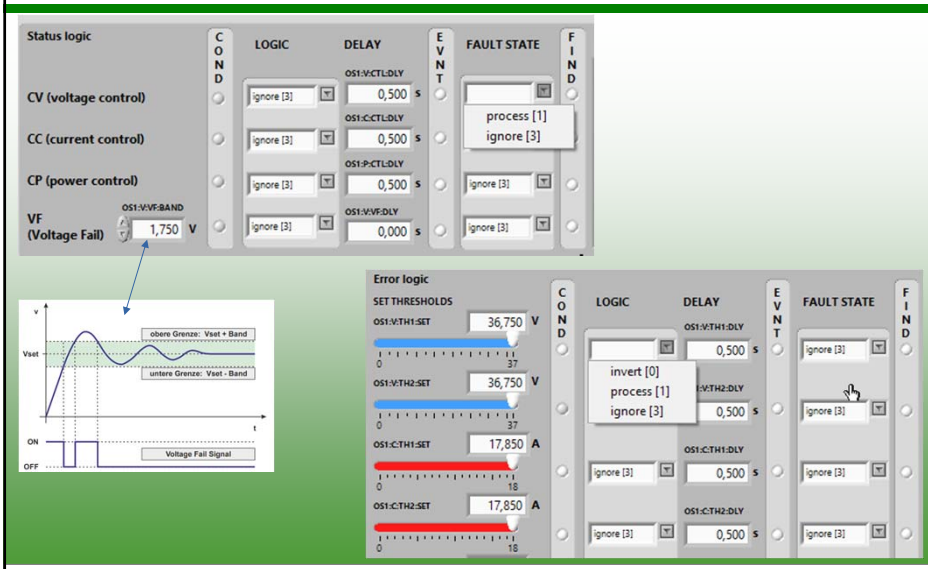


ENERGY DIGITAL Serien

- Standard / Fast
- Leistungsbereich
- Montage
- Potentialtrennung
- Schnittstellen
- Soft-/ Hardwaretrigger
- Redundante Abschaltung

Control

Statuses & Error



50 Memory banks on board

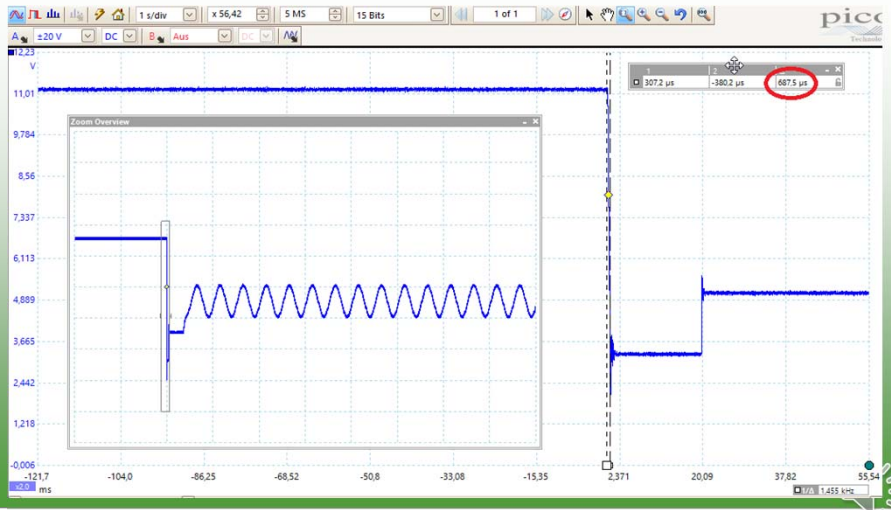
SB	SV	SC	SP	OS1:V:MIN	OS1:V:MAX	OS1:C:MIN	OS1:C:MAX	OS1:P:MIN	OS1:P:MAX	OS1:V:SLB:INCR	OS1:V:SLB:DECR	OS1:C:SLB:INCR	OS1:C:SLB:DECR
0	35.000	17.000	19.965	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
1	0.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
2	0.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
3	0.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
4	0.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
5	0.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
6	0.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
7	0.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
8	0.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
9	0.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
10	0.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
11	6.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
12	10.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000
13	15.000	17.000	408.000	0.000	35.000	0.000	17.000	0.000	408.000	0.000	0.000	0.000	0.000

Prüfzyklen via Sequenzen

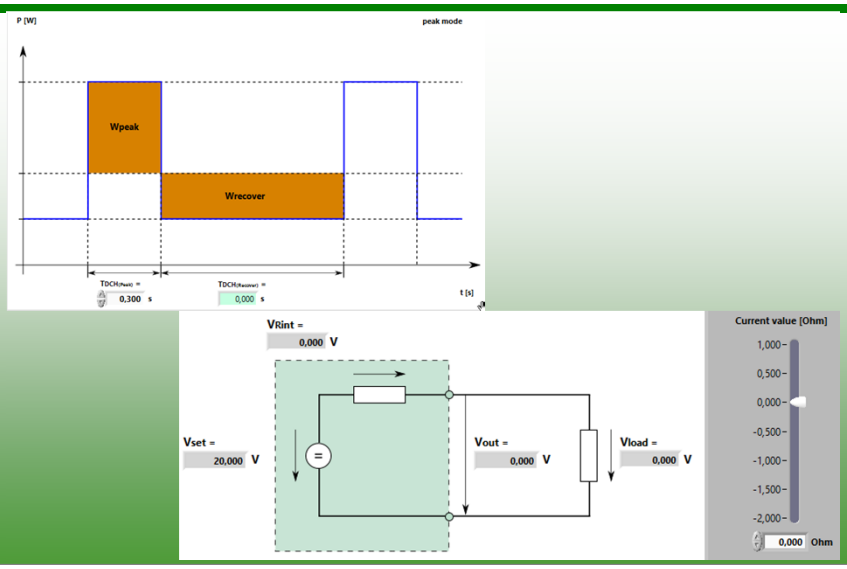
- **Zeit oder Ereigniss-gesteuert**
- Min. Stepzeit 1 msec
- Bis zu 100 Steps

Fast Versionen

- 0 auf Max und Max auf ~0 in < 1 msec



Aktive Last und Sensleitung



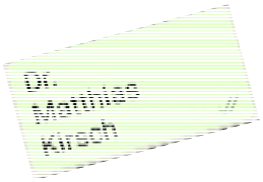
C. Vief Kniel System-Electronic GmbH - Kurzheckweg 8 - 76187 Karlsruhe www.kniel.de

Kniel macht den Unterschied

Stromversorgungen

Netzteile mit integrierter Intelligenz

MTCA and MTCA.4 Developments for Large Scale European Accelerators



Outline

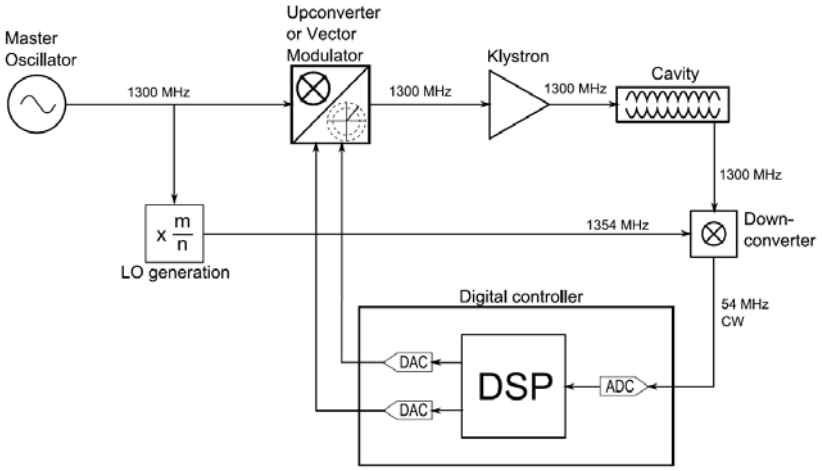
XFEL
- SIS8300-L2/DWC8300 LLRF

ESS
- SIS8300-KU/DWCx LLRF and BPM
  AXI based Firmware Framework

FAIR
- SIS8800/SIS8980 Scaler/Discriminator LASSIE
- SIS8864 Digital I/O AMC Generic
- SIS8300-KU/DS8VM1 UNILAC LLRF (CERN SPS)
- SIS8160/SFMC01 FMC Carrier/Digitizer FMC FCT

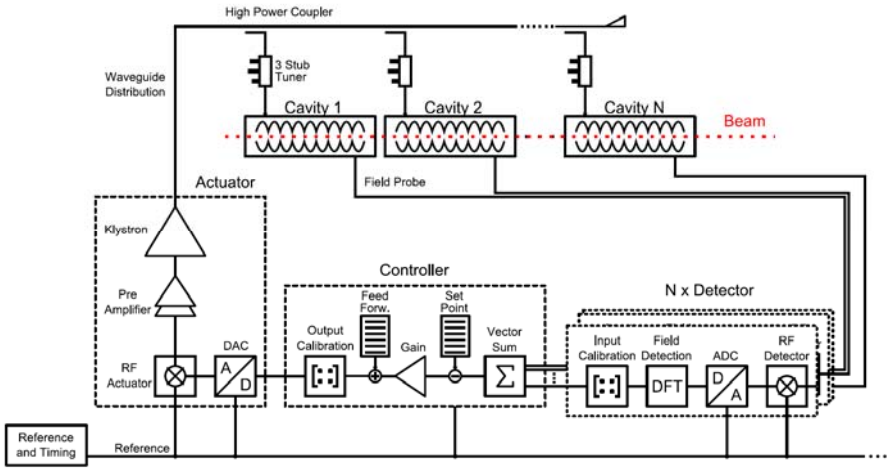
→ Worldwide MTCA community

LLRF (Low Level Radio Frequency) IF Sampling Scheme

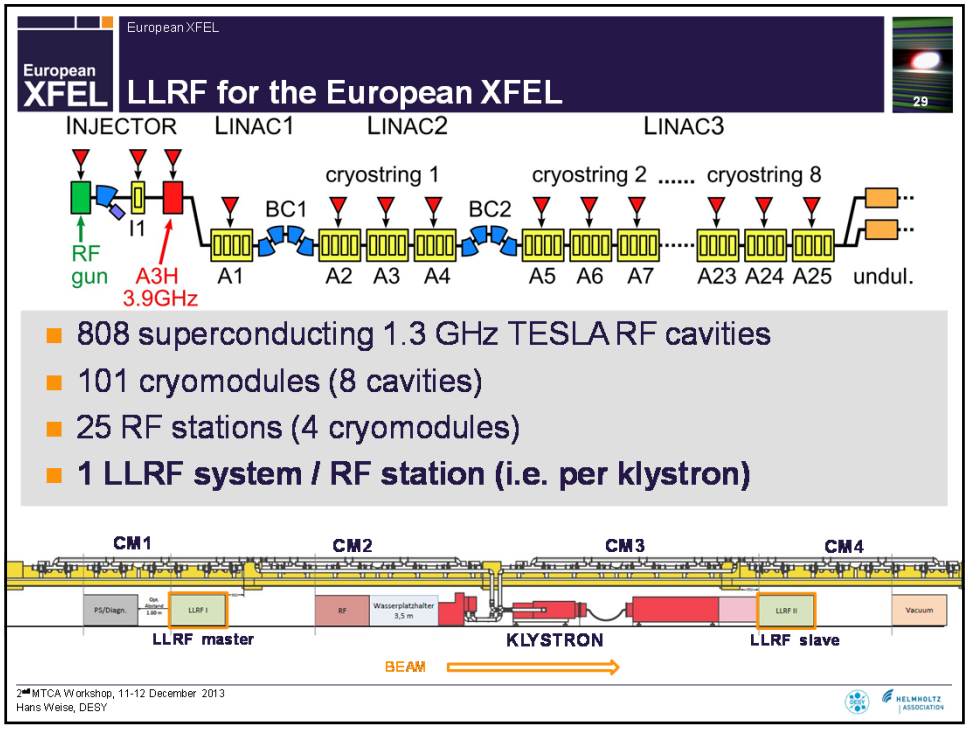


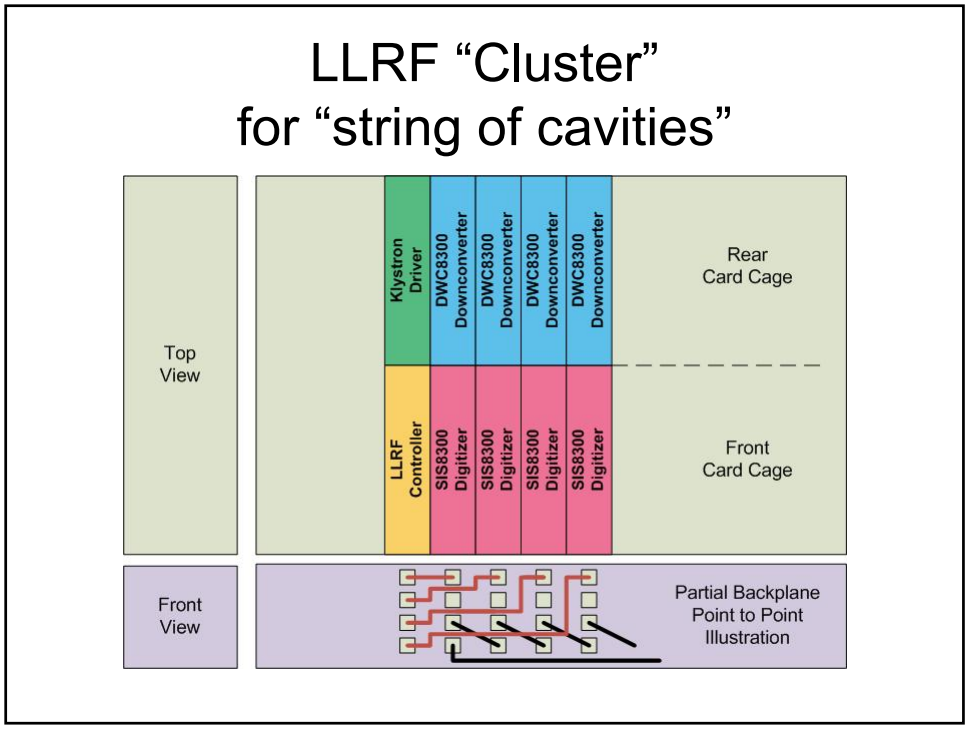
from thesis Karol Suchecki

Multi Cavity Vector Sum based LLRF Control Loop



from thesis Karol Suchecki


European XFEL
LLRF for the European XFEL
29
INJECTOR
LINAC1
LINAC2
LINAC3
cryostring 1
cryostring 2 ..... cryostring 8
RF gun
I1
A3H 3.9GHz
BC1
BC2
A1
A2 A3 A4
A5 A6 A7
A23 A24 A25
undul.
808 superconducting 1.3 GHz TESLA RF cavities
101 cryomodules (8 cavities)
25 RF stations (4 cryomodules)
1 LLRF system / RF station (i.e. per klystron)
CM1
CM2
CM3
CM4
LLRF master
KLYSTRON
LLRF slave
BEAM
2nd MTCA Workshop, 11-12 December 2013
Hans Weise, DESY


LLRF "Cluster"
for "string of cavities"
Top View
Front View
Klystron Driver
DWC8300 Downconverter
LLRF Controller
SIS8300 Digitizer
Rear Card Cage
Front Card Cage
Partial Backplane Point to Point Illustration

SIS8300-L/L2

SIS8300-L2 Digitizer Properties

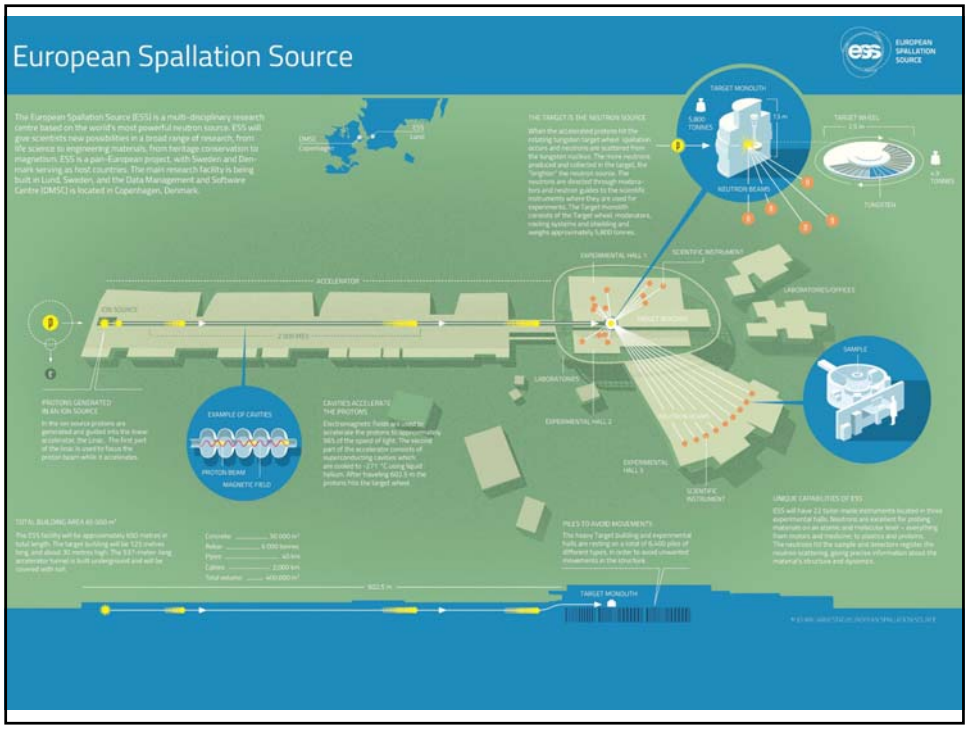
- MTCA.4
- 4 lane PCI Express
- 10 channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s per channel
- AC and DC input stage
- two 250 MS/s 16-bit DACs for fast feedback implementation
- high precision, flexible clock distribution logic
- Internal, front panel, RTM and backplane clock sources
- Programmable delay of twin ADC groups
- Gigabit Link Port implementation to backplane
- Double SFP cage for high speed system interconnects
- XC6VLX130T-2FFG1156C FPGA
- 4 x 4 GBit DDR3 Sample Memory
- additional point to point links over backplane
- In field firmware upgrade
- DESY MMC1.0

DWC8300/DWC10 Downconverter RTM

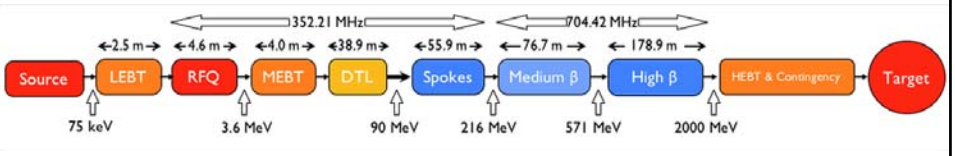
- 10 channel downconverter
- 1 to 4 GHz
- FP and RF backplane

- 1.3, 3.0 and 3.9 GHz units shipped

Under license of DESY



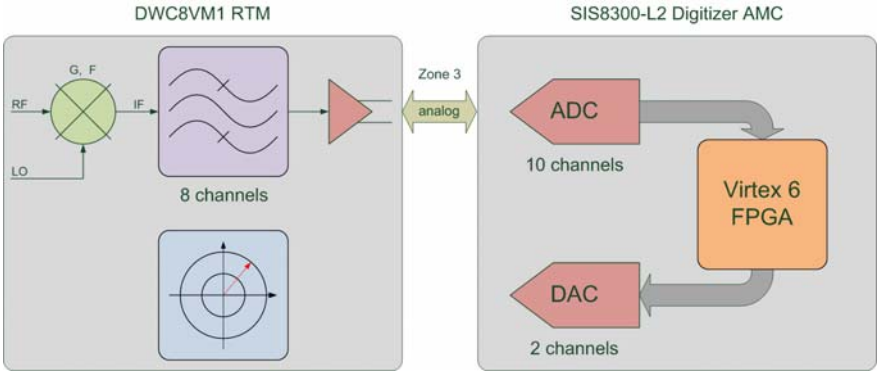
ESS Accelerator Layout



Source: https://europeanspallationsource.se/accelerator/how-it-works

- 1 RFQ
- 3 Pillbox buncher cavities in MEBT
- 5 Drift Tube Linac sections
- 26 Superconducting spoke cavities
- 36 Superconducting medium-b cavities
- 84 Superconducting high-b cavities

SIS8300-x/DWC8VM1 as single cavity LLRF solution covering 350 MHz to 6 GHz



Current combination: SIS8300-KU Kintex Ultrascale Digitizer and DWC8VM1

DWC8VM1
8 Channel Downconverter
One Channel Vectormodulator*

Model	f_{min} in MHz	f_{max} in MHz
DWC8VM1LF	350	500
DWC8VM1	500	3500
DWC8VM1HF	3500	6000

DWC8VM1 Overview Table

*under license from DESY

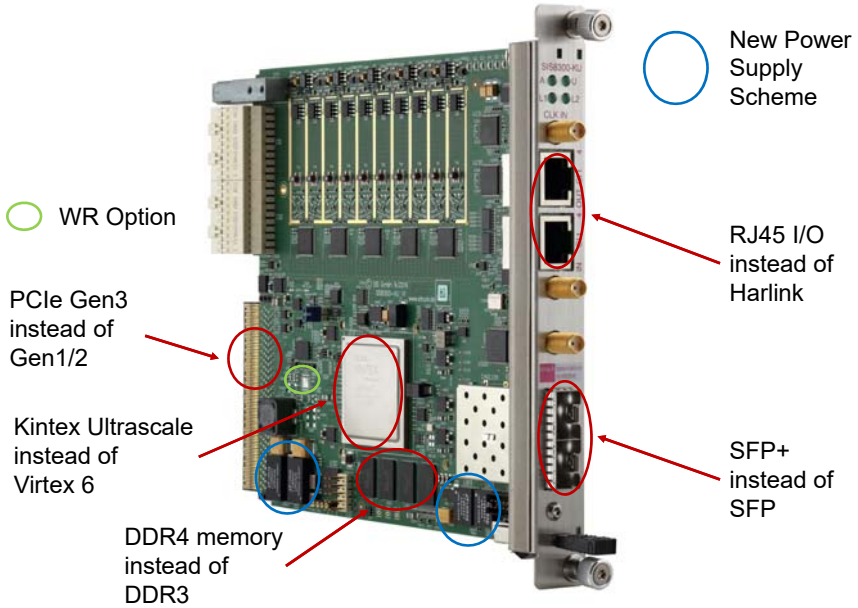
DWC8VM1 Properties

- MTCA.4 RTM Implementation
- 8 Channels Downconverter
- 350 MHz - 6 GHz (3 different types)
- 8 Channel FBM Multi Coax. Connector (CH1 to CH8)
- 2 Auxilliary Channels
- One Channel Vector Modulator
- VM Output 50 MHz to 6 GHz
- SMA Vector Modulator Output
- Various Intermediate Frequencies
- Switchable Front End Attenuators
- LO Clock From Front Panel or RF Backplane
- LO Power Level Monitor
- Interlock Scheme
- I2C Support
- Zone 3 Class A1.1 compatible

DWCx @ ESS

- DWC8VMLF 352 MHz for low energy part
- DWC8VM1 704 MHz for high energy part
- DWC10LF for Beam Position Monitor (BPM)

SIS8300-KU versus L2 changes

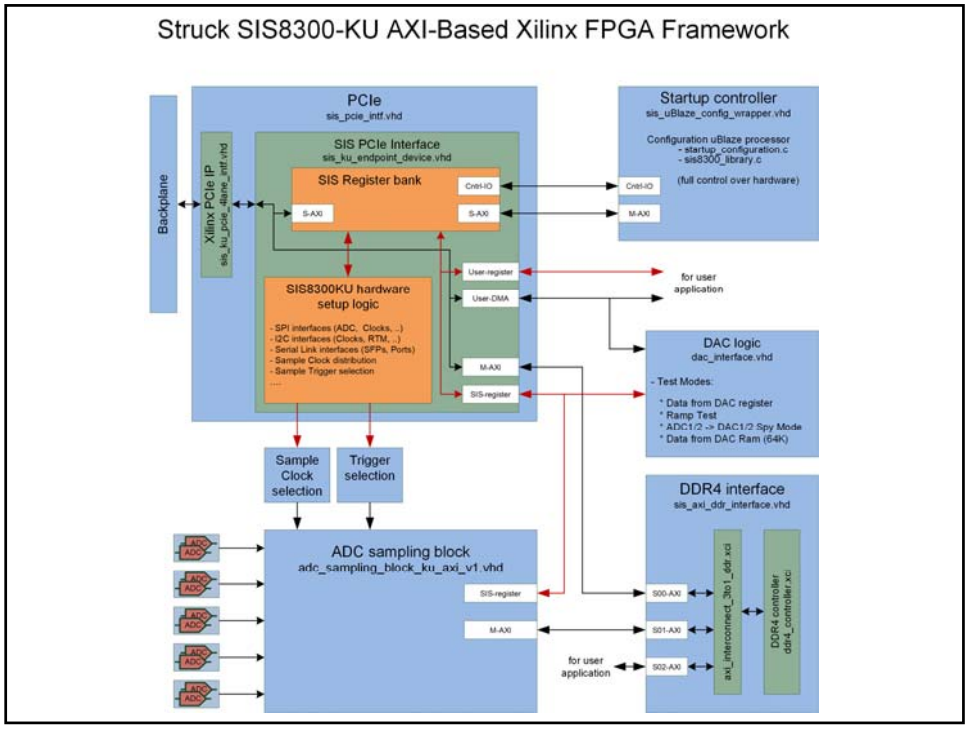


SIS8300-KU Properties

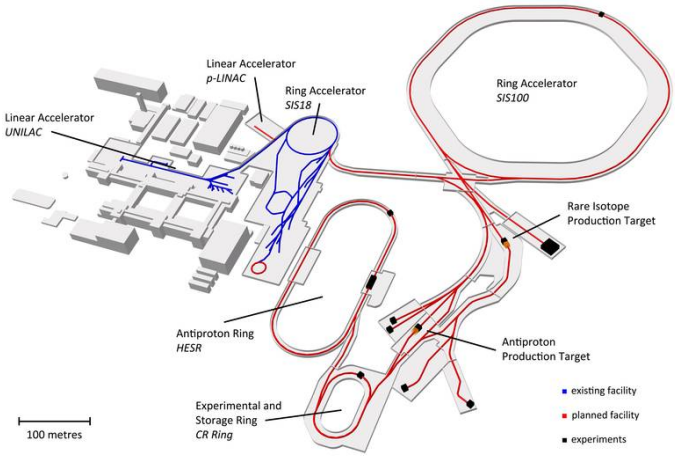
- 10 Channels 125 MS/s 16-bit ADC (250 MS/s 14-bit ADC version available also)
- 10 MS/s to 125 MS/s Per Channel Sampling Speed
- AC or DC Input Stage
- Internal, Front Panel, RTM and Backplane Clock Sources
- Two 16-bit 250 MS/s DACs for Fast Feedback Implementation
- High Precision Clock Distribution Circuitry
- Programmable Delay of Dual Channel Digitizer Groups
- Multi Gigabit Link Port Implementation to Backplane
- Twin SFP+ Card Cage for High Speed System Interconnects
- White Rabbit Clock Option for SFP+ Ports
- Two RJ45 Connectors (One Clock + 3 Data or 4 Data In/Out)
- XCKU040-1FFVA1156C Kintex Ultrascale FPGA
- 2 GByte DDR4 Memory (flexible partitioning scheme)
- 4 lane PCI Express Gen3 Connectivity
- Dual boot
- MMC1.0 under DESY license LV91
- In Field Firmware Upgrade Support
- Zone 3 class A1.0, A1.0C or A1.1CO Compatible

SIS8300-KU
AXI Based VIVADO Project

- Cooperation Lund University/ESS/Struck
- To Meet ESS/ERIC Firmware Specs
- ESS Version → COSYLAB EPICS
- Struck Version available to all users

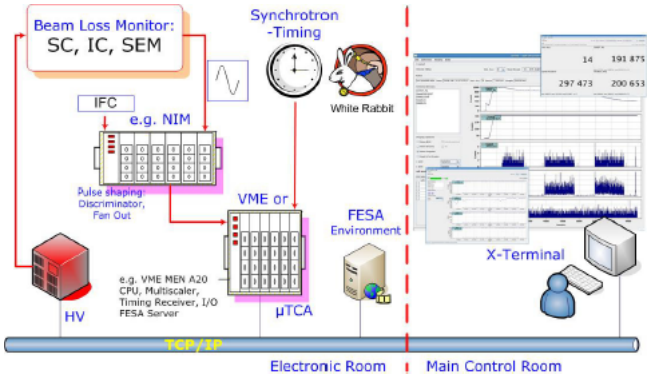


The FAIR Complex
Facility for Antiproton and Ion Research



1,3 GEUR → One of the larger accelerator projects in the world
Modularized Start Version with 2022 timeframe and full operation in 2025

Large Analog Signal and Scaling Information Environment (LASSIE)



SIS8800 Multi Purpose Scaler

Functionality

- MTCA.4 AMC
- 4 Lane PCI Express connectivity
- XC6VLX130T-2FFG1156C Xilinx
- Dual boot
- Redundant PCIe implementation
- 2 GByte DDR3 memory
- 16 front inputs NIM or TTL/LEMO, TTL,ECL or LVDS/flat cable
- 200 MHz count rate (NIM/ECL)
- 4 control in-/4 control front outputs
- Zone 3 Class D1.1 compatible
- MMC 1.0 under DESY license LV91

→ good fit for SRI (Synchrotron Radiation Instrumentation) also

SIS8890 Discriminator RTM for SIS8800 Multi Purpose Scaler

Functionality

- MTCA.4 RTM
- 16 Discriminator Inputs, Connector Type MMCX
- Leading Edge
- 50 Ω Input Termination
- 14 Bit Threshold DAC for each Channel, 0.4 mV/Step
- 16 Outputs to Zone 3 (to Scalers on SIS8800)
- 16 Front Outputs, Connector Type MMCX
- Programmable Pulse Width 10 ns -250
- Zone 3 Class D1.1 Compatible
- MMC1.0 Compatible

SIS8980 in NIM/MMCX Configuration

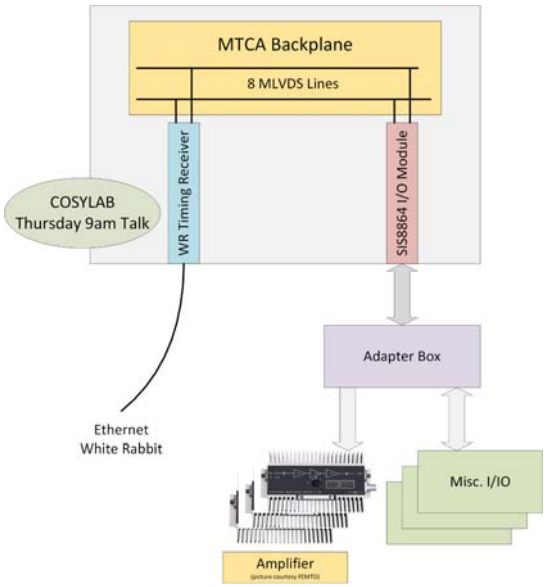
SIS8864 64 channel LVTTL Digital I/O AMC

- Machine cycle dependent & generic ouput pattern with digital input
- Alternative to OHWR FMC carrier and two I/O FMC‘s
- Ready to run firmware
- Application specific firmware adaptations

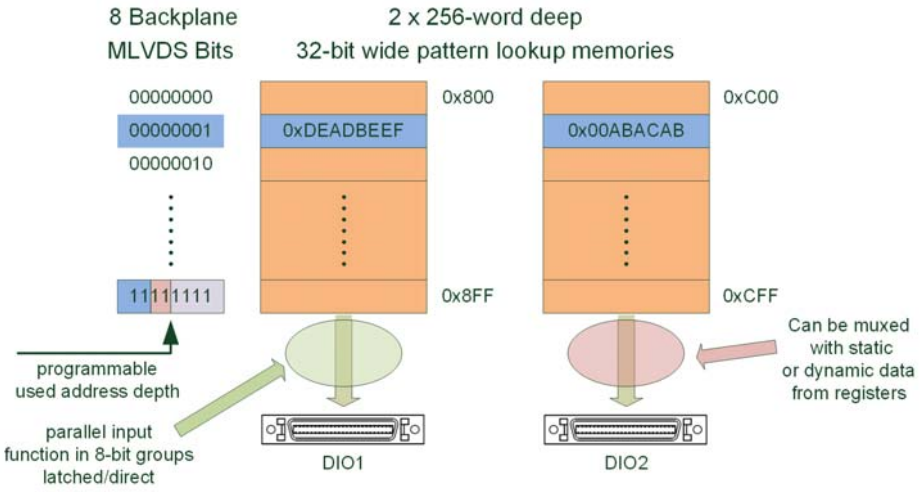
SIS8864 64 channel LVTTL Digital I/O AMC Properties

- AMC with Double Width Mid-Size form factor
- Xilinx XC7A15T-2FGG484C Artix-7 FPGA
- Single lane PCI Express Gen2 Interface
- 1 AMC Port GbE
- 2 AMC Ports Point-to-Point Serial Link
- 4 AMC Ports MLVDS (8 MLVDS lines)
- 2 Front panel 32 data I/O: Mini D Ribbon (MDR) (TTL/LVTTL)
- I/O direction programmable in 8-Bit Groups
- 1 Front panel control Input: LEMO (TTL/LVTTL)
- 1 Front panel control Output: LEMO (LVTTL)
- In field firmware upgrade capability
- Module Management Controller ATxmega128A1U, IPMB-L interface
- DESY MMC1.0 (under LV 91)

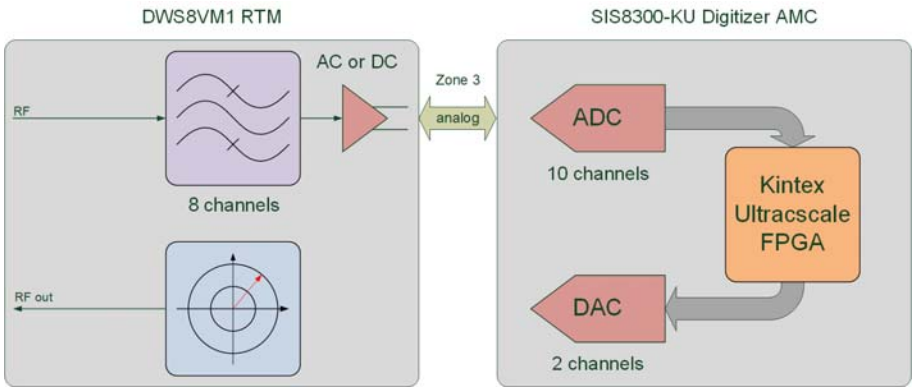
Typical FAIR SIS8864 Digital I/O Use Case



SIS8864 Digital I/O Firmware Detail
Event Receiver/MLVDS → Pattern Memory



SIS8300-KU/DS8VM1
as single cavity LLRF solution
covering 5 MHz to 500 MHz

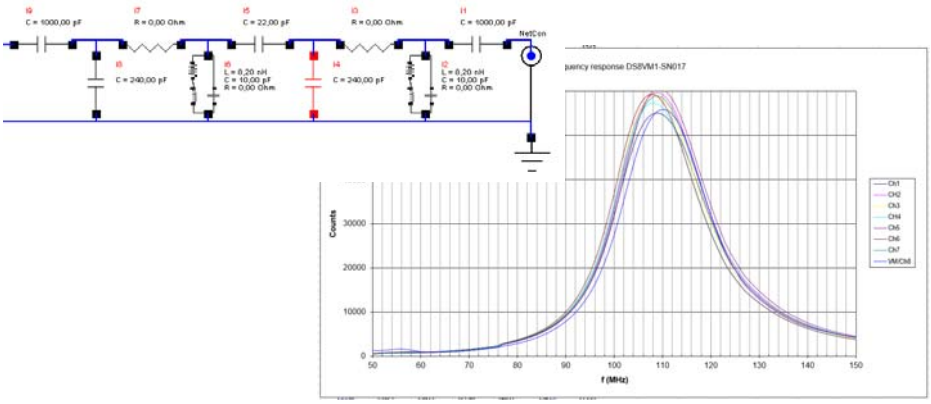


DS8VM1
8 Channel Direct Sampling
One channel vectormodulator*

SIS8300-KU/DS8VM1
as single cavity LLRF solution
covering 5 MHz to 500 MHz
UNILAC: 108.4 MHz
Undersampling at 86.7 MSPS

*under license from DESY

DS8VM1 GSI 108 MHz Input Filter and Input Response



Jens Zappai et. al. LLRF2017 P12
A MTCA.4 BASED DIGITAL LLRF SYSTEM FOR THE GSI UNILAC

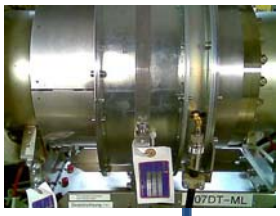
FAIR FCT Application (Fast Current Transformer)

- Test System with SIS3350 500 MSPS 12-bit VME Digitizer
- Development of new MTCA FMC Carrier and 2.5 GSPS 14-bit Digitizer FMC

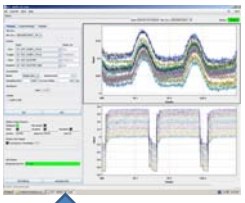
Measurements in the SIS 18. Setup (courtesy GSI)

Detector in SIS tunnel, view 2

Detector in SIS tunnel, view 1



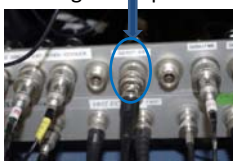
GUI in control room



~100m cable

Electronic room

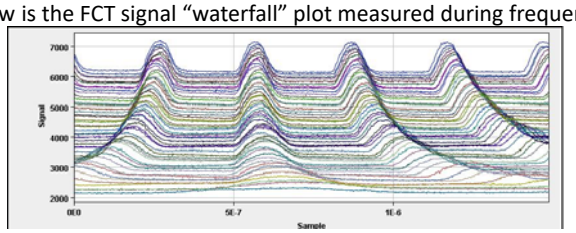
Signal output



Amplifier

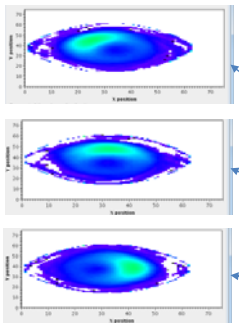
VME DAQ

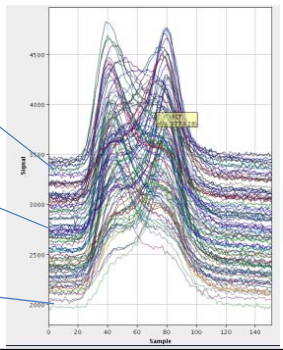
Observation of the signal during different processes
(below is the FCT signal "waterfall" plot measured during frequency ramp)



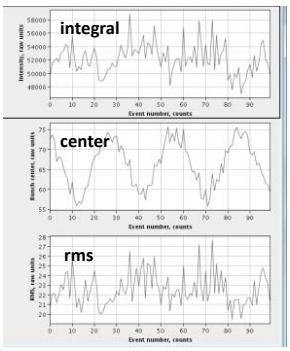
Applications

Bunch phase space reconstruction
(tomography) at different times





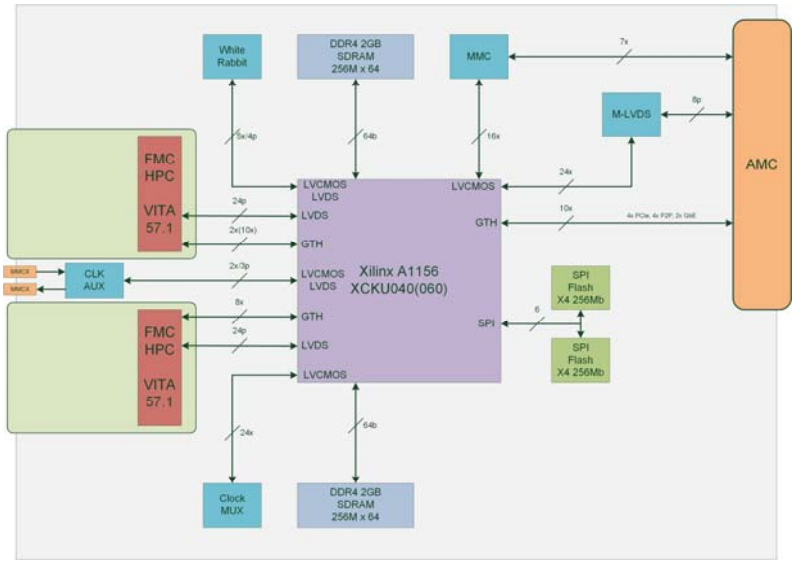
Observation of the single bunch parameters
in time during unstable behavior



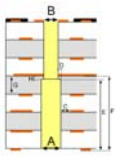
SIS8160 Dual FMC Carrier AMC

- 4-lane PCI Express Gen3 Connectivity
- Xilinx XCKU40- or XCKU060-1FFVA1156C Kintex Ultrascale FPGA
- Dual Boot
- Front Panel MMCX Clock Input
- Front Panel MMCX Digital In-/Output (HW Configuration)
- Point to Point Links
- 4 MLVDS µTCA Ports (AMC Ports 17-20) → 8 MLVDS lines
- 2 HPC FMC Sites
- Variable FMC VADJ (1,0V - 1,8V)
- Low Jitter Clock Generation and Management
- 2 x 2 GByte DDR4 Memory with two Memory Controllers
- White Rabbit Option (over FMC 2)
- Stand Alone Operation Option
- MMC1.0 under DESY LV91

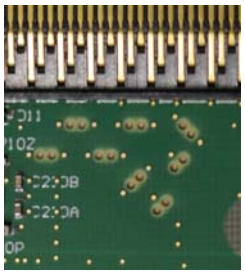
SIS8160 Block Diagram



Technical Aspect I: Backdrilled Vias



Decreasing via stub length by backdrilling significantly reduces a particularly problematic form of signal distortion called deterministic jitter. Because Bit Error Rate (BER) is strongly dependent on deterministic jitter, any reduction in deterministic jitter by backdrilling will significantly reduce the overall BER of the interconnect – often by many orders of magnitude. Other key advantages to backdrilling PTH vias include less signal attenuation due to improved impedance matching, increased channel bandwidth, reduced EMI/ EMC radiation from the stub end, reduced excitation of resonance modes and reduced via-to-via crosstalk.



24 (12 pairs) backdrilled vias for 4 PCIe lanes JESD routed without backdrilling requirements tradeoff: size (rest ring plus 200 µm)

Drawing source: www.multi-circuit-boards.eu
Text source: www.sanmina.com

Technical Aspect II: PCB Layer Stack

Layer Stack SIS8160						
Target Thickness = 1.6mm ± 10%						fix
10% ≙ ± 160µm						
Layer / Kerne /Prepreg	Mat.	CU Aufgabe Verwendung	PP = Pregreg LA = Laminat Mat.-Bez.	Style / Dicke	Copper Coverage %	berechnete verpresste Starke(µm)
	Lötstop					20
18+37 galv. Cu L1	Cu-Folie	Signal			100 fix	52
1080	Prepreg		Megtron PP R-5670	1080 / 76µ		71,5
L2	Cu	Powerplane			78	32
Core 100um + 35um CU	Laminat		Megtron LA R-5775	3313 / 100µ		100
L3	Cu	Powerplane			78	32
3313	Prepreg		Megtron PP R-5670	3313 / 106µ		93,4
L4	Cu	Signal			43	15
Core 100um + 18um CU	Laminat		Megtron LA R-5775	3313 / 100µ		100
L5	Cu	Signal			42	15
3313	Prepreg		Megtron PP R-5670	3313 / 106µ		96,4
L6	Cu	Powerplane			77	15
Core 100um + 18um CU	Laminat		Megtron LA R-5775	3313 / 100µ		100
L7	Cu	Signal			42	15
3313	Prepreg		Megtron PP R-5670	3313 / 106µ		90,4
L8	Cu	Signal			43	15
Core 100um + 18um CU	Laminat		Megtron LA R-5775	3313 / 100µ		100
L9	Cu	Powerplane			78	15
3313	Prepreg		Megtron PP R-5670	3313 / 106µ		95,9
L10	Cu	Signal			41	15
Core 100um + 18um CU	Laminat		Megtron LA R-5775	3313 / 100µ		100
L11	Cu	Signal			42	15
3313	Prepreg		Megtron PP R-5670	3313 / 106µ		92,9
L12	Cu	Powerplane			77	32
Core 100um + 35um CU	Laminat		Megtron LA R-5775	3313 / 100µ		100
L13	Cu	Powerplane			78	32
1080	Prepreg		Megtron PP R-5670	1080 / 76µ		71,5
18+37 galv. Cu L14	Cu-Folie	Signal			100 fix	52
	Lötstop					20
						1604
						variabel

Megtron 6 layers because of Gen3 PCIe and JESD speeds

8 signal, 6 power layers

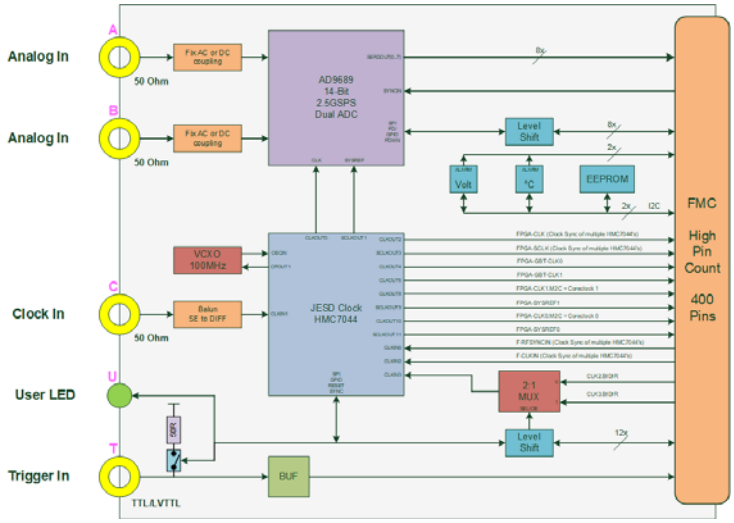
Limited number of PCB foundries with sufficient capabilities

Measured thickness of prototype batch 1.58 mm versus calculated value of 1.60 mm (excellent match)

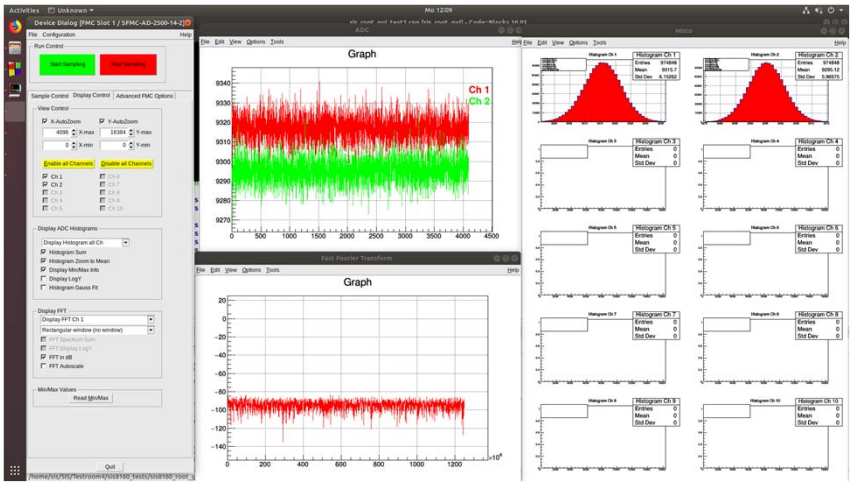
SFMC01
2 Channel 2.5 GSPS 14-Bit

- Single width, 10mm stacking height, air cooled commercial grade HPC FMC Module
- Analog front-end factory configurable for DC- or AC (Balun) input coupling
- Up to 5 GHz AC Analog BW
- Up to 1 GHz DC Analog BW
- Dual channel 14-Bit, 2.5 GSPS with JESD204B Interface
- 50 Ohm Input Termination
- 4 Front panel SMA Inputs for Analog A/B, Clock and Trigger
- Ultra low phase noise 100 MHz on board clock source
- High performance jitter attenuating frequency generator for JESD204B
- one green Front panel user LED
- System management EEPROM and Temperature Sensor with Thermal Watchdog

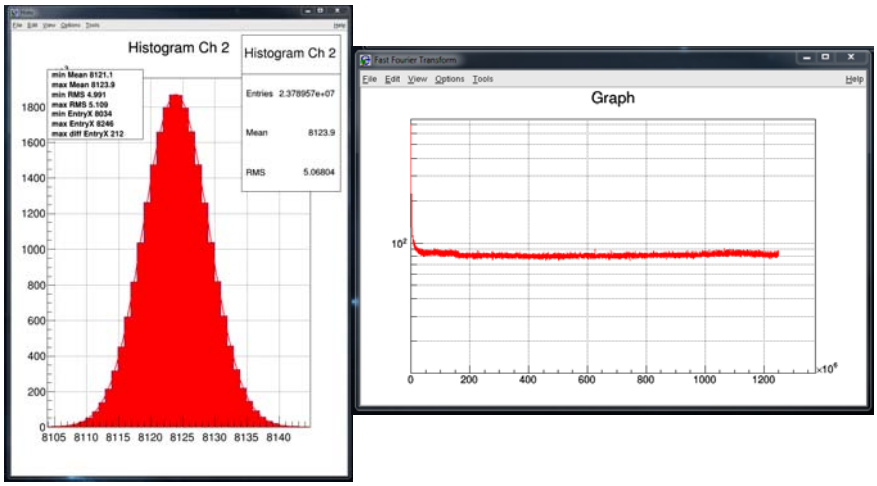
SFMC01
2 Channel 2.5 GSPS 14-Bit



SIS8160/SFMC01 ROOT GUI
DC Configuration 1 GHz BW



SFMC01 AC 5 GHz BW Open Input



Possible next FMC JESD Developments

- 4 Channel GSPS 16-bit Digitizer
- 8 Channel 500 MSPS 14-bit Digitizer
- Project Driven …
- ADC/DAC Combination …

Summary

MTCA/MTCA.4 adopted by many European (and Asian) accelerators as instrumentation standard

XFEL (and FLASH) in reliable user operation

ATCA, still VME, custom designs, other standards in use as well → niche market

MTCA.4 Relevance, current Struck user base

AU	Australian Synchrotron
BR	LNLS
CH	CERN, PSI
CN	IHEP Beijing, SINAP, USTC, IMP
CZ	ELI (Inst of Physics, Praha)
DE	DESY, HZDR, PTB, MPG, KIT, HZB, GSI, DESY Zeuthen, HIM
ES	ESS Bilbao, GMV
FR	ITER, Saclay
GB	Diamond, STFC
IN	TIFR
JP	KEK, SPring-8
KR	PAL
RU	ITER, NICA (Bevatech/DESY)
SE	ESS, Lund University
TR	TARLA (DESY)
TW	NSRRC
US	SLAC, NSCL/FRIB, ANL, ORNL

Questions/Discussion

TEMPERATURE DRIFT CORRECTION IN A RIGID-BOOM ELECTROMAGNETIC INDUCTION GEOPHYSICAL INSTRUMENT

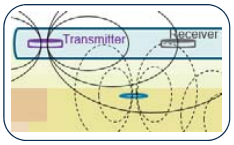
8TH APR 2019 | XIHE TAN | ELECTRONIC SYSTEMS (ZEA-2) | FZ JUELICH

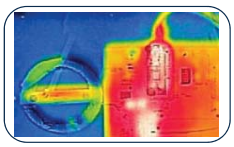
Co-authors: A. Mester[1], E. Zimmermann[1], M. Dick[1], W. Glaas, M. Ramm, J. van der Kruk[2], S. van Waasen[1,3]

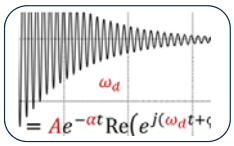
[1]Electronic Systems (ZEA-2) FZJ, [2]Agrosphere (IBG-3) FZJ, [3]University of Duisburg-Essen, Communication Systems (NTS)

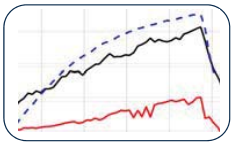
OUTLINE

- Introduction to Electromagnetic Induction (EMI)
- Pre-measurements & Analytical Study of the Temperature Drifts
- Temperature Drift Correction Method
- Experimental Verification
- Case Study
- Conclusion & Outlook





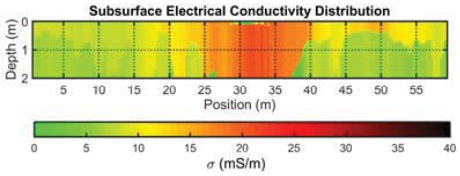




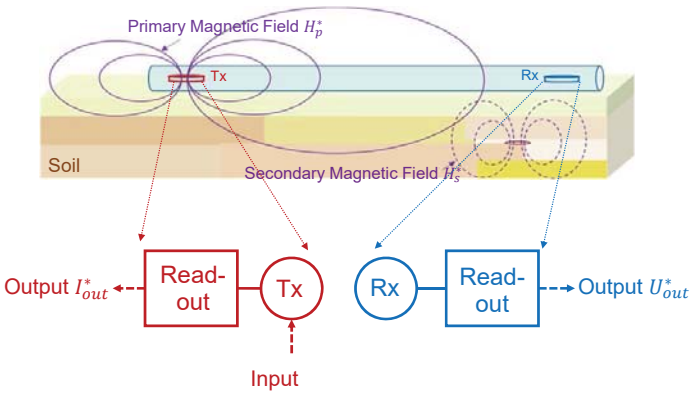
ELECTROMAGNETIC INDUCTION (EMI) SYSTEM

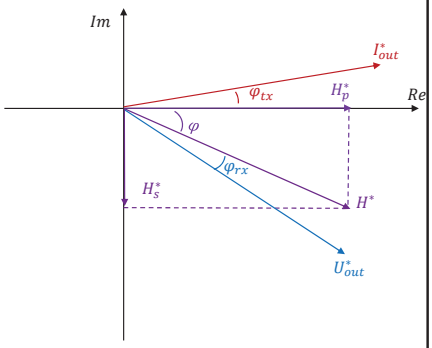
- Frequency-domain electromagnetic induction technique
  - Contactless
  - Non-invasive
  - Portable

- Geophysical investigations: electrical conductivity (σ) distribution of subsurface
  - Soil salinity characterization
  - Mineral exploration
  - Clay and water content analysis
  - Organic matter evaluation



EMI THEORY





Apparent electrical conductivity (McNeil 1980)

$$\mathrm{ECa} = \frac{4}{\mu_0 \omega_{tx} s^2} \mathrm{Im}\left(\frac{H_s^*}{H_p^*}\right) \approx \frac{4}{\mu_0 \omega_{tx} s^2} \varphi$$

s: Tx-Rx separation
ω_{tx}: angular Tx frequency
μ_0: free space magnetic permeability

RIGID-BOOM EMI SYSTEM

- Concept View

- System specification

Tx-Rx Separation (m)	0.3 – 1
Tx Frequency (kHz)	5 – 35
Maximum Detecting Depth	1.5 times Tx-Rx separation
U_0 (Vp)	10
24-bit ADC Fs (kHz)	100

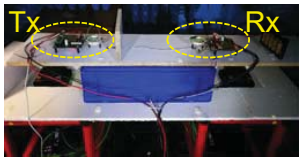
- Measurement Parameters

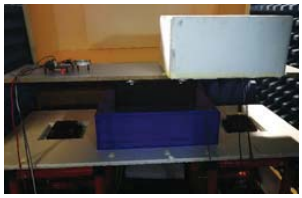
@ Tx frequency = 15 kHz, Tx-Rx Separation = 0.8 m	
I_{out} (mA)	~121
U_{out} (mV)	~9.8
φ (μrad) @ECa = 1 mS/m	~19
φ (μrad) @ECa = 50 mS/m	~900

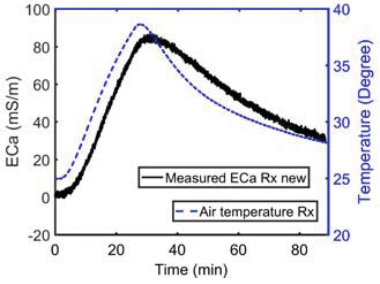
$$\varphi = \frac{\mu_0 \omega_{tx} s^2}{4} ECa$$

s: Tx-Rx separation
ω_{tx}: angular Tx frequency
μ_0: free space magnetic permeability

PRE-MEASUREMENT 1:
TEMPERATURE DRIFTS OF THE RECEIVER



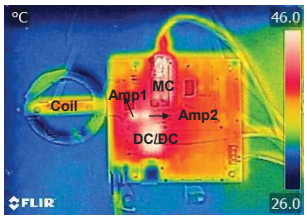


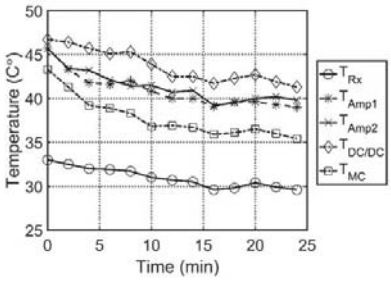


Where the drifts come from?

PRE-MEASUREMENT 2:

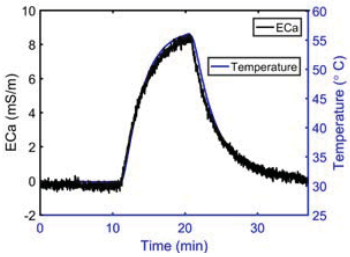
TEST USING THERMAL CAMERA



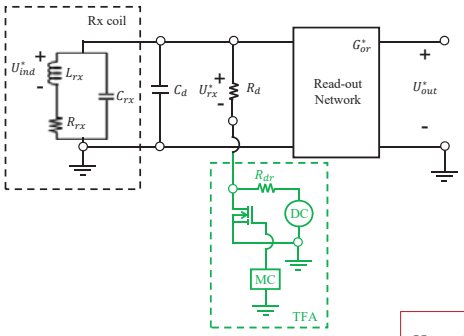


Amp: amplifier
DC/DC: DC/DC converter
MC: Microcontroller

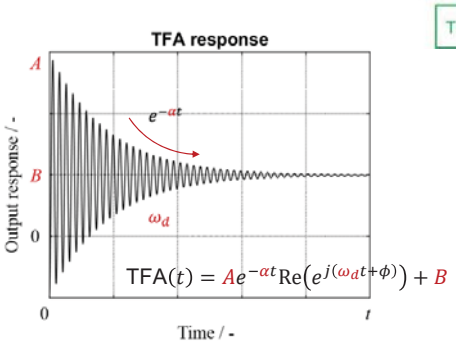
TEST OF ONE AMPLIFIER IN THE READ-OUT CIRCUIT



TRANSFER FUNCTION ANALYZER (TFA)



MC: microcontroller



α: damping factor
ω_d: damping frequency

$$\mathrm{H_{TFA}}(j\omega) = \frac{j\omega + \alpha}{(j\omega + \alpha)^2 + \omega_d^2}$$

$$\arg(\mathrm{H_{TFA}}) \sim \varphi_{rx}$$

TEMPERATURE DRIFT CORRECTION

- TFA to correct temperature drift in the Rx coil

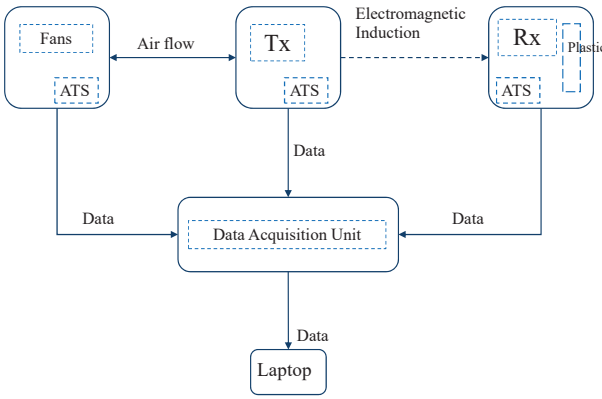
TFA: Transfer Function Analyzer

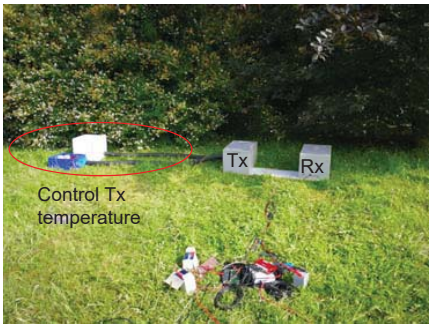
- ATS to correct temperature drifts in the Read-out circuit of Rx unit

ATS: Ambient Temperature Sensor

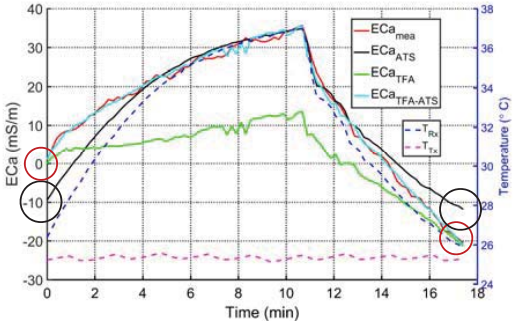
- Manually Control the Tx unit

EXPERIMENTAL SETUP





EXPERIMENTAL RESULTS



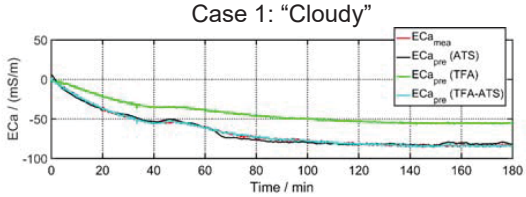
Standardized regression coefficient (beta weight, $\boldsymbol{\beta}$) of the multiple linear regression (MLR) algorithm

$\boldsymbol{\beta}(\Delta\varphi_{\mathrm{TFA}})$	$\boldsymbol{\beta}(T_{\mathrm{Rx}})$	$\boldsymbol{\beta}(T_{\mathrm{Tx}})$
0.56	0.48	0.02

Methods	No-correction	ATS	TFA	TFA-ATS
Root Mean Square Error (RMSE) (mS/m)	21.0	4.8	12.3	1.2

EXPERIMENTAL RESULTS

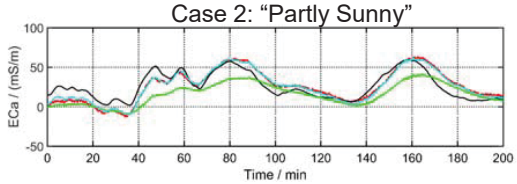
Case 1: “Cloudy”



Temperature range: 26 to 38 ℃

RMSE of TFA-ATS method: 1.2 mS/m

Case 2: “Partly Sunny”

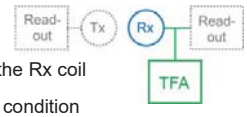


Temperature range: 24 to 32 ℃

RMSE of TFA-ATS method: 2.3 mS/m

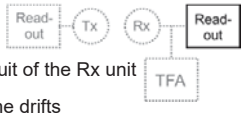
CONCLUSION

TFA



- monitors the phase response of the Rx coil
- is able to trace the initial thermal condition
- TFA corrects for 41% of the drifts

ATS

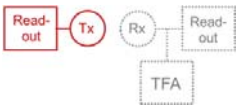


- monitors the read-out circuit of the Rx unit
- ATS corrects for 77% of the drifts

TFA-ATS corrects for 94% of the drifts

OUTLOOK

Monitor the Tx unit



- shows influences in the ECa values
- Further development is needed by applying TFA-ATS to the Tx unit

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THANK YOU FOR YOUR ATTENTION!

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Table 2.3: Mathematical expression for the three methods.

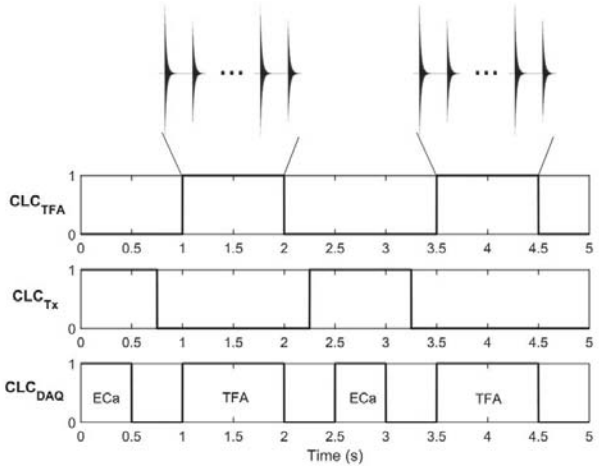
Method	Data used	Mathematical expression
ATS	T_{Tx}, T_{Rx}	$arg(ECa_{pre}) = offset + b\Delta T_{Tx} + c\Delta T_{Rx}$
TFA	TFA	$arg(ECa_{pre}) = \Delta\phi_{TFA}$
TFA-ATS	TFA, T_{Tx}, T_{Rx}	$arg(ECa_{pre}) = offset + a\Delta\phi_{TFA} + b\Delta T_{Tx} + c\Delta T_{Rx}$

$$\arg(ECa_{pre}) = \text{offset} + \boldsymbol{a}\Delta\varphi_{TFA} + \boldsymbol{b}T_{Tx} + \boldsymbol{c}T_{Rx}$$

Linear regression parameters of TFA-ATS method

Measurements	$b(\Delta T_{tx})$	$c(\Delta T_{rx})$
Manually controlled	2.8×10^{-3}	2.0×10^{-3}
"Cloudy"	3.3×10^{-3}	1.5×10^{-3}
"Partly Sunny"	1.8×10^{-3}	1.7×10^{-3}

TIME LINE



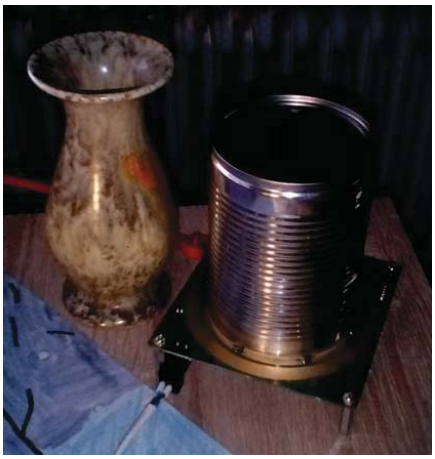
DAQ: Data Acquisition

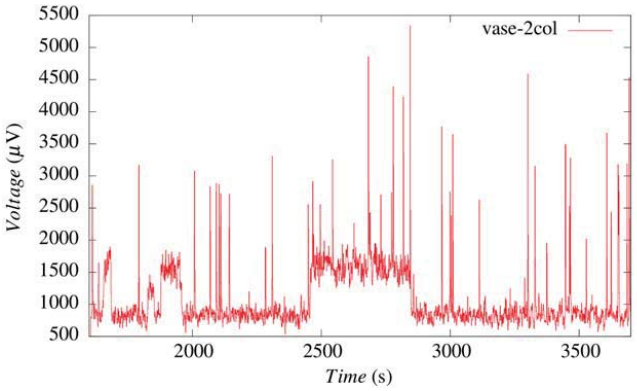
- Use microcontroller to switch the signal
- Each TFA measurement includes 100 TFA pulses
- Each transient pulse decays in about 1 ms, from which 700 μs data is analyzed
- Temperature sensors measure continuously
- A warm-up measurement is performed in advance for about 20 min

Development of a simple ion-chamber based dosemeter system

TECHNISCHE UNIVERSITÄT DARMSTADT

J. Birkhan, U. Bonnes, L. Riik, L. Stobbe, D. Erb, N. Pietralla

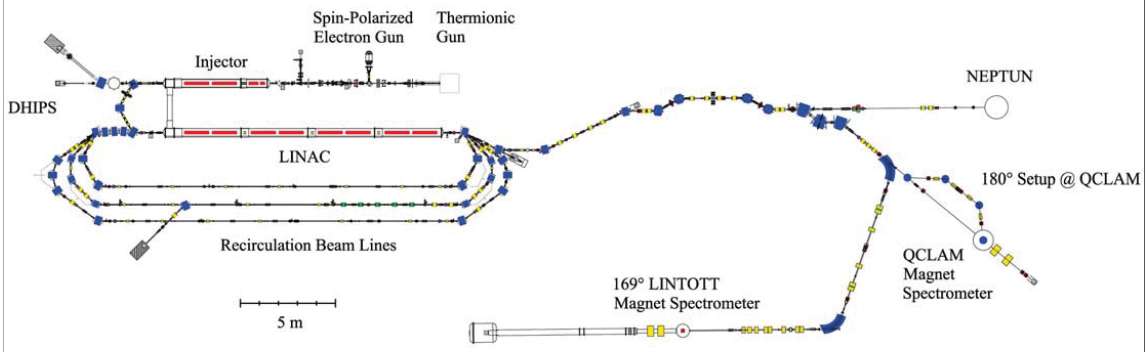




Why developing an ion-chamber based dosemeter system?

TECHNISCHE UNIVERSITÄT DARMSTADT

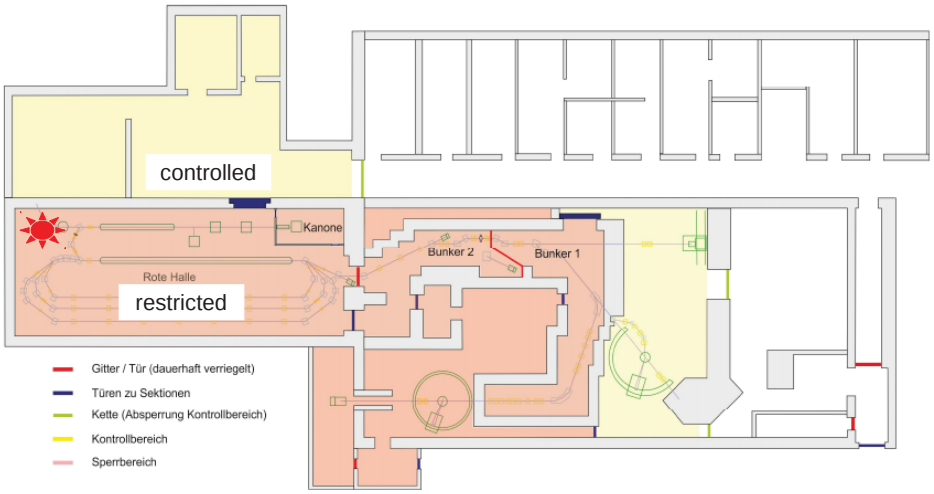
The Superconducting Darmstadt Electron Linear Accelerator S-DALINAC and its nuclear structure experimental facilities



Why developing an ion-chamber based dosemeter system?

TECHNISCHE UNIVERSITÄT DARMSTADT

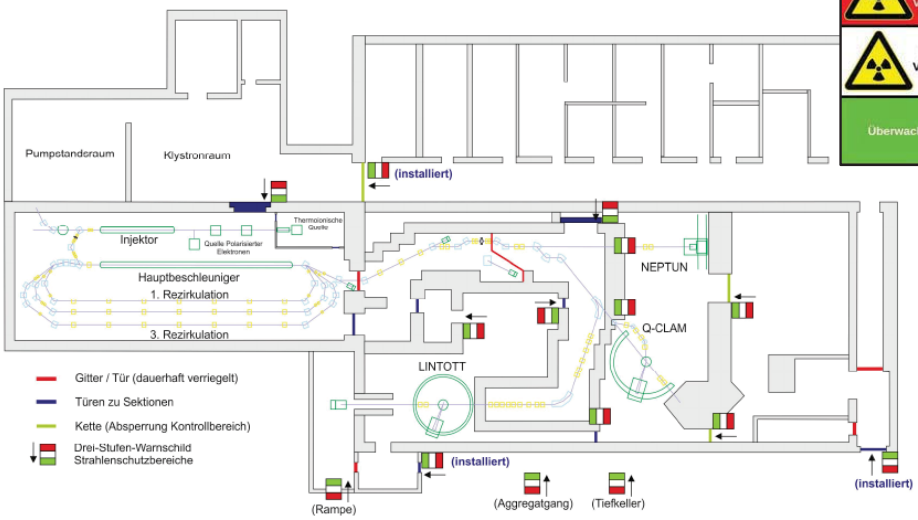
Radiation protection areas at the S-DALINAC during beam@DHIPS



Why developing an ion-chamber based dosemeter system?

TECHNISCHE UNIVERSITÄT DARMSTADT

Declaration of radiation protection areas by illuminated 3-level panels



Why developing an ion-chamber based dosemeter system?

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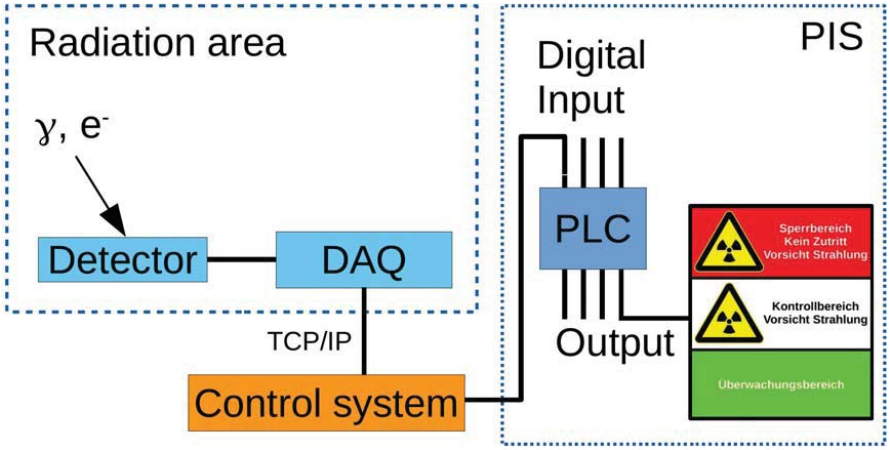
Automatically switching the status of the radiation protection panels when certain dose-rate constraints are fulfilled



Why developing an ion-chamber based dosemeter system?

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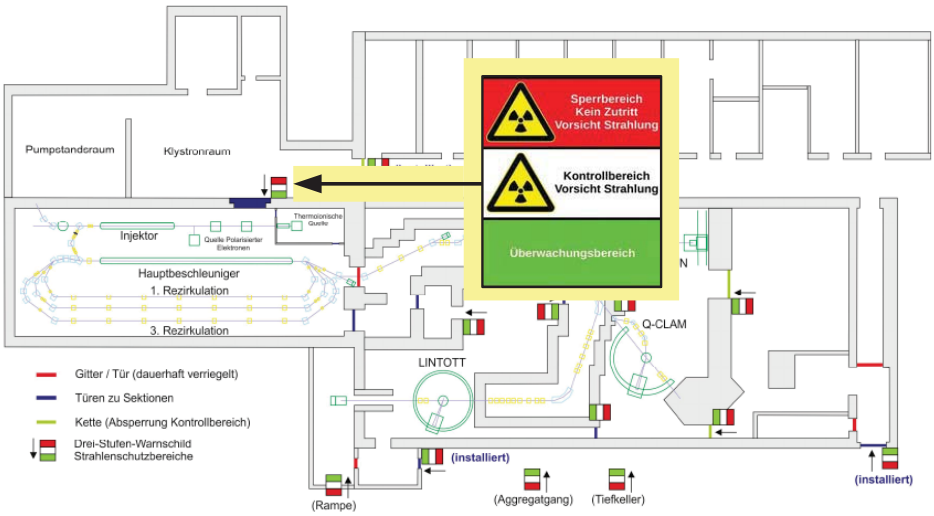
Switch from „Kontrollbereich“ to „Überwachungsbereich“ only if the known hot spots show dose rates < 3 µSv/h



Why developing an ion-chamber based dosemeter system?

TECHNISCHE UNIVERSITÄT DARMSTADT

Constraints on a suitable dose-rate monitor:

1) Simple integration into existing EPICS-based control system
2) Linear response across a large dose-rate range
3) Radiation hardness
4) Detection limit << 3 µSv/h
5) Low maintenance effort
6) Sufficient reliable for the given purpose
7) Fitting to the budget

ION CHAMBER SEEMS TO FIT PERFECTLY.

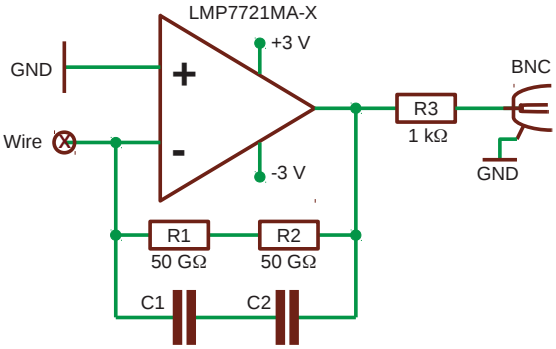
But commercial products take ca. **10000 EUR** for four ion-chamber channels!

Is this the ultima ratio?

Developing a simple ion-chamber based dosemeter system - first version

TECHNISCHE UNIVERSITÄT DARMSTADT

The very beginning, ion chambers made of cans

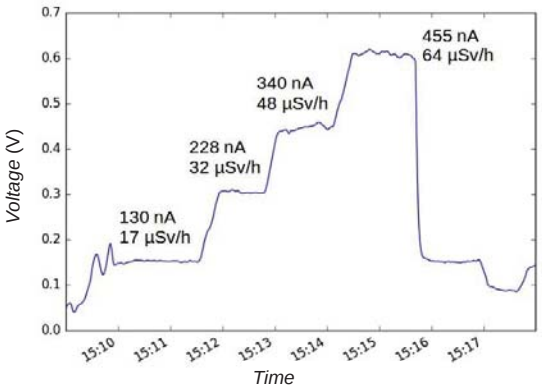


Developing a simple ion-chamber based dosemeter system - measurements

TECHNISCHE UNIVERSITÄT DARMSTADT

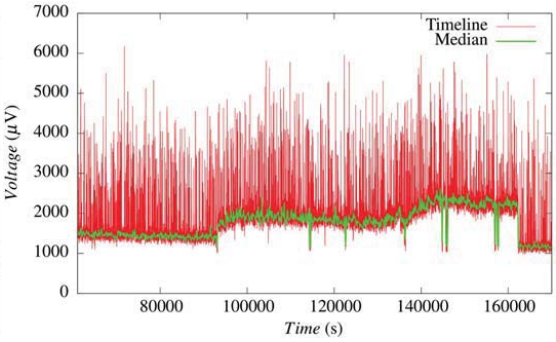
The very beginning, ion chambers made of cans

Close to main LINAC



Ref.: [1]

Klystron room



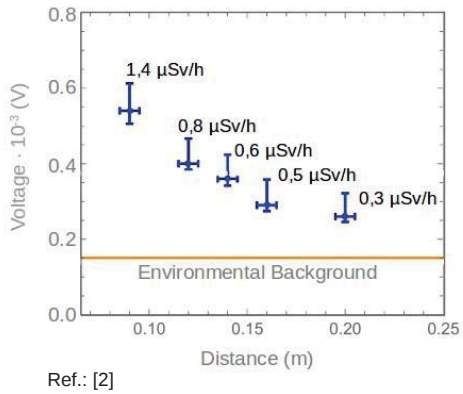
ɣ-radiation exposure is mapped to the median!

Developing a simple ion-chamber based dosemeter system - measurements

TECHNISCHE UNIVERSITÄT DARMSTADT

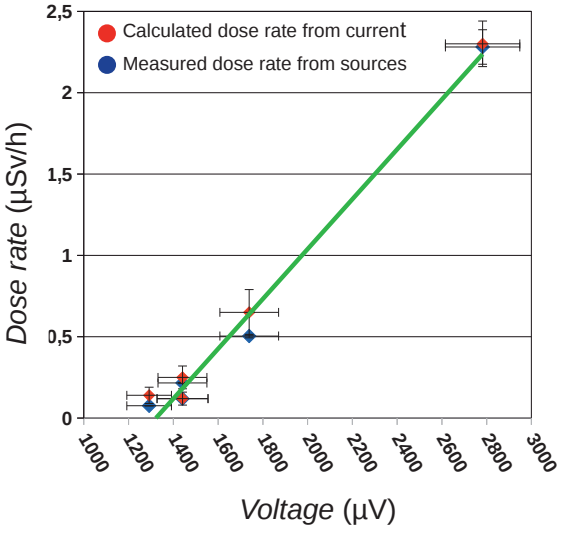
The very beginning, ion chambers made of cans

Co-60 source



Ref.: [2]

Co-60, Cs-137, Am-241 source



Developing a simple ion-chamber based dosemeter system – latest version

TECHNISCHE UNIVERSITÄT DARMSTADT

The latest version, still made of cans

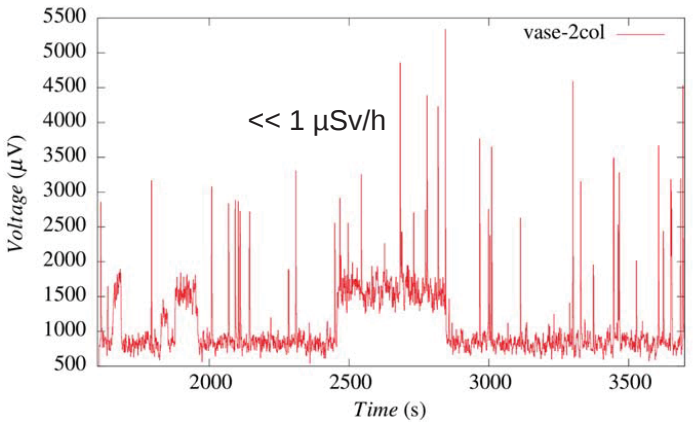
„Hochohmiger Transimpedanzverstaerker (Rueckkopplung 100 GOhm, 10 pF mit Zeitkonstante ~ 1 s)

- OPAmp = LMP7721 (relativ geringe Offsetspannung)
- Rueckkopplung und OPAmp Eingang von der Platine abgehoben
- Alle "heissen" Punkte mit Masse umgeben und mit offenen Masseflächen ohne Lötstopp zur Ableitung von Oberflächenströmen versehen
- On-Board 24-bit Sigma Delta Wandler (Max11200) mit ± 1.65 Volt Versorgung und Messbereich
- Auswertung mittels Mikrokontroller
- Unabgeschlossene Übertragung mittels eines Adernpaares eines RJ45 Kabels, die drei anderen Paare werden zur Speisung mit 5 Volt benutzt
- Vorspannung der Kammer mit 10 Lithium Knopfzellen auf Gehäuse der Ionenkammer“

Developing a simple ion-chamber based dosemeter system - measurements

TECHNISCHE UNIVERSITÄT DARMSTADT

The latest version, still made of cans → suitable for measurements of low activity!



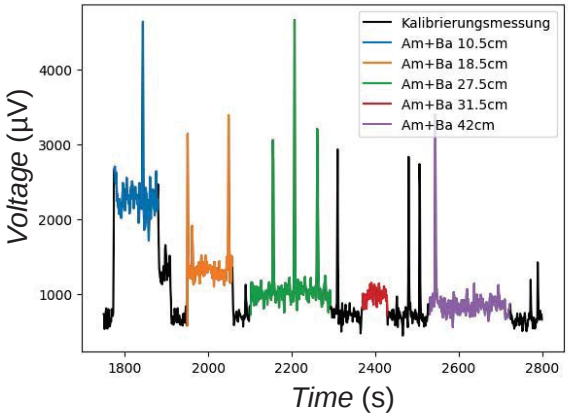
Uranium colour

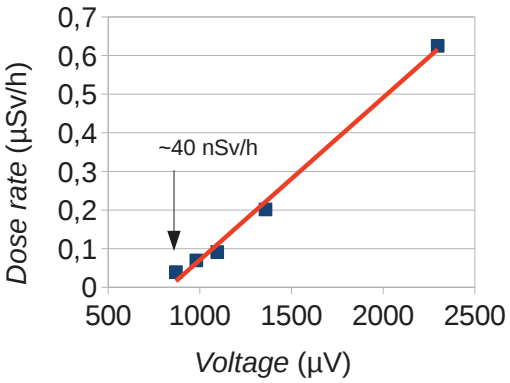
Developing a simple ion-chamber based dosemeter system - measurements

TECHNISCHE UNIVERSITÄT DARMSTADT

The latest version, still made of cans

Am-241, Ba-133 source



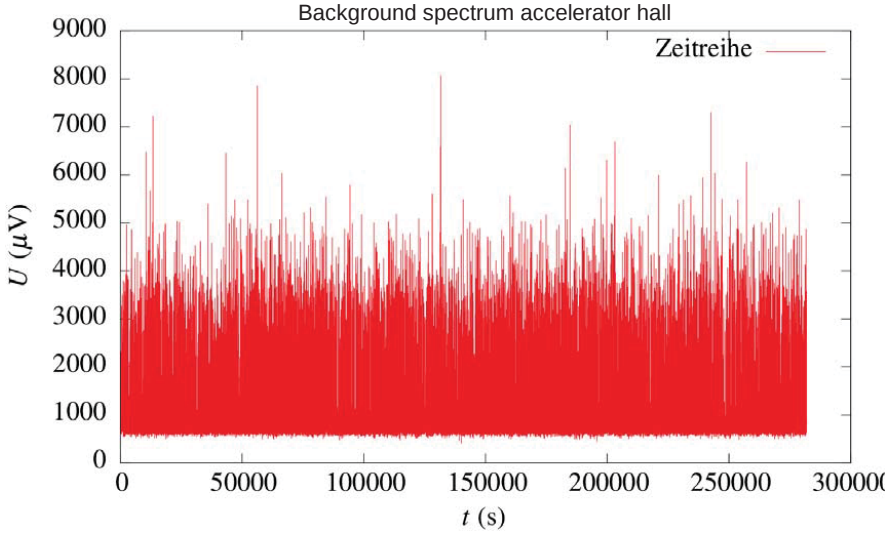


Developing a simple ion-chamber based dosemeter system - measurements

TECHNISCHE UNIVERSITÄT DARMSTADT

The latest version, still made of cans

Background spectrum accelerator hall

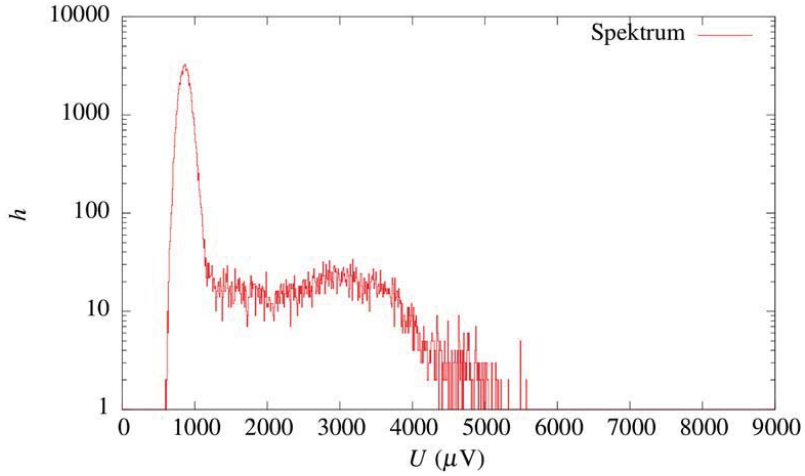


Developing a simple ion-chamber based dosemeter system - measurements

TECHNISCHE UNIVERSITÄT DARMSTADT

The latest version, still made of cans

Background spectrum accelerator hall

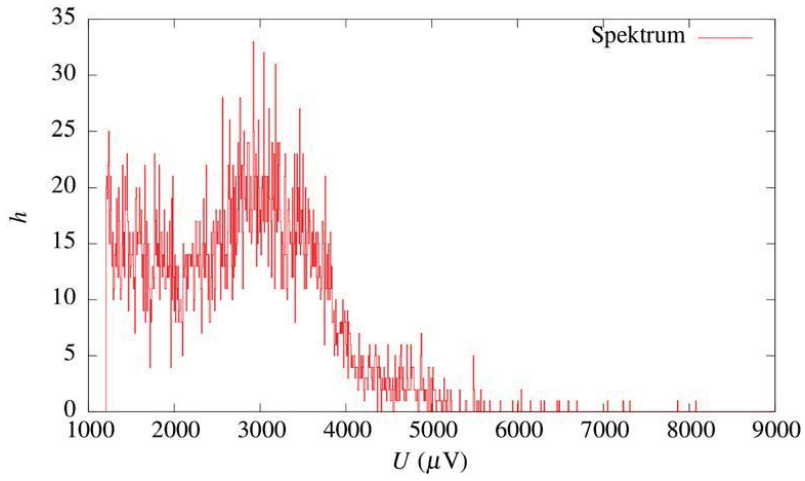


Developing a simple ion-chamber based dosemeter system - measurements

TECHNISCHE UNIVERSITÄT DARMSTADT

The latest version, still made of cans

Background spectrum accelerator hall



Summary & Outlook

TECHNISCHE UNIVERSITÄT DARMSTADT

- Successful test of a simple and low cost ion-chamber designs
- Low-activity (dose rate << 1 µSv/h) measurements of environmental samples can be done
- All requirements are fulfilled except:

1) a median filter needs to be implemented
2) the origin of the single peaks needs to be determined via
   I. measurement in He or N_2 environment (radon)
   II. coincidence measurements (cosmics)

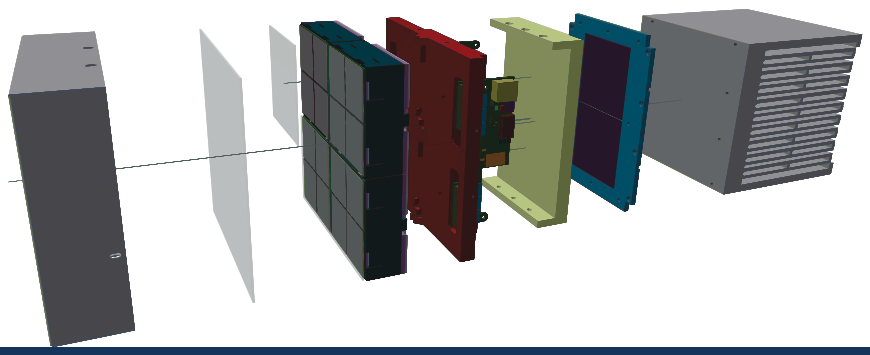
Thanks for your attention!

List of references

TECHNISCHE UNIVERSITÄT DARMSTADT

[1] Lennart Stobe: *Simulation von Strahlungsflüssen am S-DALINAC mit FLUKA und Inbetriebnahme von PIN-Dioden-Detektoren und einer Ionisationskammer für Dosisleistungsmessungen,* B.Sc.-Arbeit, TU Darmstadt, 2017.

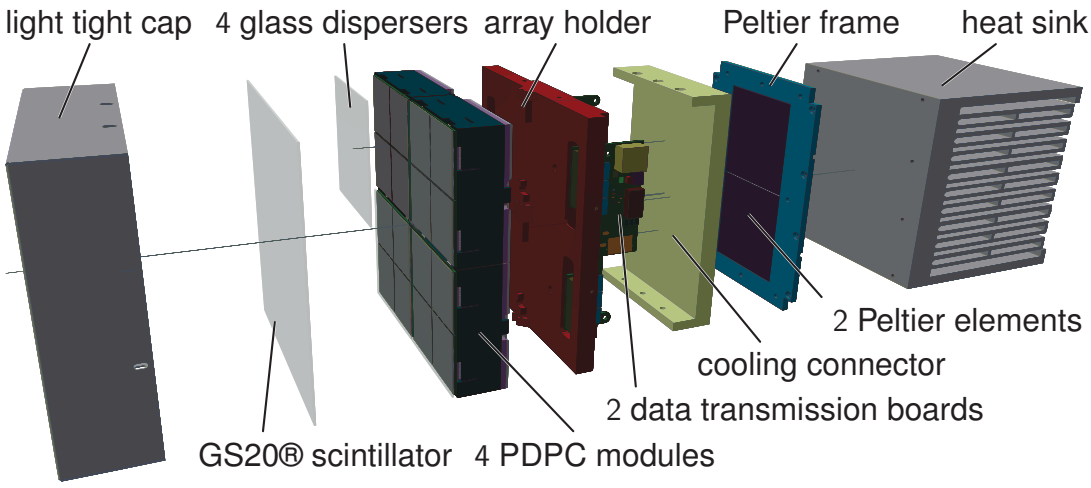
[2] Louise Marc: *Strahlenschutzrelevante Charakterisierung der Beschleunigerhalle des S-DALINACS*, B.Sc.-Arbeit, TU Darmstadt, 2017.



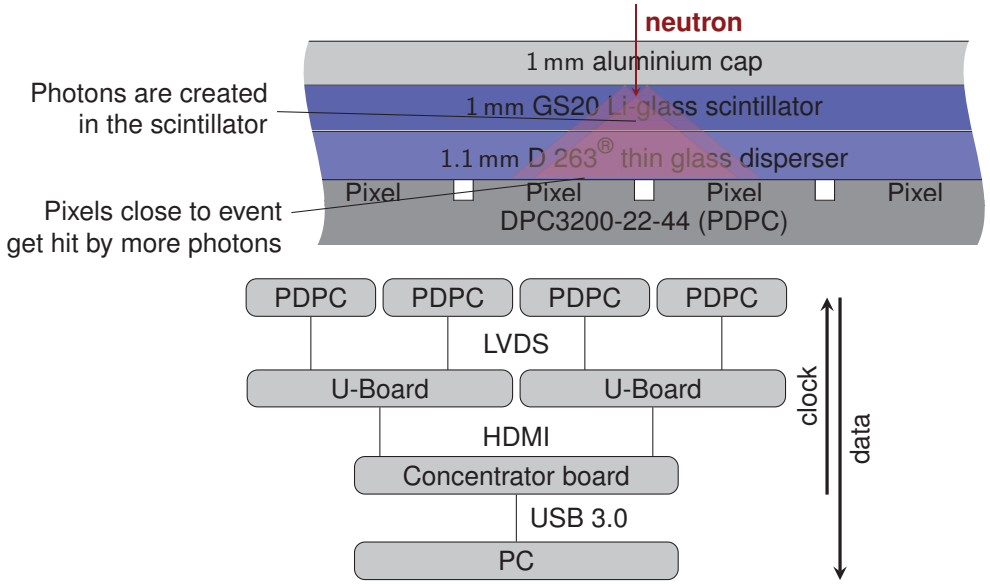
Development of a Scintillation Neutron Detector Prototype using Digital SiPMs

10.04.2019 | Matthias Herzkamp | Central Institute of Engineering, Electronics and Analytics - Electronic systems (ZEA-2)

DETECTOR DESIGN



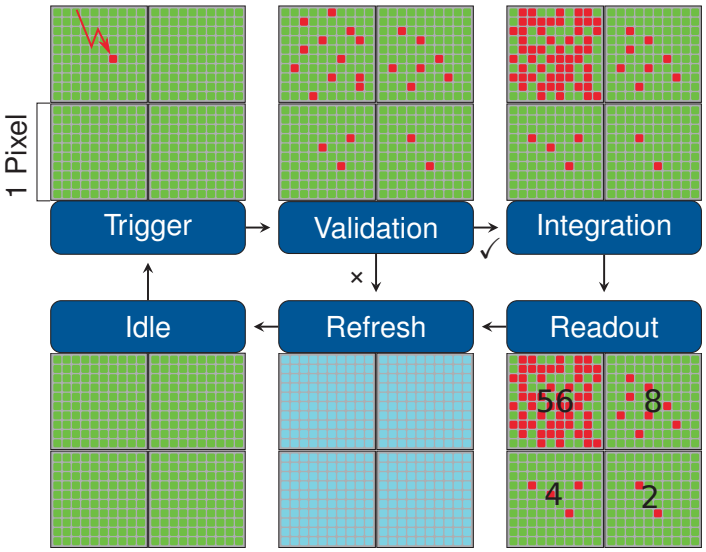
DETECTION PRINCIPLE



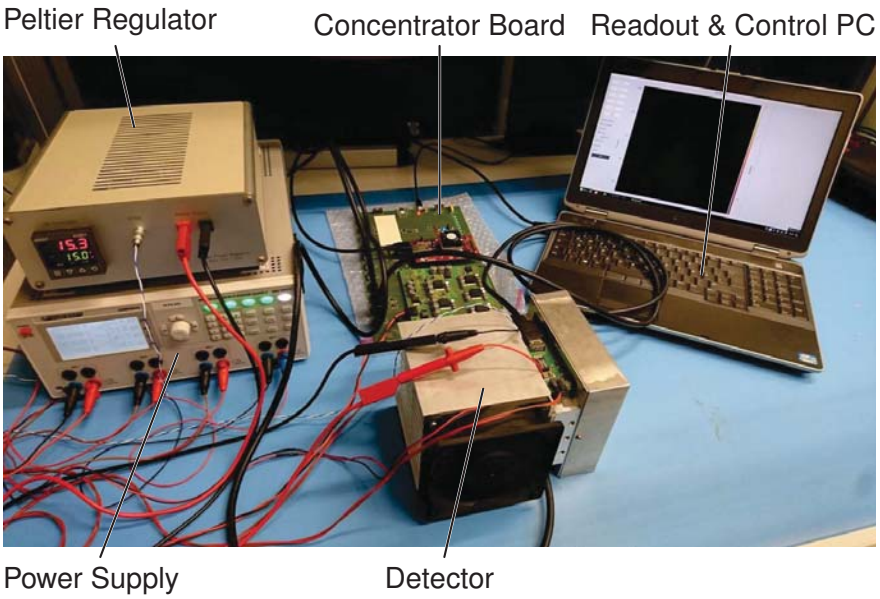
PDPC

SPAD cells:
- actively quenched
- 3200 per pixel
- digital readout

Signal:
- 4 pixels form a die
- no. of triggered SPAD cells
- timestamp via TDC



SYSTEM SETUP

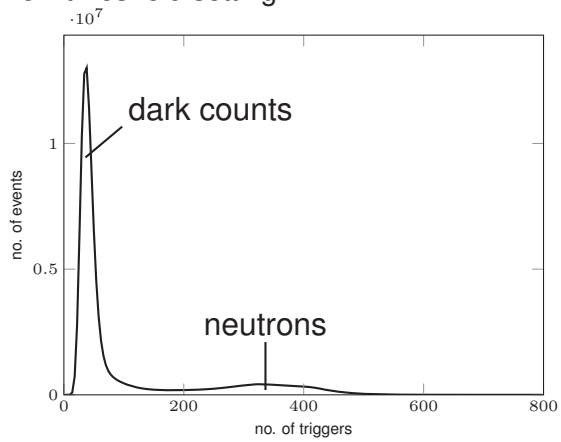


FIRST MEASUREMENTS AT TREFF

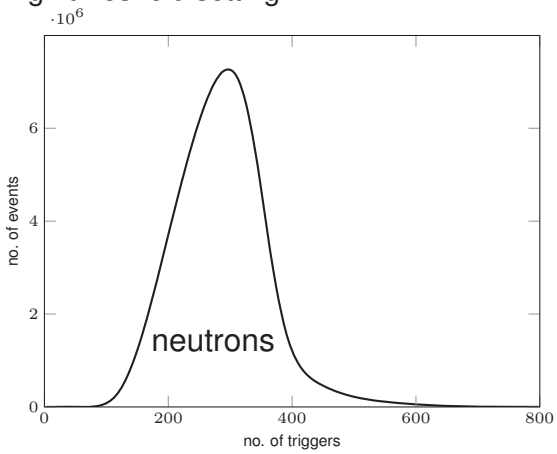
- Measurement time: 24.09.2018 – 27.09.2018
- Bug in firmware caused problems during measurement
  → Homogeneity and validation measurements could not be performed
  Bug is fixed → application for 2 additional days at TREFF
- Successful mask measurements and detection efficiency test
- In total, roughly 100 GB of data was recorded

SPECTRAL ANALYSIS

Low threshold setting



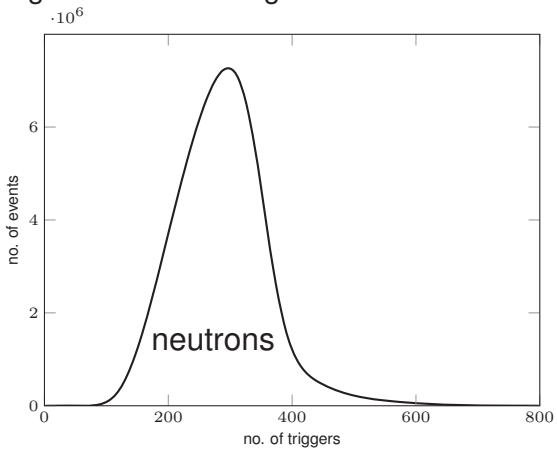
High threshold setting



SPECTRAL ANALYSIS

- Excellent dark count suppression
- Used during further measurements
- Unfortunately: also neutron events are discarded

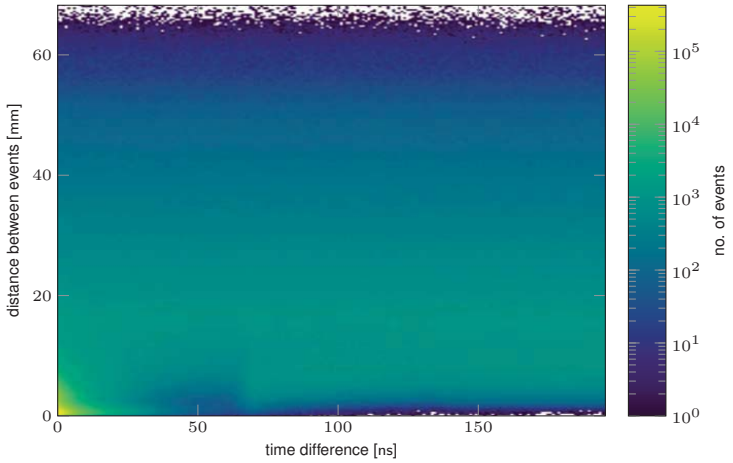
High threshold setting



Member of the Helmholtz Association 10.04.2019 Slide 6

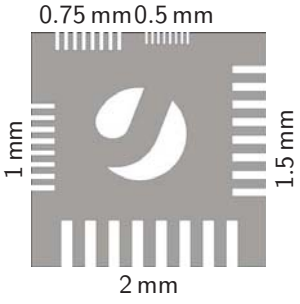
COINCIDENCE ANALYSIS

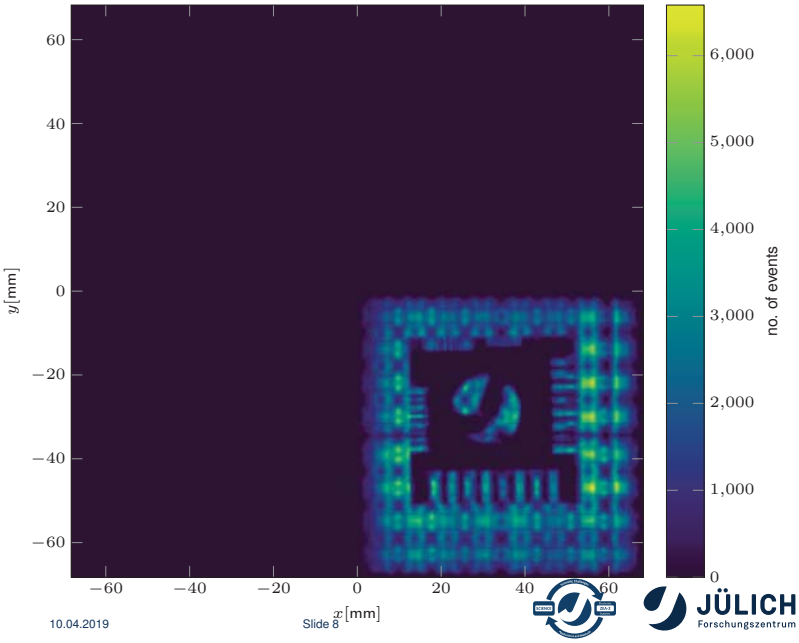
- Comparison between two sequential events
- Peak at origin: single neutron creating multiple events
- Overall rate of coincidence: 2 %
  (low because of high threshold setting)



RECONSTRUCED IMAGES

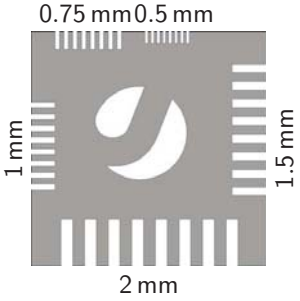
Boron carbide mask



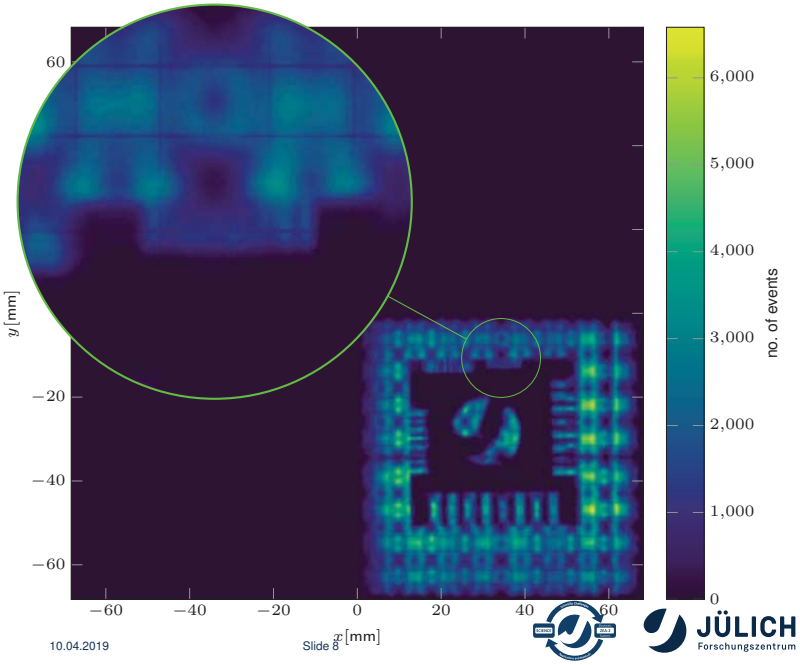


RECONSTRUCED IMAGES

Boron carbide mask



- 0.5 mm structure is visible!



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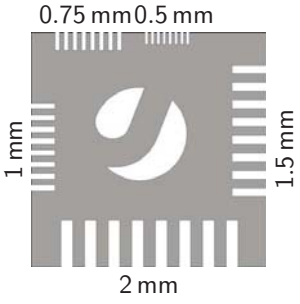
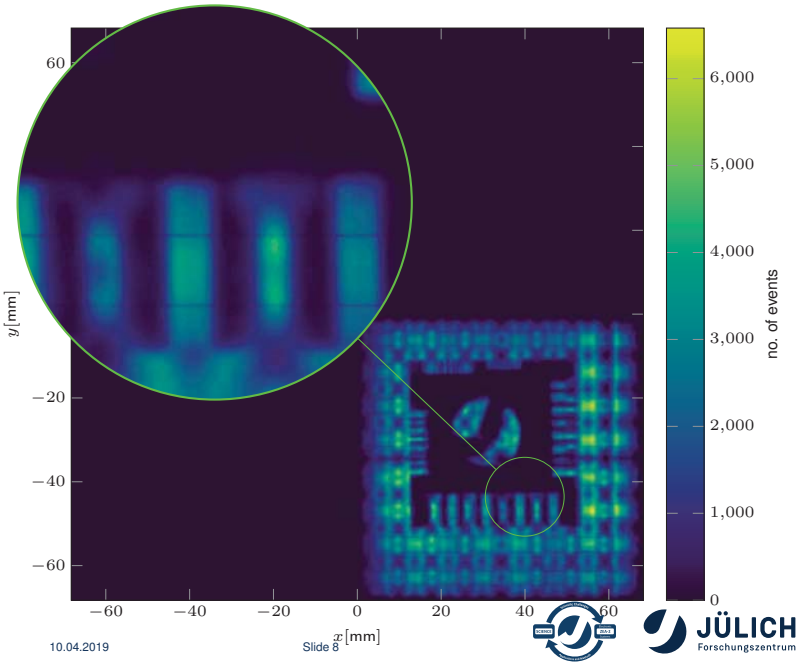
RECONSTRUCED IMAGES

Boron carbide mask



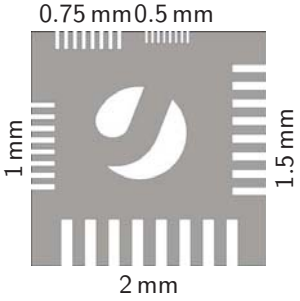
- 0.5 mm structure is visible!
- Distortion at die corners



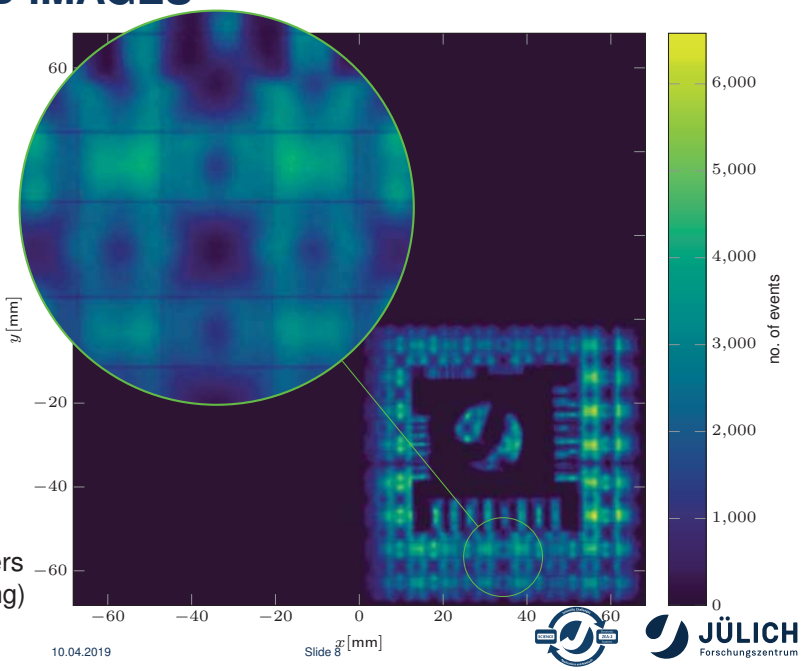
JÜLICH Forschungszentrum

RECONSTRUCED IMAGES

Boron carbide mask

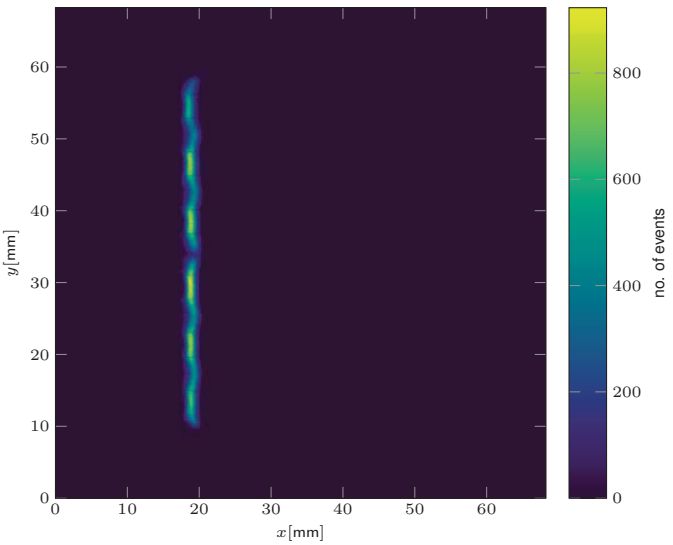


- 0.5 mm structure is visible!
- Distortion at die corners
- Low sensitivity at die corners (due to high threshold setting)

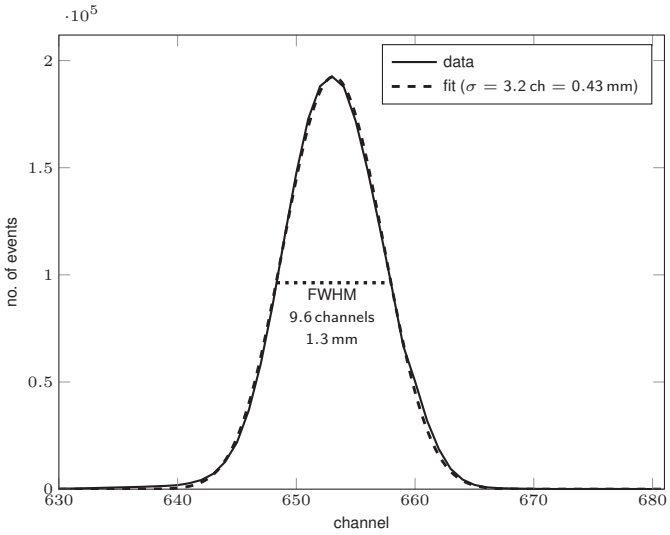


DETECTION EFFICIENCY

- Detector response to 1 mm slit aperture
- 1.97×10^6 neutrons in 129 s
  $\rightarrow$ count rate: 15.3 kcps
- Reference He-tube: 26 kcps
  Reason: low sensitivity at die boundaries due to threshold setting



1 mm SLIT RESPONSE – PROJECTION ON X-AXIS



Fit function:

$$f(x) = \int_{x_0}^{x_0+1\,\mathrm{mm}} dt\, \frac{A}{\sqrt{2\pi\sigma}} e^{-\frac{(x-t)^2}{2\sigma^2}}$$

Normal distribution convoluted with 1 mm rectangle function

CONCLUSIONS

- Prototype was partially tested
- Reconstruction algorithm still warps image at die boundaries
- Good resolution (0.5 mm structure visible, standard deviation 0.43 mm)
- Threshold setting must be lowered to increase homogeneity and thus total efficiency
- Second measurement necessary

MTCA.4 based Wire Scanner System for the European-XFEL

Timmy Lensch
DESY / MDI
SEI Tagung 2019
Jülich, 10/04/2019

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

Überblick

- Desy / MDI
- European XFEL
- Was ist ein Wire Scanner?
- Wire Scanner beim E-XFEL
- “Richtige” Hardware und Ansteuerung der Drähte
- Detekor und Auslese
- Messungen, Slow, Fast und wofür?
- Herausforderungen
- Zusammenfassung

DESY / Gruppe MDI

Deutsches Elektronen Synchrotron

MDI – Maschine Diagnose, Instrumentierung

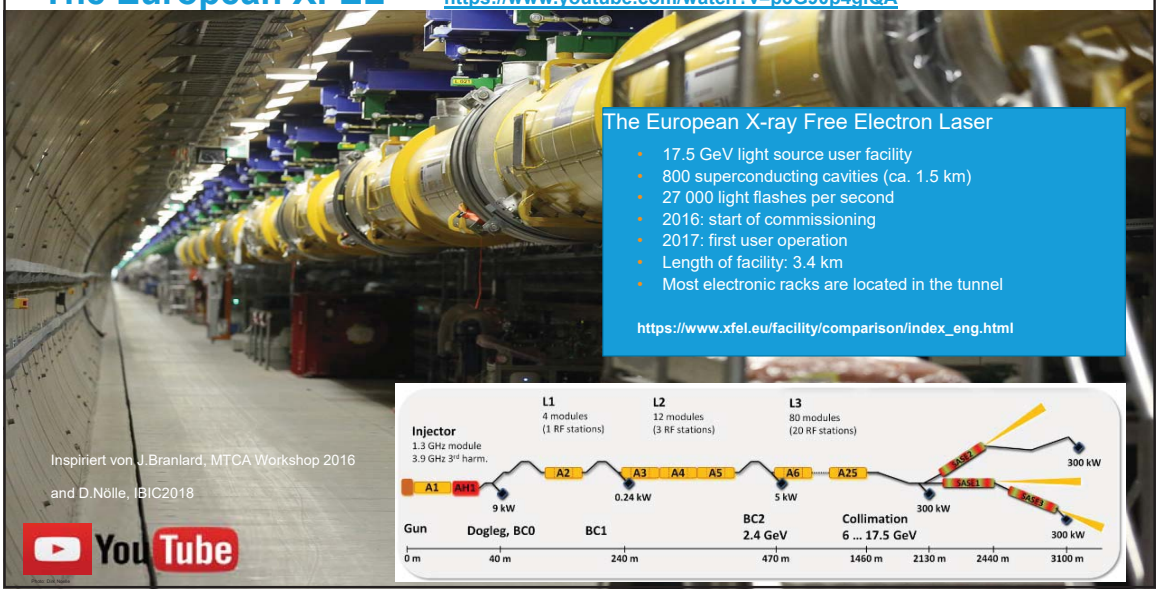
- Ca. 40 Personen (je 30% Wissenschaftler, Ingenieure, Techniker)
- (Vakuum-) Konstruktion, Elektronik+Firmware
- Installation, Betrieb und Service der Systeme

Systeme (unvollständig):

- PETRA 3, Vorbeschleuniger: Machine Protection System, Temperaturinterlock, BPM, Stahlprofil, Strommonitore, …
- XFEL: Ladungsmessung, Dosimetry, Beam Loss, Wire Scanner und optische Emittanzmessung, BPM, …

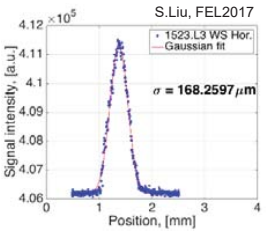
The European XFEL

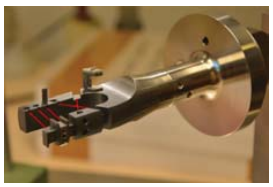
https://www.youtube.com/watch?v=p3G90p4glQA

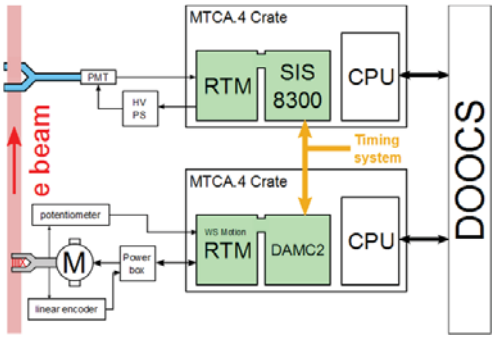


Was ist ein Wire Scanner?

Drähte an einer beweglichen Gabel im Vakuum …



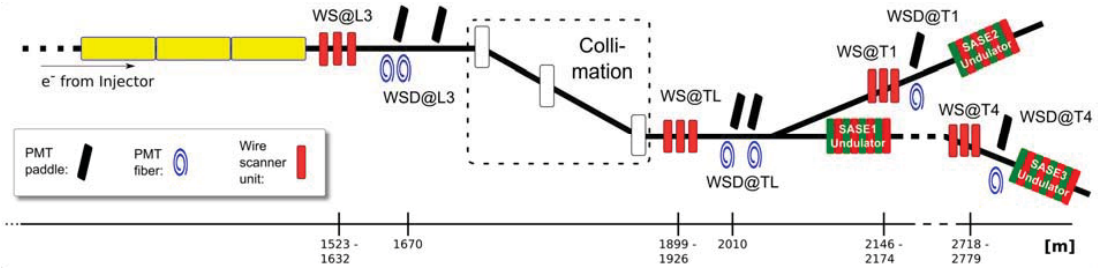




- Wolframdrähte von 50-30-20µm an einer Titan Gabel montiert
- Elektronen des Strahls erzeugen Teilchenschauer, der mit Photomultipliern (PMT) außerhalb des Strahlrohrs detektiert werden können
- Position der PMTs im Beschleuniger simuliert

Wire Scanner beim E-XFEL

An “interessanten” Positionen



- Derzeit 12 Wire Scanner Stationen im E-XFEL, je horizontale und vertikale Ebene
- Gruppen von drei Stationen mit je 2-4 Detektoren
- Detektoren: Faser um das Strahlrohr und „Paddel“ auf Photomultiplier (Philips XP2243), auch reguläre Beam Loss Monitore (sehr empfindlich)
- Weitere zwei Stationen: je eine vor SASE1 und SASE2 Undulator im Laufe 2019 (+Detektoren)

“Richtige” Hardware für die Drähte

Motor und Positionsauslese des Drahtes

Eine WS Station jeweils für horizontale und vertikale Ebene:

- **Linearmotor** mit Servoantrieb (Fa. Linmot)
  - Datenblatt: Kraft 48N (passiv gekühlt), Geschw. 3,8 m/s
  - Modifizierter Fast Trigger
- **Magnetische Federn** kompensieren die Kraft des Vauums, so ausgelegt, dass bei Ausfall des Motors die Gabel mechanisch aus dem Strahl gezogen wird
- **Fangschalter**, wenn WS Station ausgeschaltet ist wird überprüfbar sichergestellt, dass die Gabel außerhalb bleibt (muss aktiv entriegelt werden)
- **Inkrementelle Positionsauslese** mit optischer Abstastung (Fa. Heidenhain)
  - 0.5 µm Schritte
  - Relative Position (Referenzmarke)
- **Linearpoti** (50 µm Auflösung) für absolute Position (für MPS)
- Hor/Ver Station **verringert** Einfluss von **Schwingungen** der Mechanik gegenüber einer Ebene mit 45°

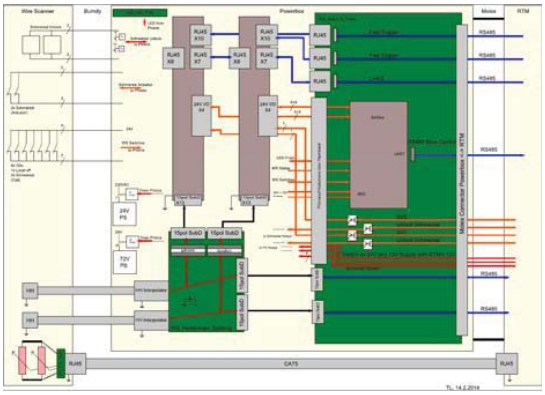
Linearmotor

Ansteuerung der Drähte

Powerbox

Eine Powerbox pro WS Station im Rack:

- Motor Servocontroller (Linmot)
- Netzteile
  - 72V Trafo für Motor
  - 24V Schaltnetzteil für Servocontroller, Endschalter …
  - Wenn WS Station nicht benutzt, ausgeschaltet (Strahlung)
- Interface zu MTCA System
- viel RS485, RJ45, SCSI Stecker 64 pol.

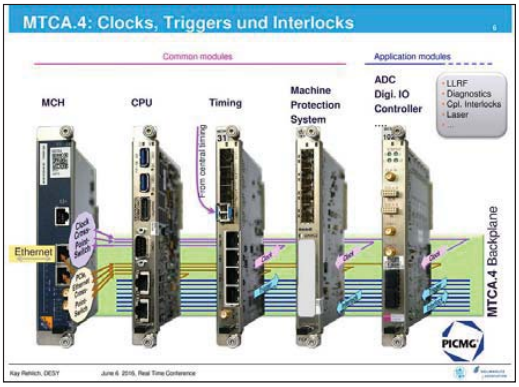


Exkurs: MTCA.4

Kontroll- / Feldbussystem für E-XFEL, FLASH, …

MTCA.4

- Crate mit CPU, Timing, Management Hub, Power Supply
- 10 User Slots:
  - vorne FPGA (ADC) Boards
  - hinten RTM für Signalanpassung
  - Für verschiedene Systeme in einem Crate
    - Machine Protection System
    - Beam Loss Monitore
    - Ladungsmessung
    - Wire Scanner
    - LLRF, Standard ADC Auslese …
- Ca. 250 Crates in E-XFEL
- DESY Systeme: Kontrollsystem DOOCS



https://www.picmg.org/openstandards/microtca/

DOOCS Referenz:
http://tesla.desy.de/doocs/doocs.html

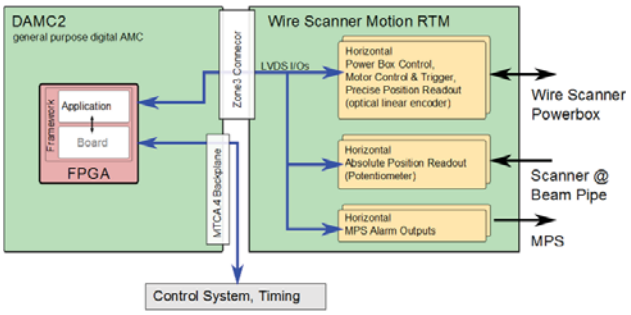
µTCA® PICMG

Drähte: Interface zu MTCA

Motor und Positionsauslese des Drahtes

Wire Scanner Motor in MTCA.4

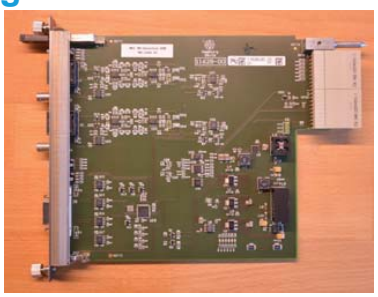
- AMC: DAMC2: Board mit Virtex5 FPGA (Gruppe FEA)
  - Firmware
    - VHDL Framework (Gruppe FEA)
    - User VHDL von MDI
      - Empfängt Trigger vom Timing System, startet Motor
      - Überwacht Drahtposition, Alarm zu MPS
      - Liest und zeichnet Drahtposition auf
      - Zugriff vom Kontrollsystem per PCIe (DMA)
- **RTM**: Entwicklung durch Gruppe MDI
  - Signalanpassungen



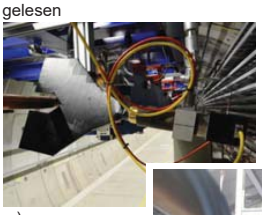
Detektorauslese: SIS8300-L2D ADC + eigenes RTM

Wire Scanner Detector in MTCA.4

- AMC: **SIS8300-L2D***, Virtex 6 FPGA, 16 Bit ADCs, 125MS/s
  - Firmware
    - VHDL Framework Gruppe MSK
    - User VHDL von MDI
      - Empfängt Trigger vom Timing System
      - Detektordaten Rohwerte und reduzierte Werte werden per PCIe/DMA vom Kontrollsystem gelesen



- **RTM**: Entwicklung durch Gruppe MDI
  - Signalanpassung von zwei Detektoren
  - Ansteuerung externes HV Netzteil

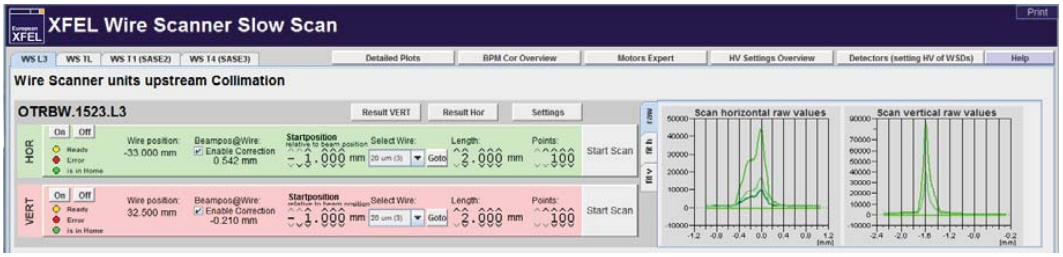


- **Detektoren**
  - Philips XP2243 (fast, 6-stages, red sensitive)
  - Hamamatsu R5505 (15-stages, red sensitive)

* wird auch für Ladungsauslese, BPM Projekte, Standard ADC Auslsese und weitere verwendet

Slow Scan

1 Bunch alle 100 ms



Den Draht langsam durch den Strahl fahren …

- Ein Elektronenbunch kommt alle 100 ms
- Draht wird langsam (z.B. 0.2 mm/s) durch den Strahl gefahren
- Messung dauert lange (z.B. 10 s)
- Wird durchgeführt beim Aufsetzen der Maschine

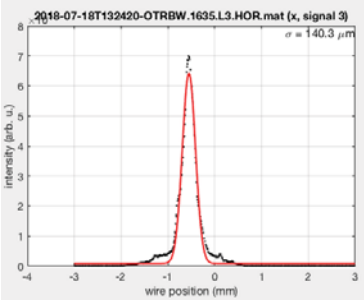
Wichtig

- Motor muss kontinuierlich fahren, kein ruckeln des Drahtes
- **Strahljitter** muss herausgerechnet werden (BPM Daten werden zeitgleich gelesen)

Und wozu jetzt?

Passt der Teilchenstrahl ins Strahlrohr? Wie ist die Verteilung der Teilchen im Bunch? Emittanz.

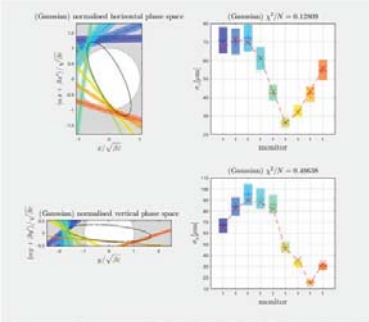
Wikipedia: Die **Emittanz** ist das Produkt aus Winkeldivergenz und Querschnittsfläche eines Teilchen- oder Lichtstrahls. Genauer bezeichnet die Emittanz das Volumen, das ein Teilchen- oder Lichtstrahl im Phasenraum ausfüllt. Der Begriff ist hauptsächlich in der Elektronenoptik und der Beschleunigerphysik von Bedeutung als **Maß für Querschnitt und Bündelung** eines Teilchenstrahls in einem Beschleuniger. …



Messung des **Beam Halo eines Bunches**, Teilchen, die am Rand „mitfliegen“, Strahlbreite

(Courtesy of Shan Liu)

1 Bunch / 100 ms



Beam Optics Matching, mit unterschiedlichen Magnetstärken und an drei WS Stationen gemessen kann die Teilchenverteilung an einer bestimmten Stelle der Maschine berechnet und mit den Designwerten verglichen werden.

(Courtesy of Matthias Scholz)

Und jetzt in schnell: Fast Scan

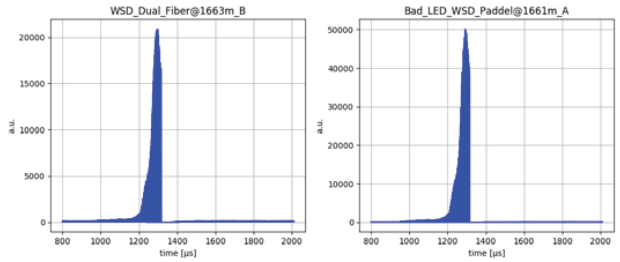
Alles in einem Bunch Train

- Bis zu 2700 Bunche / 100 ms, ~300 werden getroffen
- Bunche haben einen Abstand von ca. 1 µs
- Draht wird schnell (1 m/s) durch den Strahl gefahren
- Schnelle Messung innerhalb eines Bunchtrains
- Kann während User Run gemacht werden

Wichtig

- Motor muss mit mindestens 1 m/s fahren (sonst kann der Draht thermisch zerstört werden)
- **Orbitdrift** muss herausgerechnet werden (BPM Daten werden zeitgleich gelesen und verrechnet)
- Triggerzeitpunkt zum Motorstart muss genau eingestellt werden

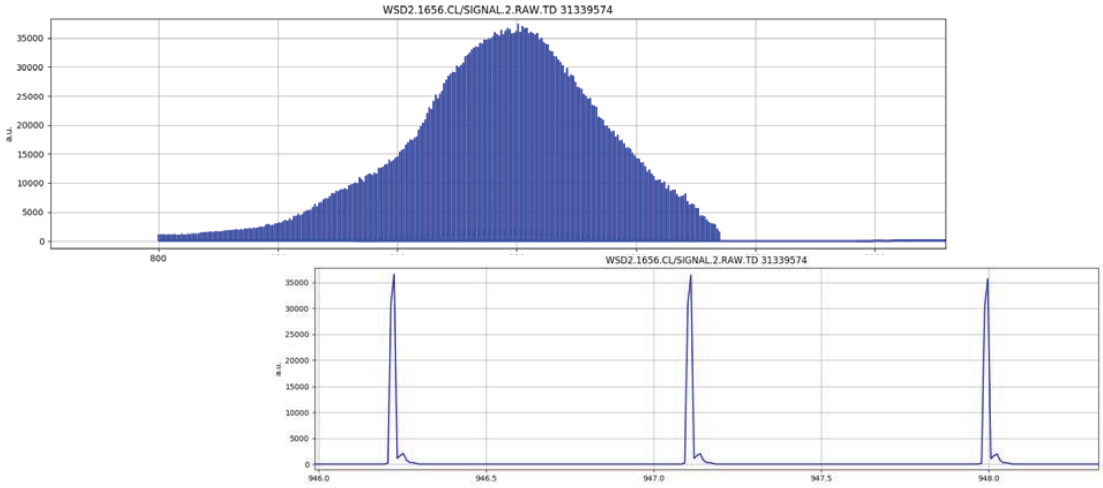
→ Wiederholgenauigkeit ~10 µm



Machine Setup:

- 500 Bunche
- 250 pC / Bunch
- Bunch Rate 1 MHz
- Bei ca. 1350 µs Bunchtrain durch Alarm geschnitten

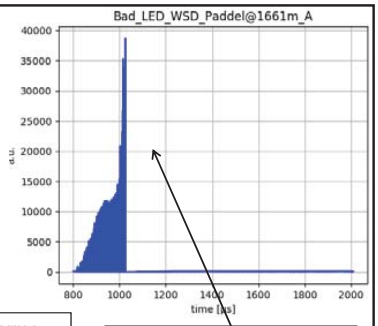
Fast Scan Messung



~~Probleme~~ Herausforderungen

Während der Inbetriebnahme …

- Beam Loss Monitore und Ladungsmonitore sehen während der Messung einen Strahlverlust
  - Erzeugt Alarme die über das Machine Protection System den Strahl abschalten
  - Fast Scan → der Bunchtrain, der gescannt wird, muss den Beam Loss Monitoren und Ladungsmonitoren über das Timingsystem angekündigt werden
  - Slow Scan → (fast) egal, aufeinanderfolgende Alarme schalten bei sehr langer Messung uU auch ab
- Vorteil: auch Beam Loss Monitore und Ladungsauslese (FW, Hardware) innerhalb der Gruppe MDI
- (Nachteil) Keine komplettes Test-Setup. Nur die Maschine.

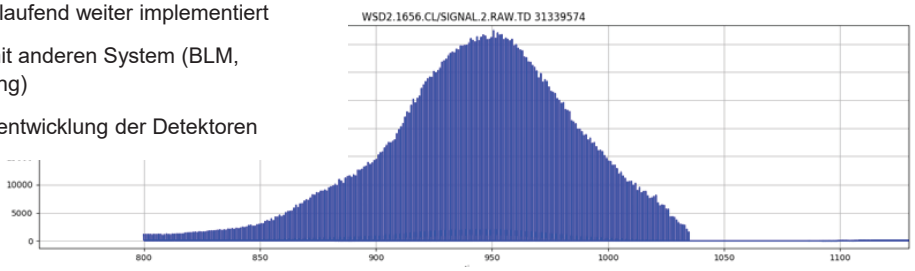


Slow Scan: Daueralarme über längere Zeit schalten auch die Maschine ab

Fast Scan: Strahl wurde abgeschnitten

Zusammenfassung

- Mechanik, Motoransteuerung, Detektor und Auslese für den E-XFEL neu entwickelt
- 12 Stationen installiert
- Integriert ins Kontrollsystem (DOOCS)
- Slow Scan mittlerweile Quasi-Standard Tool
- Fast Scan wird laufend weiter implementiert
- Eng verzahnt mit anderen System (BLM, Ladungsmessung)
- Laufend Weiterentwicklung der Detektoren



Vielen Dank!

MDI: Mechanik, Elektronik, Firmware, Installation, Inbetriebnahme, Weiterentwicklung und Service

A.Brenger
V.Gharibyan
I.Krouptchenkov
T.Lensch
D.Nölle
M.Pelzer
P.Smirnov
H.Tiessen
M.Werner
K.Wittenburg
A.Ziegler

ZE (Elektronik Werkstatt):

R.Apel

MCS4: Device-, Middlelayer Server, Kontrollsystem Support

O.Hensler

FE: DAMC2 Board, Firmware Framework und Support

Q.Sha
F.Krivan
P.Vetrov

MPY: Physics Group

S.Liu
B.Beuthner
M.Scholz

MSK: Firmware Framework SIS8300-L2D

L.Butkowski, …

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www.desy.de

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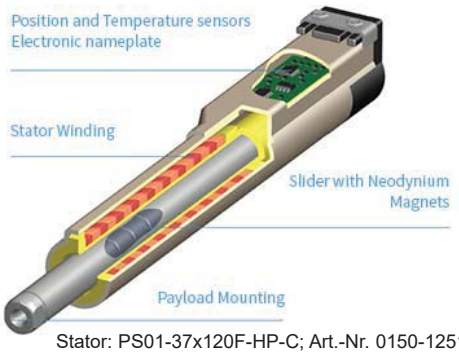
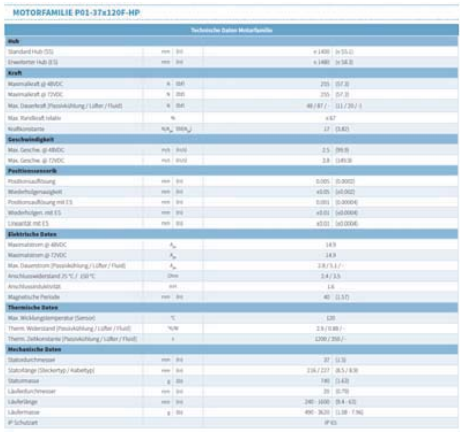
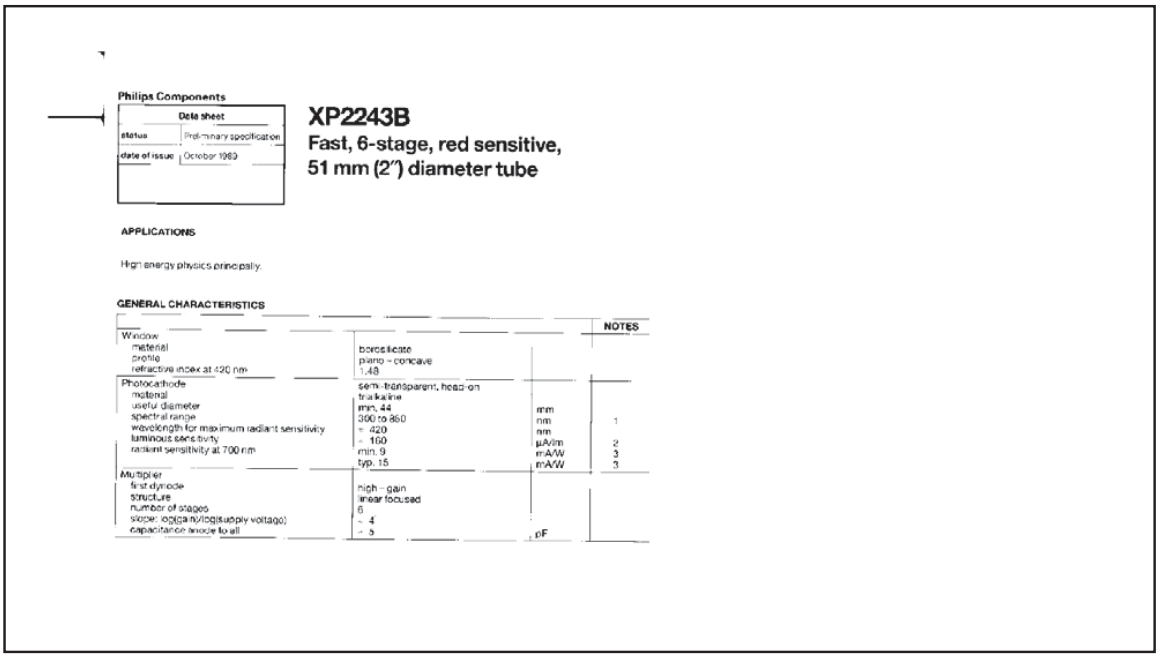


Stator: PS01-37x120F-HP-C; Art.-Nr. 0150-1251
Läufer: PL01-20x300/240-HP; Art.-Nr. 0150-1506

https://linmot.com/de/produkte/linearmotoren/

Servo Drive E1200





Philips Components

Data sheet

status: Preliminary specification

date of issue: October 1989

XP2243B

Fast, 6-stage, red sensitive, 51 mm (2″) diameter tube

APPLICATIONS

High energy physics principally.

GENERAL CHARACTERISTICS

			NOTES
Window			
material	borosilicate		
profile	plano – concave		
refractive index at 420 nm	1.48		
Photocathode	semi-transparent, head-on		
material	trialkaline		
useful diameter	min. 44	mm	
spectral range	300 to 860	nm	1
wavelength for maximum radiant sensitivity	= 420	nm	
luminous sensitivity	= 150	μA/lm	2
radiant sensitivity at 700 nm	min. 9	mA/W	3
	typ. 15	mA/W	3
Multiplier			
first dynode	high – gain		
structure	linear focused		
number of stages	6		
slope: log(gain)/log(supply voltage)	= 4		
capacitance anode to all	= 3	pF	

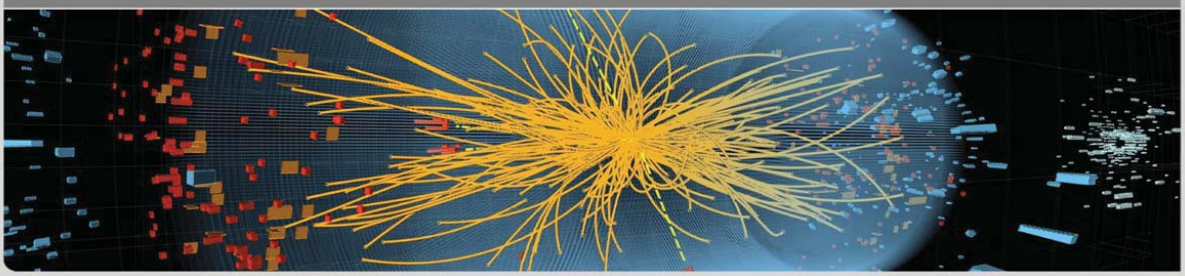
Karlsruher Institut für Technologie

HELMHOLTZ
RESEARCH FOR GRAND CHALLENGES

The HL-LHC CMS Level-1 Track Trigger

Luis Ardila

INSTITUTE FOR DATA PROCESSING AND ELECTRONICS (IPE)

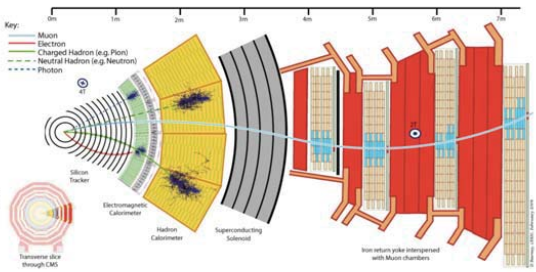


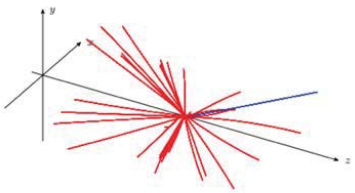
KIT – The Research University in the Helmholtz Association

www.kit.edu

HIGH LUMINOSITY LHC – CMS

- By **2026** the LHC will be upgraded in luminosity 5-7 x 10^{34} / cm^2 / s
- **Silicon** strip **tracker** will be **replaced**
- Challenging high occupancy conditions. ~10,000 charged particles per bx
- Necessary to **include tracking** information at **first level** of **triggering**



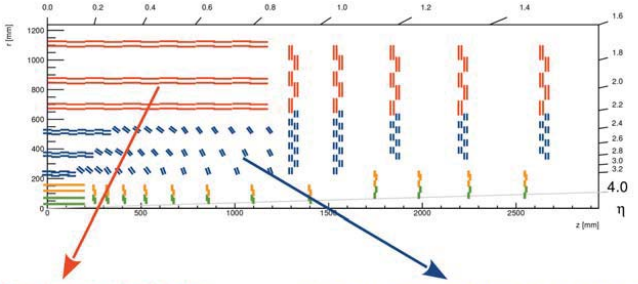


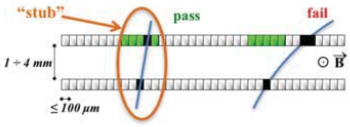
CMS TRACKER UPGRADE

Karlsruher Institut für Technologie

p_T discrimination provided by use of special modules

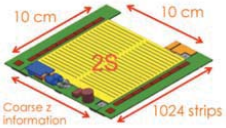
- Pairs of closely spaced silicon sensors, separated 1.6 - 4 mm
- Signals from each sensor are correlated
- Only hit pairs compatible with **p_T > 2 – 3 GeV/c ("Stubs") are forwarded off-detector**
- Factor ~10 data reduction ~12,000 stubs per bx



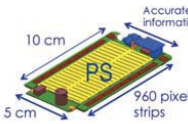


"2S" 2 Strip Modules r > 60 cm

Strip Sensor × 2:
5 cm × 90 μm
+
Strip Sensor × 2:
5 cm × 90 μm



'PS" Pixel + Strip Modules 20 < r < 60 cm



Strip Sensor × 2:
2. 5 cm × 100 μm
+
Pixel Sensor × 32:
1.5 mm × 100 μm

TRACKER → TRIGGER DATA FLOW

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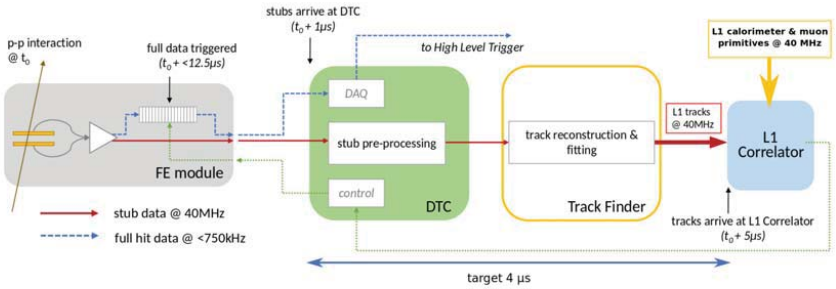


Average 15,000 stubs every 25ns (200PU) → **Stub bandwidth O(20) Tb/s**

L1 hardware trigger reduces event rate from **40 MHz to < 750 kHz** using calorimeter, muon and tracker primitives

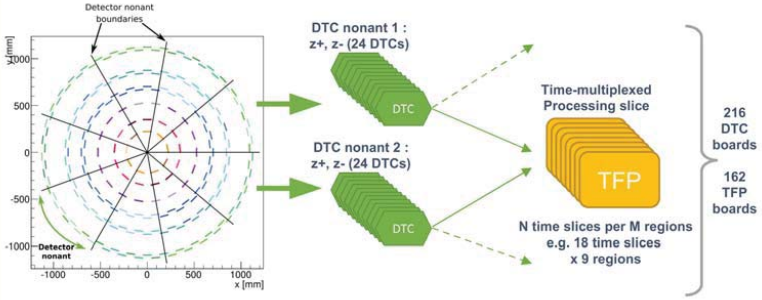
- **TK primitives are all tracks (pT > 2-3 GeV/c) from Outer Tracker**
- L1-Accept triggers all front-end buffers to read out to DAQ → HLT farm

FE L1 latency buffers limited to 12.5 μs

Transmission of stubs to BE electronics	1 μs
Correlation of trigger primitives (inc. tracks)	3.5 μs
Broadcast of L1-Accept to FE buffers	1 μs
Safety Margin	3 μs

→ Track finding from stubs must be performed in 4 μs

TRACK FINDER ARCHITECTURE



Two stages of data processing

- **DAQ, Trigger and Control (DTC) layer**
- **Track Finding Processor (TFP) layer**
- **All-FPGA** processing system
- **ATCA** form factor; CMS standard dual-star backplane

Outer Tracker cabled into **nonants**

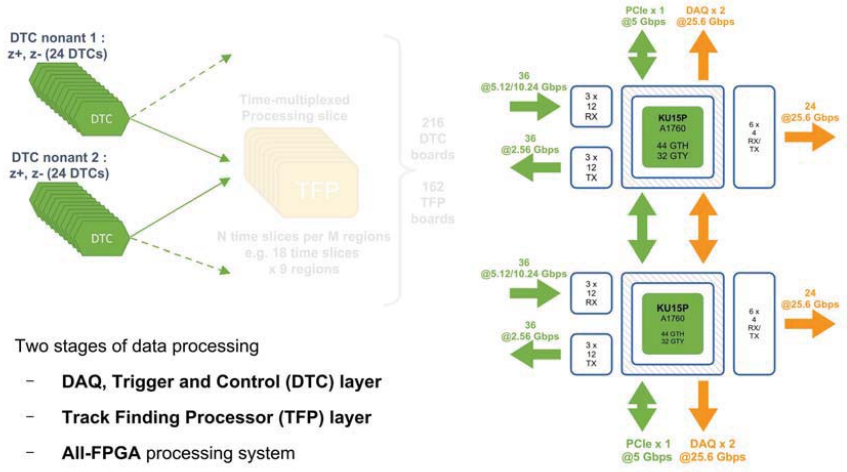
Use of time-multiplexing to increase parallelization

- Time-multiplexing directs data from multiple sources to a single processing node
- **1 event per processing node**

Processors are independent entities → simplifies commissioning and operation

Spare nodes available for redundancy

TRACK FINDER ARCHITECTURE – DTC



Two stages of data processing

- **DAQ, Trigger and Control (DTC) layer**
- **Track Finding Processor (TFP) layer**
- **All-FPGA** processing system
- **ATCA** form factor; CMS standard dual-star backplane

→ **216 DTC boards, 18 crates, 1 rack/nonant**

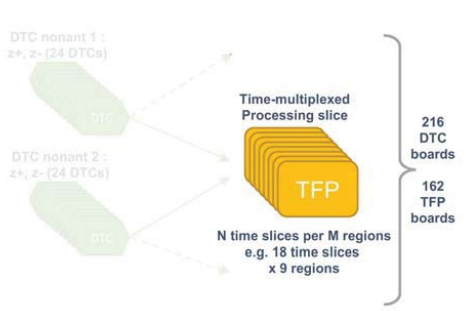
DTC card must handle

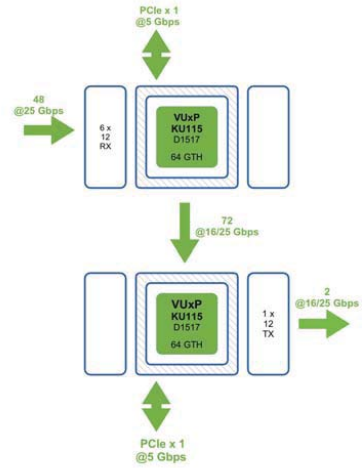
- **<=72 modules (5G/10G lpGBT opto-links)**
- Control/Readout for each module
- Direct L1 stream to central DAQ (16G/25G)
- Direct stub stream to TFPs (25G)

Stub pre-processing includes:

- **Local→ Global** look up, position calibration
- Sort and pre-duplication
- Time-multiplexing

TRACK FINDER ARCHITECTURE – TFP





TFP card must handle

- **Up to 48 DTCs (25G optical links)**
- Track Finding from stubs
- Track Fitting
- Transmission to L1 Correlator Trigger

High bandwidth processing card

- **~1 Tb/s** processing bandwidth
- Rate to L1 Correlator much lower < 30 Gb/s

Two stages of data processing

- **DAQ, Trigger and Control (DTC) layer**
- **Track Finding Processor (TFP) layer**
- **All-FPGA** processing system
- **ATCA** form factor; CMS standard dual-star backplane

→ **162 TF boards, 18 crates (one per time-node)**

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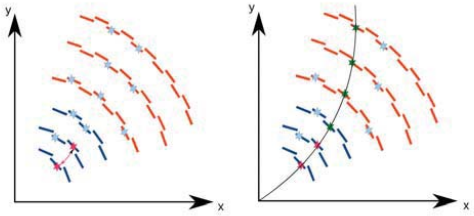
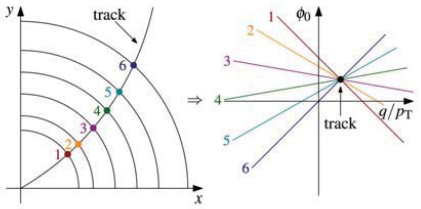
TRACK FINDING ALGORITHMS

Two main algorithms for reconstructing tracks, plus a number of hybrids, variation and options



TRACKLET + CHI2 FIT APPROACH

- Combinatorial approach using **pairs of stubs as seeds**
- **Extrapolation** to other layers → hit matching
- **Linearized χ2** fit on candidates
- Uses **full resolution stubs** at earliest stage of processing
- N time-slices x M regions → 6 x 24, 9 x 18



HOUGH TRANSFORM + KALMAN FILTER APPROACH

- Uses a **Hough Transform** to detect coarse candidates
- Candidates are filtered and fitted in a single subsequent step using a **Kalman Filter**
- Combinatorial problem pushed to latter stages of processing
- N time-slices x M regions → 18 x 9

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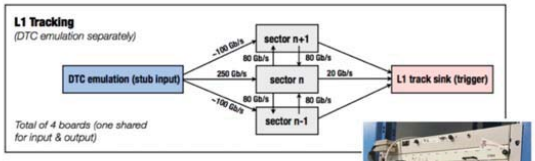
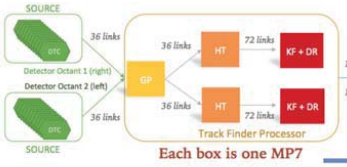
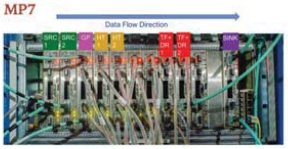
HARDWARE DEMONSTRATORS



Demonstrator in hardware, verified using emulation software





Both Demonstrators were tested with samples from PU 0→ 200

Hardware demonstrator has been built to validate the algorithm and measure latency

- 4 CTP7 boards with Virtex-7 FPGA – 3 CTP7 cover 3 Φ sectors – 1 CTP7 emulate DTC
- 1 AMC13 card for clock and synchronization
- 240 MHz internal fabric speed
- Measured latency of **3.33 µs** in agreement with latency model

Demonstrator in hardware and emulation

- One per time multiplexing and detector nonant
- Each box is one MP7 board with Virtex-7 FPGA
- Can compare hardware output directly with software
- 240 MHz internal fabric speed
- Latency verified to be **3.5 µs**

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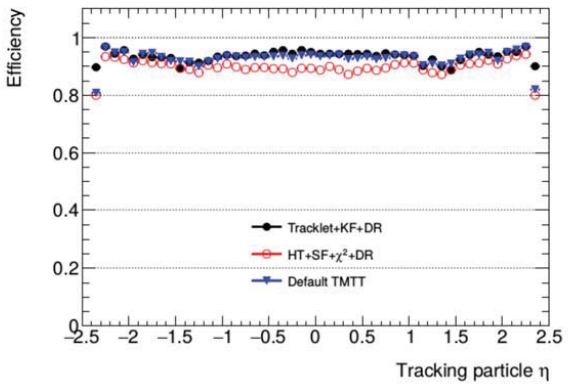
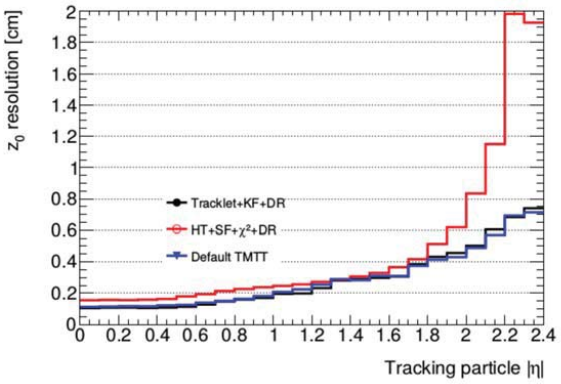
HYBRID ALGORITHMS





Efforts have started to **merge** the two approaches

- Working on defining a **reference algorithm**

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HYBRID ALGORITHMS

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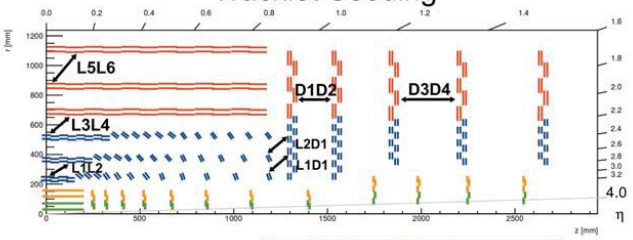
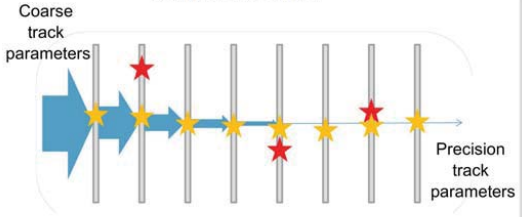
Tracklet Seeding + Kalman Filter





1. Tracklet Seeds formed in multiple layer combinations

2. Projection and match in other layers

3. Candidates sharing stubs are merged

4. Kalman Filter fits track and selects best stubs candidates

- 9 Φ sectors
- No η division
- Time-Multiplex Period of 18

HW - R&D

Bristol University, Imperial College, Ioannina, INFN, KIT, RAL, SACLAY, TIFR

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ATCA infrastructure

- Systematic **thermal studies** about air x-section and impact on opto-lifetime
- Backplane signal integrity → important for DAQ/timing

Use of **interposer technology**

- Flexibility (e.g. FPGA)
- Mitigate losses/costs due to yield issues
- Modularity; separate complex and simpler part of the board design

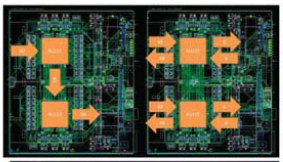
On-board computing and control variety

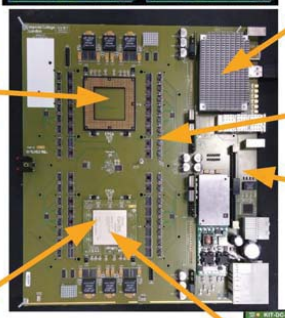
- Standard on-board PC (COM Express mini)
- ZynqUS+ SoC
- IPMC

PCB design practices, stackup and material

- Build up relationship with manufacturers

Samtec Z-RAY interposer





COM Express

Samtec Firefly x12 RX/TX pairs

CERN-IPMC

Clock test daughtercard

FPGAs
KU115
KU15P
VU9P
daughtercards

HW - R&D

APOLLO uses coplanar PCBs with Back-Plane Connectors in between

- Flexibility (e.g. FPGA+Optics)
- Modularity; separate complex and simpler part of the board design

On-board computing and control variety

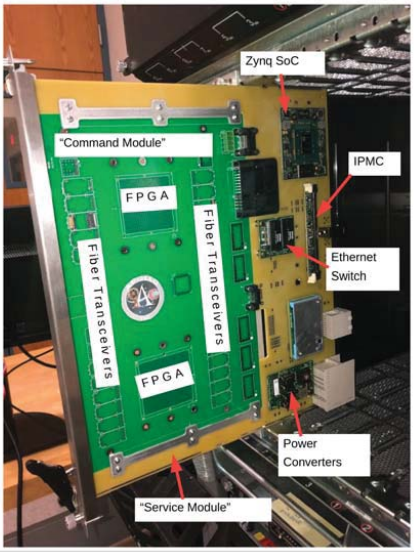
- Zynq Soc
- IPMC

Initial Tests

- Fits well in Comtel shelf
- Mechanically stable
- All major components placed

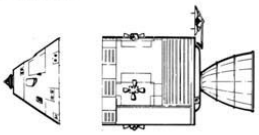
Status

- Final design boards due in 1-2 weeks



PCB Characteristics:
16 layers / Megtron-6 / 1.8 mm

Apollo analogy: Split into "Command" and "Service" modules



Boston University, Cornell University, Rutgers University, Ohio State University, University of Notre Dame, Northwestern University, University of Colorado

THERMAL SIMULATION AND TESTS

Simulation setup

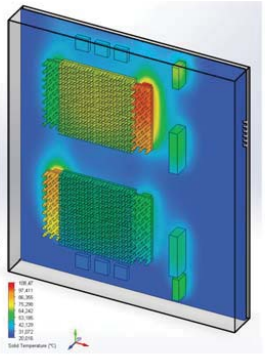
- PCB imported from PADS
- Placed in a 33 mm deep tunnel
- 4 m/s airflow from bottom (20 °C) to top

Placed components

- KU15P (50 W) doubled θ_{JB} to take interposer into account
- Firefly banks 25 G (30W) and 16 G (12 W)
- **Total power 205.4 W**

Test setup

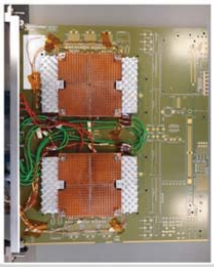
- Two heat-pads **45 mm x 45 mm** and **12 mm x 70 mm**
- Just one mockup board is present, it will be put in between two additional soon
- **~11 W for 6x block** of 16 Gbps optics
- **~10 W for 6x block** of 25 Gbps optics

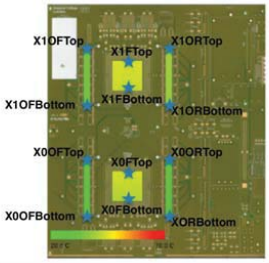


Test1 (°C)
4xFan-block speed=50%
Exhaust temp ~17°C (~amb)
Power on FPGA heaters = 86 W
Power on Optics heaters = 41 W

X1FTop = 60.7
X1FBottom = 59.1
X1ORTop = **50.8**
X1ORBottom = **49.7**
X1OFTop = 43.1
X1OFBottom = 41.7

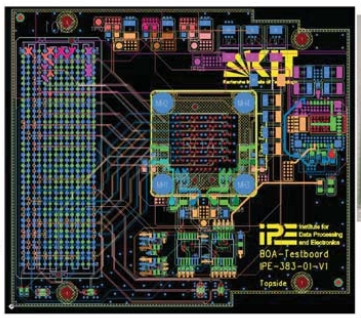
X0FTop = 53.7
X0FBottom = 50.1
X0OFTop = 35.8
X0OFBottom = 28.2
X0ORTop = 37.2
X0ORBottom = 31.1

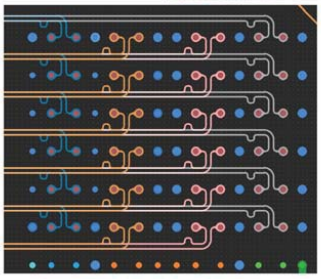


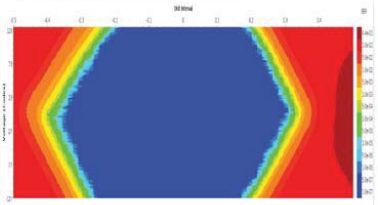


HIGH-SPEED OPTICAL EVALUATION

- FMC+ sized board for evaluation of the Finisar BOA 25 Gb/s transceiver
- 12 TX and 12 RX integrated in the same package
- 4 Electrical loop-back channels capacitively coupled with different features
- Skew < 20 µm
- MT ferrule optical interface
- Performance of capacitively coupled lanes looks good







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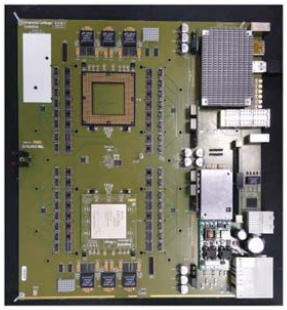
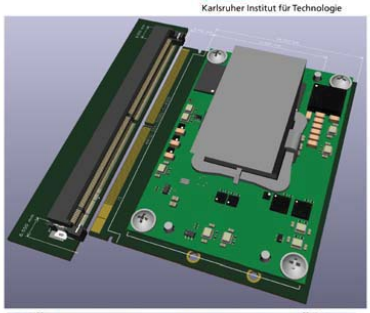
INTEGRATED BOARD MANAGEMENT

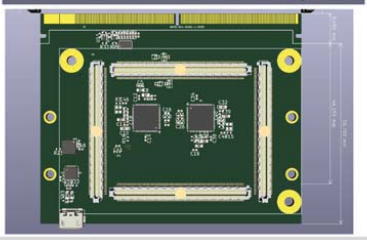
Integrate IPMC, GPP based slow control functionality and FPGA in one single heterogeneous MPSoC (Zynq Ultrascale+)

- **IPMI** in ARM-R5 processor running freeRTOS
- **TCDS** in PL-FPGA
- Xilinx Virtual Cable (**XVC**) JTAG
- **AXI C2C** slow control capable
- **I2C-SPI** to configure Optics/Clocks
- **PMBus** to configure Power Supplies

Trenz TE0803







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SUMMARY

HELMHOLTZ
RESEARCH FOR GRAND CHALLENGES

CMS needs tracks at L1 for HL-LHC pileup conditions

- p_T modules provide first layer of efficient data reduction

Two all-FPGA approaches: **Tracklet** and **TMTT**

- Use high-performance FPGAs
- Highly parallelized tracking algorithms
- Data organization → pattern recognition → track fitting → duplicate removal
- **Both have demonstrated feasibility and good performance with currently available hardware**

Efforts have started to merge the two approaches

- Working on defining a **reference algorithm**
- **Common infrastructure R&D**
  - ATCA thermal simulations and tests
  - Slow-control and shelf manager concept
  - High-speed optical link test

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METHODENPROJEKT: „GIGABIT SERIAL INTERFACES“

Gbit Ethernet

Dec. 2018 | Dr. H. Rongen (G. Schardt)

Background: Development of Methods

Many projects need high speed interfaces
- BrainPET (and other PET); pnCCD, PANDA_x, Sonde, GLORIA / AtmoSat, ….

Ethernet is „de-facto“ standard
- Gigabit Ethernet
  - Interfaces: GMII, RGMII, SGMII, XAUI, SFP-optical links, …
  - Protocols: UDP, TCP, ARP, ICMP, …

Aim of the project
- TCP/IP on FPGA without CPU
- Feasibility study & Market analysis
- Development of Test-Cases and demonstrators (based on commercial Evaluation boards)
- Generate Repositories and Libraries
- Building Blocks for future projects
- Documentation

Mitglied der Helmholtz-Gemeinschaft

JÜLICH Forschungszentrum

Diversity of interfacing standards …

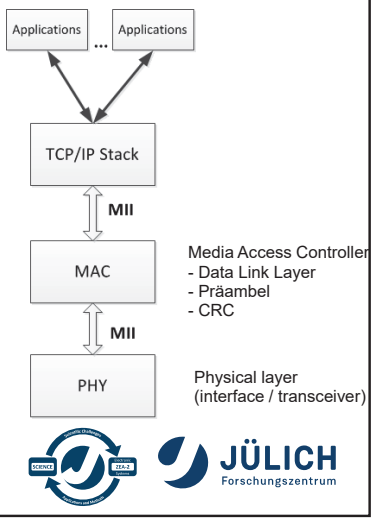
https://en.wikipedia.org/wiki/10_Gigabit_Ethernet#SFP+_Direct_Attach

1 Standards
2 Physical layer modules
3 Optical fiber
3.1 10GBASE-SR
3.2 10GBASE-LR
3.3 10GBASE-LRM
3.4 10GBASE-ER
3.5 10GBASE-ZR
3.6 10GBASE-LX4
3.7 10GBASE-PR
3.8 Bi-Directional Single Strand
4 Copper
4.1 10GBASE-CX4
4.2 SFP+ Direct Attach
4.3 Backplane
4.3.1 10GBASE-KX4
4.3.2 10GBASE-KR
4.4 10GBASE-T
5 WAN PHY (10GBASE-W)

Ethernet Class	Copper Spec.	Fiber optic Spec. (*1)	
10 MbE	10Base-T		Copper: 10 Mb/s Single LVDS for each direction
100 MbE	100Base-TX		Copper: 4B/5B encoding, 125 Mb/s, Single LVDS for each direction
1 GbE	1000Base-T		Copper: PAM-5 TCM coding , 125 Mb/s Two LVDS for each direction Fiber: 8b/10b Codierung,
10 GbE	10GBASE-T 10GBASE-Cx 10GBASE-Kx	10GBase-R	Copper: PAM-16 DSQ128 coding, 833.3 Mb/s Two LVDS for each direction Fiber: 64b/66b encoding, 10.3125 Gb/s
25 GbE	--	25GBase-R	Fiber: 64b/66b encoding, 25.78125 Gb/s
40 GbE	--	40GBase-R	Fiber: 64b/66b encoding, 10.3125 Gb/s 4 x 10 Gb lanes
100 GbE	--	100GBase-R	Fiber: 64b/66b encoding, 10.3125 Gb/s 4 x 25 Gb lanes

Media Independent Interface(s)

MII	100 Mb	8 bit @ 12.5 MHz, SDR
RMII		4 bit @ 25 MHz, SDR
GMII	1 Gb	8 bit @ 125 MHz, SDR
RGMII		4 bit @ 125 MHz, DDR
XGMII	10 Gb	64 bit @156.25 MHz, SDR
XAUI		4 x 3.125 GHz



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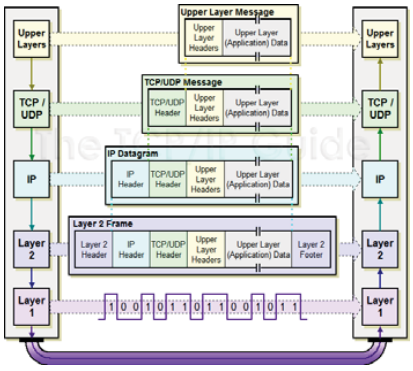
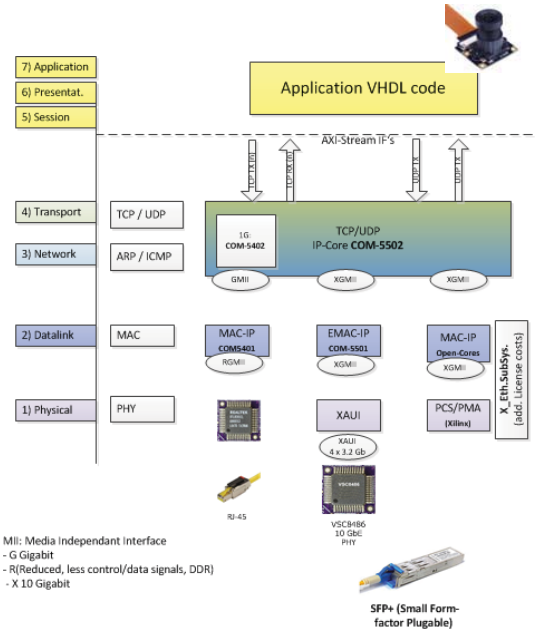
OSI model (7 layer model)





Mitglied der Helmholtz-Gemeinschaft

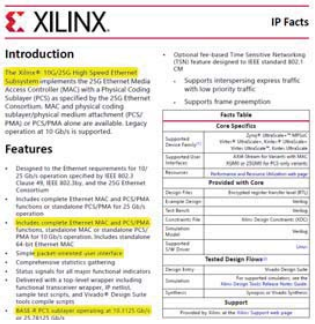
PHY

- **PCS Physical Coding Sublayer**
  - Encoding (8b/10b or 64b/66b)
  - **Serializer**
- **PMA Physical Medium Attachment**
  - Voltage / Current drivers for Physical interface

1) as external PHY component

https://en.wikipedia.org/wiki/Physical_Coding_Sublayer
https://www.xilinx.com/support/documentation/ip_documentation/xxv_ethernet/v2_4/pg210-25g-ethernet.pdf

2) IP-Core



Licensing:

10G/25G Ethernet PCS/PMA (10G/25G BASE-R)
… is provided at no additional cost with the Xilinx® Vivado Design Suite under the terms of the Xilinx End User License.

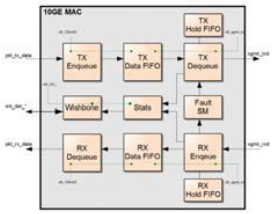
10G/25G Ethernet MAC require separate fee-based licensing ...

MAC

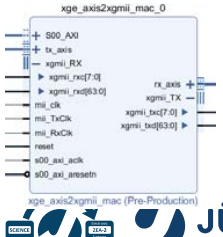
OpenCores: **'xge_mac'**
- implements the Media Access Control functions
- for 10Gbps operation
- XGMII Interface (64-bit single clock edge)
- Inter-Frame GAP (Deficit Idle Count per Clause 46)
- Pause Frames (filtering, Indication, …)
- Link Status
- Fault Detections

https://opencores.org/projects/xge_mac

VHDL/Verilog
Source code
→
IP-Core



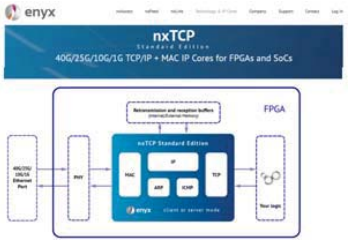
→
IP-Block
for Vivado IPI



Market analysis: TCP/IP Cores for FPGA's

- Vernetzung im industriellen Umfeld, für Echtzeit-Automatisierung und Prozesssteuerung EtherCAT, PROFINET, POWERLINK, Modbus TCP,...)
- Maschine Vision / Multi-Kamera-Überwachung (z. B. GigE Vision)
- Test & Measurement Konnektivität
- Netzwerkspeicher, wie iSCSI
- elektronischer Handel, Financial Information eXchange (FIX)-Protokoll

Info only after NDA (~20 k€)



The Expert of IP Core & Embedded
DESIGN GATEWAY

https://www.dgway.com/products/IP/IP-LF-V2.3EX.pdf

the pricing information:
TOE1G-IP core: 28,000USD
TOE10G-IP core: 42,500USD
[License condition]
* Single Project encrypted netlist license.
…

INTILOP
A Leader in TCP Offload Technology & Products.

http://www.intilop.com/

- one board locked Lic of $14K…
- plus $9K for project specific integration

easics TCP/IP-Core

Mitglied der Helmholtz-Gemeinschaft

JÜLICH Forschungszentrum

ComBlock: TCP / IP cores

www.comblock.com

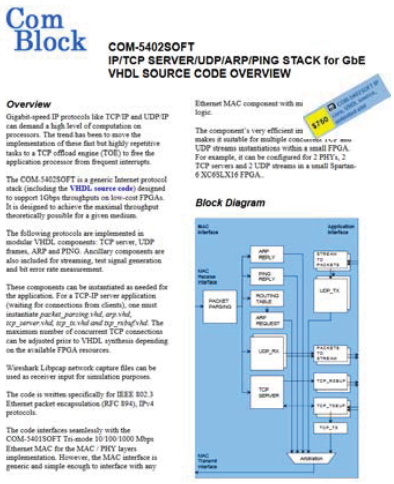
Internet Protocol IP-Block
- TCP, UDP
- ARP, ICMP (Ping)
- VHDL source

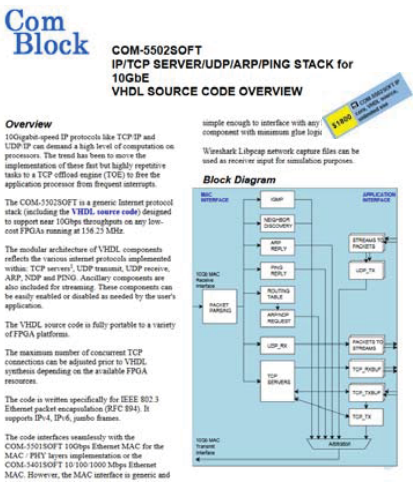
Licensing:
A nonexclusive, nontransferable, corporate/organization license to use the VHDL source code internally,

An unlimited, royalty-free, nonexclusive, transferable license to make and use products incorporating the licensed materials, solely in bitstream format, on a worldwide basis

https://www.comblock.com/product_list_IP.html

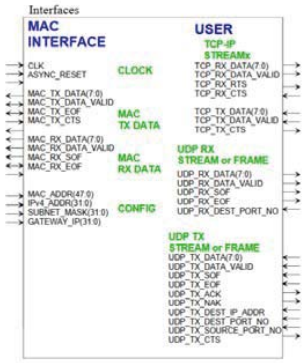
Mitglied der Helmholtz-Gemeinschaft





1G Prozessor-less Ethernet

ComBlock Tcp/IP-Core



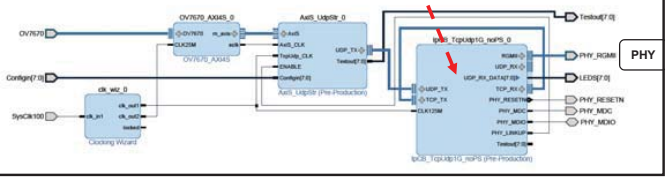
VHDL Source code

```
MacAdr48b     <= x"010203040506";

cUDP:  entity work.IpCB_TcpUdp
       generic map
       (
          CLOCKFREQMHZ  =>  TCPCLKFREQMHZ,
          NTCPSTREAMS   =>  NTCPSTREAMS
       )
       port map
       (
          CLK125M             => CLK125M,
-- Basic Configuration
          ControlWORD         => x"00000001",
          MyMACaddr           => MacAdr48b,
          MyIP                => x"c0A80302",
          MyGatewayIP         => x"c0A80301",
-- TCP Config
          TCP_LOCAL_PORT      => x"00000400",
-- Status Register
          StatusSel           => "0000",
          StatusData          => open,
-- UDP Configs
          UDP_TxDestIP        => x"C0A80306",
          UDP_TxDestPort      => x"0400",
          UDP_TxSourcePort    => x"0400",
```

FPGA Resources:
- No special functionalities
- Just „normal logic“
- @ 125 MHz
- can be implemented on „any normal FPGA“
- Spartan, Virtex, Kintex, Artix, …

as IP-Block in IPI



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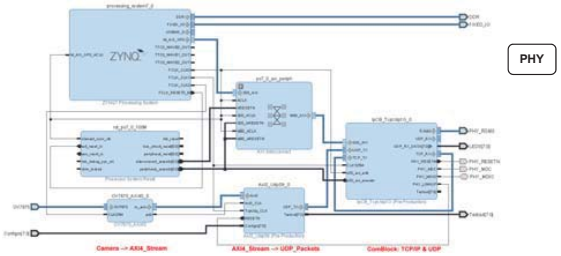
or with AXI Interface for Configuration (only !!!)

Using the ZYNQ processor PS:
- Vivado IP-Block with AXI Interface
- Setup of Network parameters via SW
- Comfortable Configuration

```
int main()
{
int Status, tcpRxBytes, tcpTxBytes, udpRxBytes, udpTxBytes, udpTxBytesLast, UdpFramesOK, UdpFramesNOK;
u32  IpAdr, IpGatew;
u8   MacAdr[6] = { 0x00, 0x0a, 0x35, 0x00, 0x01, 0x02 };

   printf("Hello World\n\r");


   IpAdr   = IP4_ADDR(192,168,3,2);
   IpGatew = IP4_ADDR(192,168,3,1);
   IpCB_TcpUdp_Init (MacAdr, IpAdr, IpGatew, 2222);

   IpCB_TcpUdp_UDP (IP4_ADDR(192,168,3,6), 1024, 1024);

   while (1)
   {
      Status  = RdStatusReg (0);
      tcpRxBytes  = RdStatusReg (8);
      tcpTxBytes  = RdStatusReg (9);
      udpRxBytes  = RdStatusReg (10);
      udpTxBytes  = RdStatusReg (11);
      UdpFramesOK  = RdStatusReg (12);
      UdpFramesNOK = RdStatusReg (13);

      printf ("Status: %02x   TCP_Rx:%d  TCP_Tx:%d UDP_Rx:%d  UDP_Tx:%d (%d KB) \n", Status, tcpRxByte
                              udpRxBytes, udpTxBytes, ((udpTxBytes-udpTxBytesLast)/1024) );
      printf ("UdpFrames OK: %d   NotOK: %d \n", UdpFramesOK, UdpFramesNOK);
      udpTxBytesLast = udpTxBytes;

      sleep(1);
   }
   return 0;
}
```

FPGA Resources:
- No special functionalities
- Just „normal logic“
- @ 125 MHz
- can be implemented on „any normal FPGA“
- Spartan, Virtex, Kintex, Artix, …

- but a processor (MicroBlaze, ARM, …)



Mitglied der Helmholtz-Gemeinschaft

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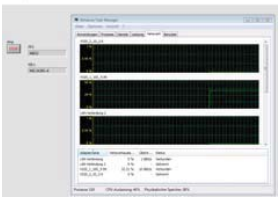
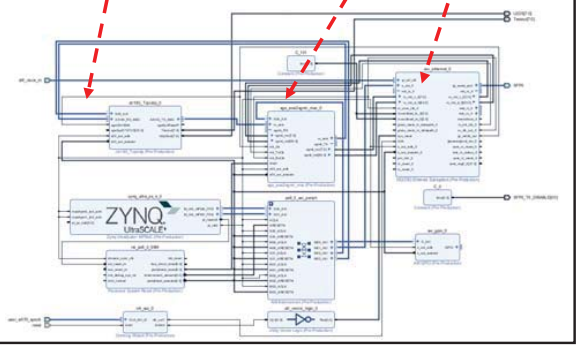
10 G Ethernet

implemented on ZCU102; ZYNQ Ultrascale+
- based on 10/25G Ethernet Subsystem
- PHY: internal GTH Serializer (10.3125 Gbit/sec)



FPGA Resources:
- Gigabit Serializer needed (GTY, GTH, …)
- Kintex, Artix, Ultrascale+, …
- On Spartan with external XAUI Interface

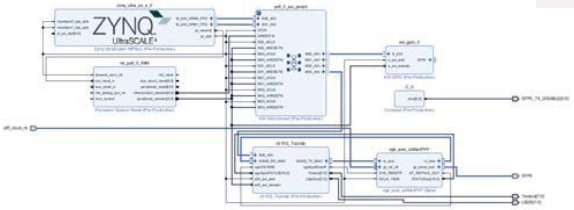
Layer / Function	Product name	IP-Integrator Block
Network / Transport Tcp/Udp Stack	ComBlock COM-5502 (Server)	cb10G_TcpUdp
Link Layer MAC	OpenCores Ethernet 10GE MAC (xge_mac) https://opencores.org/project/xge_mac	xge_axis2xgmii_mac
Physical Layer PCS/PMA	Xilinx 10G/25G High Speed Ethernet Subsystem	xxv_ethernet_0



Mitglied der Helmholtz-Gemeinschaft

Next Step: Application board

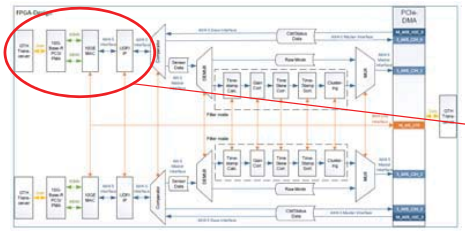
TE0808-ZU6EG
52 x 76 mm



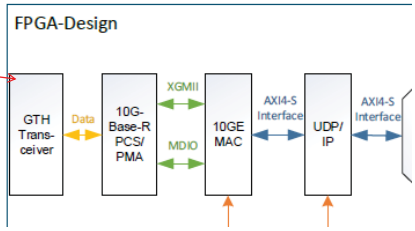
→ application specific baseboard

Compact, Ruggedized, SFP+

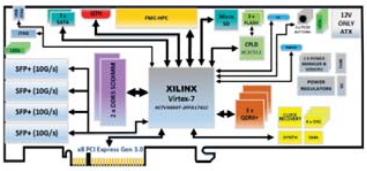
First User: BrainPET (Sebastian Völkel)



BrainPET DAQ System
- Two 10 Gbit Ethernet Interfaces



On a ‚NetFPGA-SUME' board



Mitglied der Helmh

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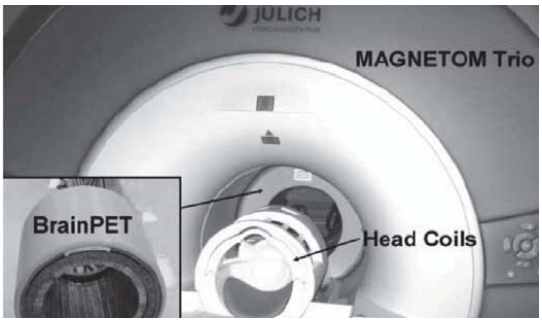
SEI-TAGUNG 2019

ANWENDUNG DES 10G BASE-R ETHERNET UDP/IP SYSTEMS IM PROJEKT BRAINPET

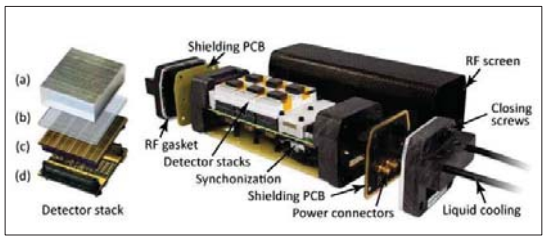
09.04.2019 I SEBASTIAN VÖLKEL

BRAINPET 9T

Einführung



BrainPET im 3T MR Scanner [1]



Detektormodule [2]

BRAINPET 9T

Einführung

Maximum Transmission Payload Bandwidth per SPU

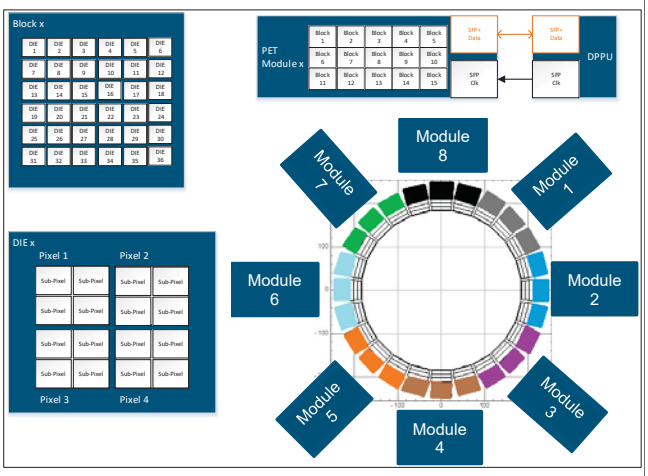
- One SPU consists of 15 Tiles/Blocks
- Each Tile have 6*6 DIEs = 36 DIEs
- 1 Hit produced 112 Bit data
- 96960 Hits/DIE/s
- 1 Tile = 96960/s * 112 Bit * 36 DIEs = ~390.94 Mbit/s
- 1 SPU = 15 * 390.94 Mbit/s = 5.8642 Gbit/s

Total Maximum Transmission Payload Bandwidth

- 8 SPUs = 8 * 5.8642 Gbit/s = 46.9136 Gbit/s

Transmission Protocol

OSI-Layer	Protocol
Physical & Data Link	10GBit-Ethernet (10GBASE-SR)
Network	IP
Transport	UDP



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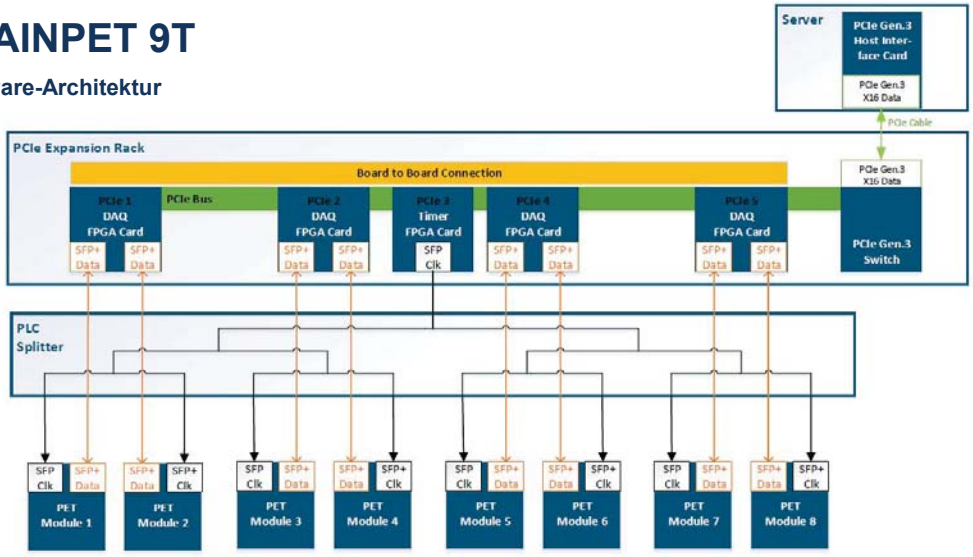
Hardware-Architektur



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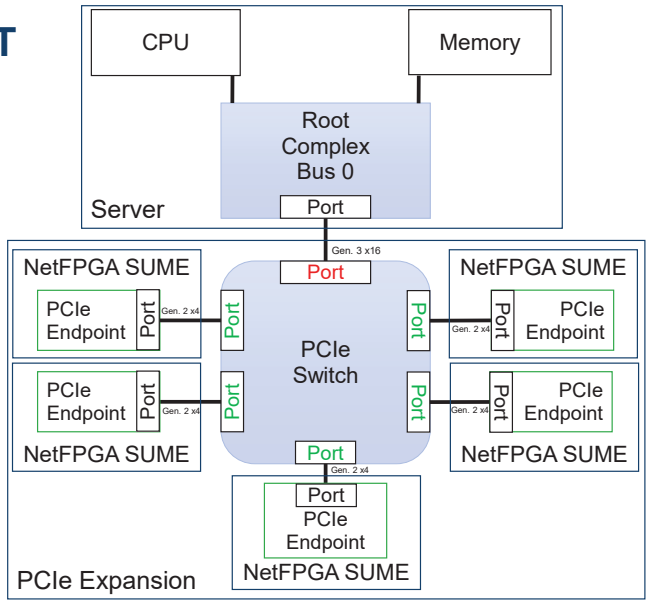
PCI-Express Topologie



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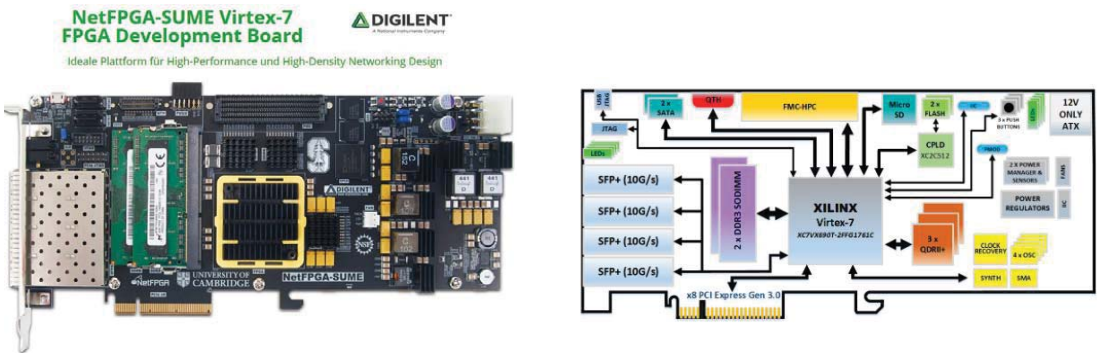
BRAINPET 9T

DAQ-Karte



NetFPGA-Sume DAQ-Karte [3]

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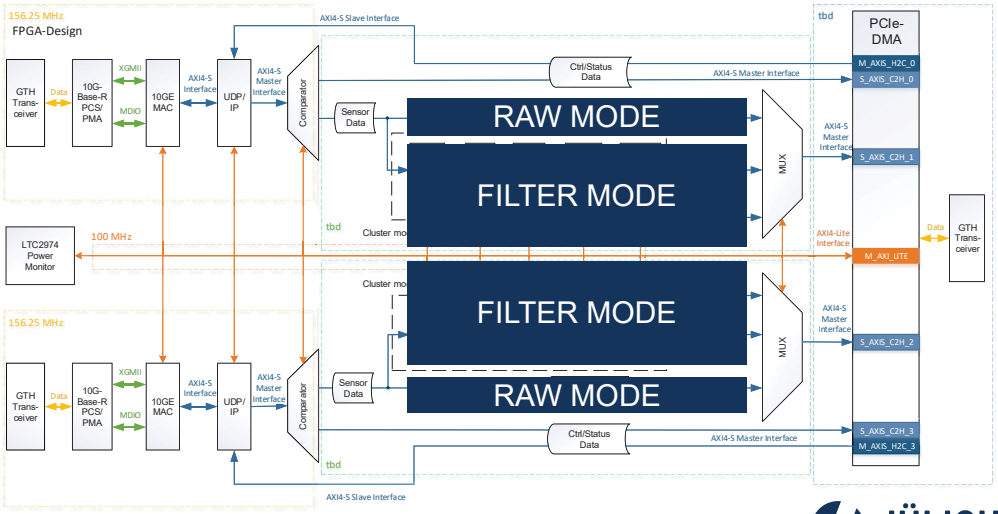
BRAINPET 9T

Firmware



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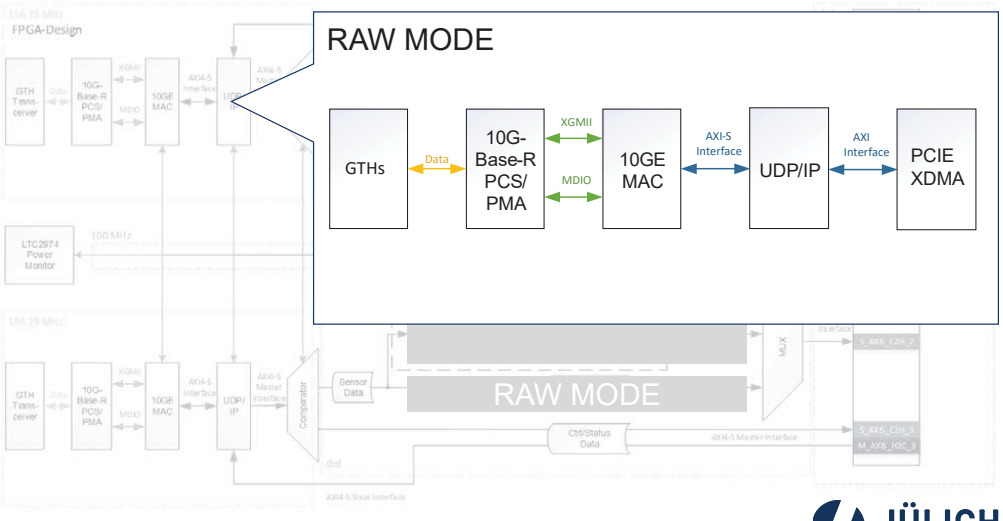
BRAINPET 9T

Firmware



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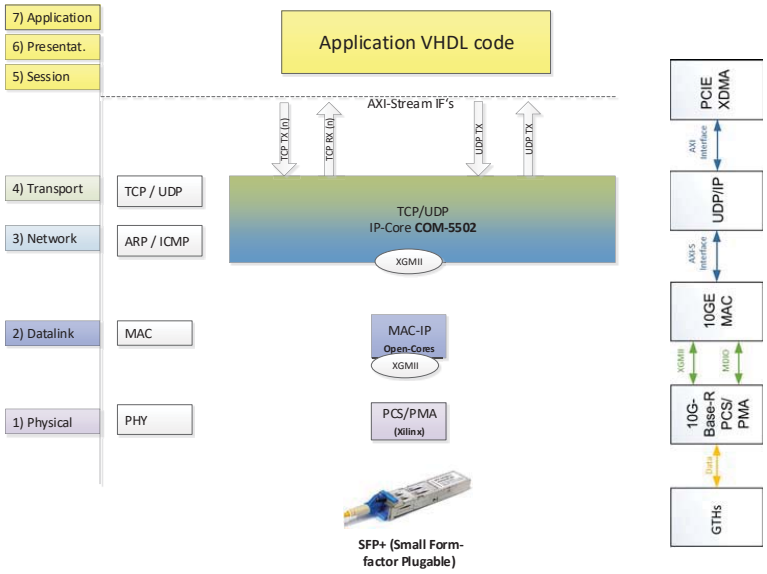
BRAINPET 9T

OSI-Layer Cores



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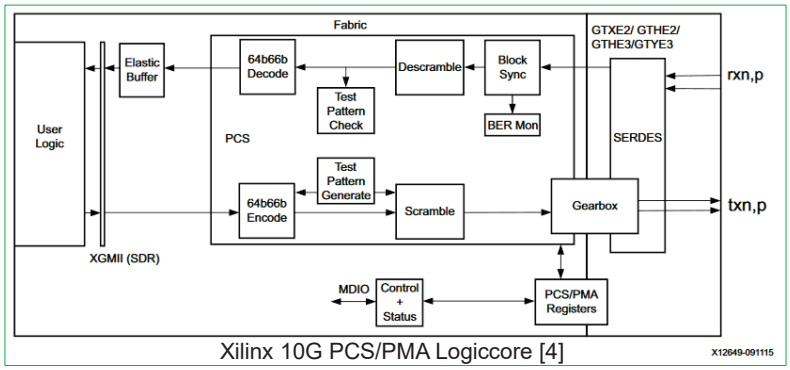
BRAINPET 9T

PHY



Xilinx 10G PCS/PMA Logiccore [4]

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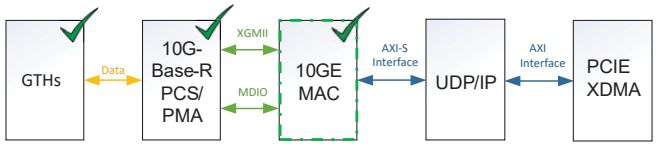
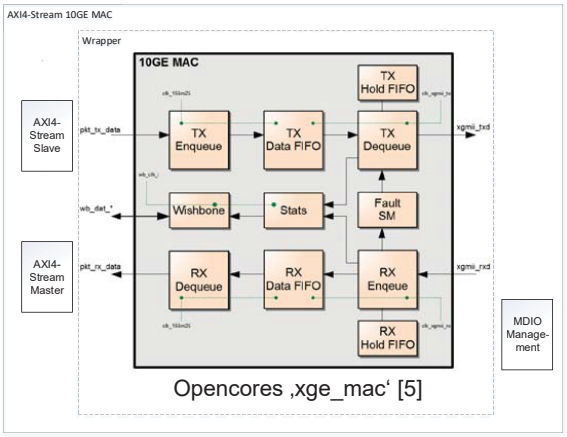
BRAINPET 9T

AXI4-Stream 10GE MAC





Opencores ‚xge_mac' [5]

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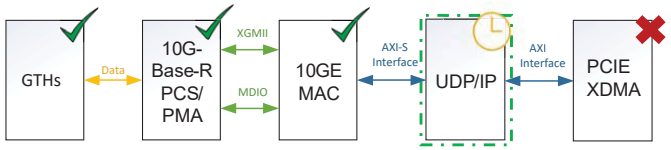
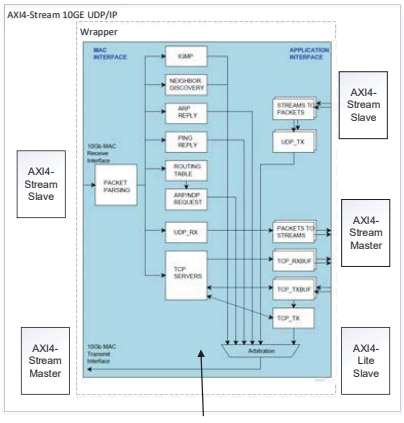
BRAINPET 9T

AXI4-Stream 10GE MAC





ComBlock ‚10G TCP:UDP/IP Core ' [6]

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QUELLEN

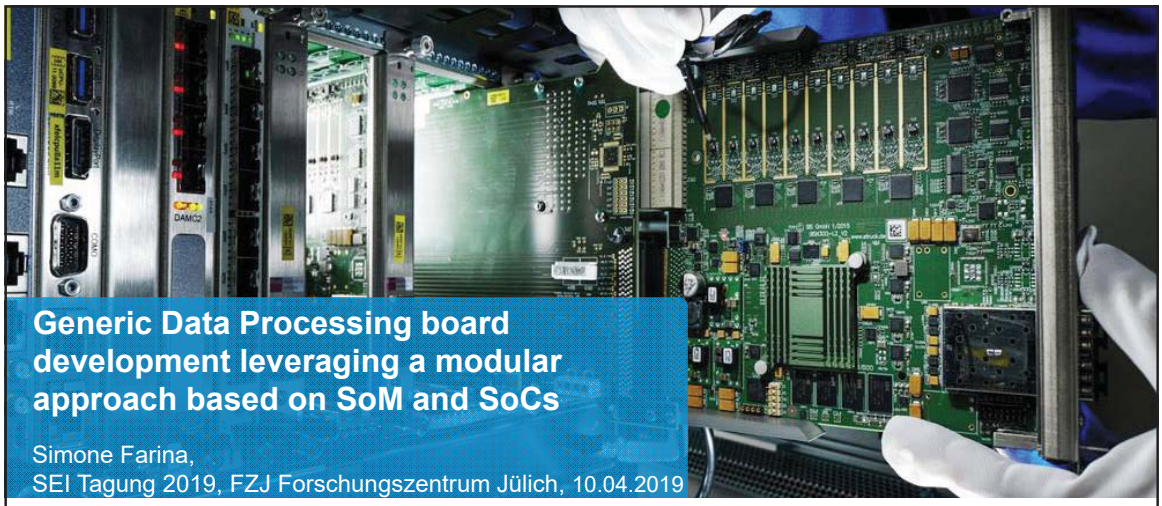
[1] Herzog H, Langen KJ, Weirich C, Rota Kops E, Kaffanke J, Tellmann L, Scheins J, Neuner I, Stoffels G, Fischer K, Caldeira L, Coenen HH, Shah NJ. High Resolution BrainPET Combined with Simultaneous MRI. Nuklearmedizin/NuclearMedicine 2011 50(2) 74-82.

[2] Bjoern Weissler, Pierre Gebhardt, Peter M. Dueppenbecker, Jakob Wehner, David Schug,Christoph W. Lerche, Benjamin Goldschmidt, Andre Salomon, Iris Verel, Edwin Heijman,Michael Perkuhn, Dirk Heberling, Rene M. Botnar, Fabian Kiessling, and Volkmar Schulz. A Digital Preclinical PET/MRI Insertand Initial Results. IEEE TRANSACTIONS ON MEDICAL IMAGING, VOL. 34, NO. 11, NOVEMBER 2015

[3] https://reference.digilentinc.com/_media/sume:netfpga-sume_rm.pdf

[4] https://www.xilinx.com/support/documentation/ip_documentation/ten_gig_eth_pcs_pma/v6_0/pg068-ten-gig-eth-pcs-pma.pdf

[5] https://comblock.com/download/com5502soft.pdf



Generic Data Processing board development leveraging a modular approach based on SoM and SoCs

Simone Farina,
SEI Tagung 2019, FZJ Forschungszentrum Jülich, 10.04.2019

Outline

- MicroTCA Technology Lab Introduction
- ZYNQ Ultrascale+ MPSoC FMC+ carrier:
  - Board overview
  - Block diagram
  - Clock tree
  - Power section
  - MPSoC features and performance
  - PCB Characteristics
- MMC Stamp (Module Management Controller SoM)
- White Rabbit SoM support

TRANSFER MTCA TO RESEARCH AND INDUSTRY

- Custom developments
- High-end test & measurement services
- System configuration & integration
- LLRF design
- New Zone3 Classes & Revisions of the Standard

Ongoing Projects

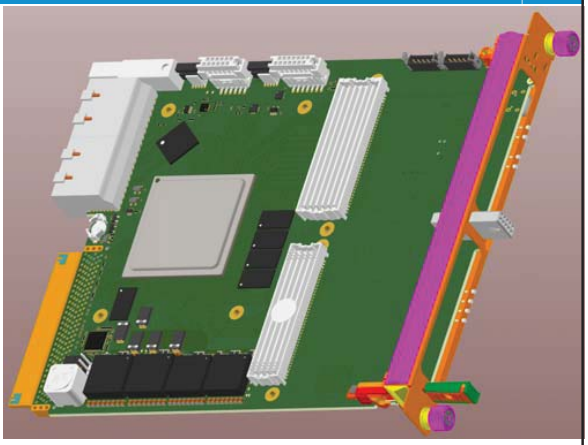
- LLRF developments
  - TARLA, NICA, ...
- System integration
  - Trioptics WaveScan - quality inspection system
  - configurator
- Custom developments
  - GigE Vision
  - FMC+ carrier with Zynq MPSoC
  - DFMC-DS800 board with new Zone 3 analog class
  - Board Support Package for TCK7
  - MMC System on a Module
- Measurement services
- Supporting activities

MTCA Technology Lab Team

- Dr. Holger Schlarb – Machine Beam Control Group Leader
- Michael Fenner – Head of Digital Electronics Development
- Dr. Thomas Walter – Head of MicroTCA Technology Lab
- Team

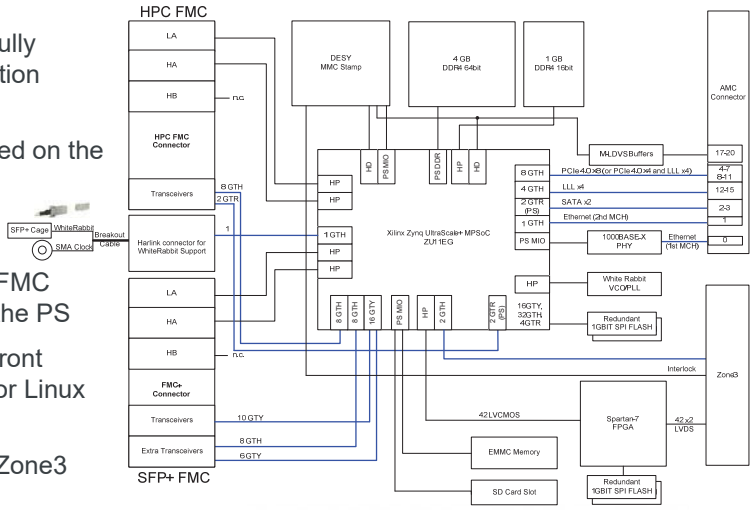
DAMC-FMC2ZUP Overview

- Double-width mid-size AMC board
- 1 FMC+ slot (VITA 57.4)
- 1 FMC HPC slot (VITA 57.1)
- ZU11EG Zynq Ultrascale+ MPSoC (650k logic cells, 2920 DSP)
- Works as “CPU module”: special FMC providing DisplayPort and USB host port.
- Front-panel clock input
- Zone 3 connector compliant to Class D1.1
- SoM MMC
- White Rabbit SoM endpoint



DAMC-FMC2ZUP Block Diagram

- Both FMC connectors are fully populated up to the HA section
- Full transceiver set populated on the FMC+ module
- 8 XCVR connected on the FMC HPC from the PL + 2 from the PS
- Embedded memories and front panel accessible SD card for Linux OS rootfs and user data
- FPGA based translator for Zone3 2.5V legacy support

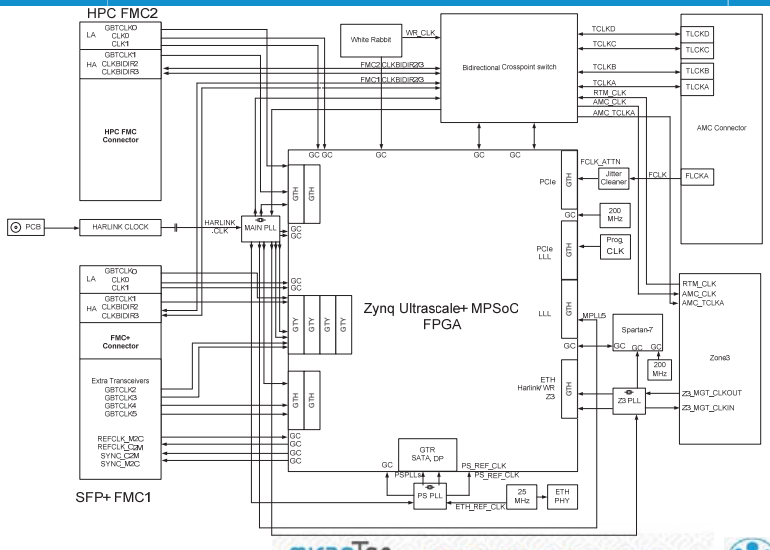


DAMC-FMC2ZUP Clock Tree Diagram

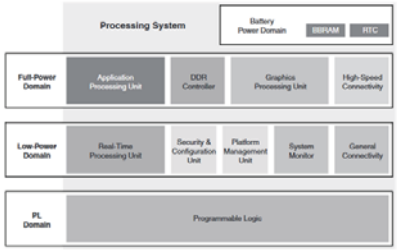
Clock Tree:

- A cross point switch collects/distributes clocks from backplane, mezzanine connectors and PLLs.
- Dedicated clock ICs for Ethernet and XCVR reference

Clock tree chain configured by MMC Stamp before PS boot sequence



DAMC-FMC2ZUP Power Stages section



To simplify the power section design:

- the 3 domains have been merged together
- a Power System Manager IC with PMBus compliant interface has been introduced
  - Additional benefits of PSM → Voltage trimming/margining and monitoring

Latest FPGA SoC families require quite complicated power distribution sections with full control over sequencing for power on/off.

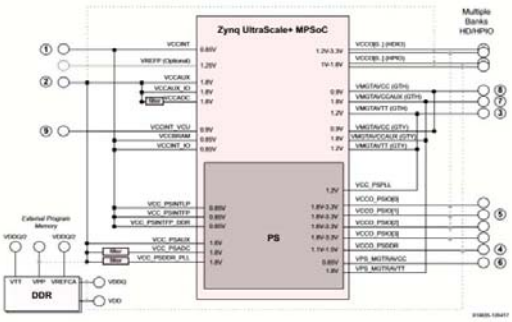
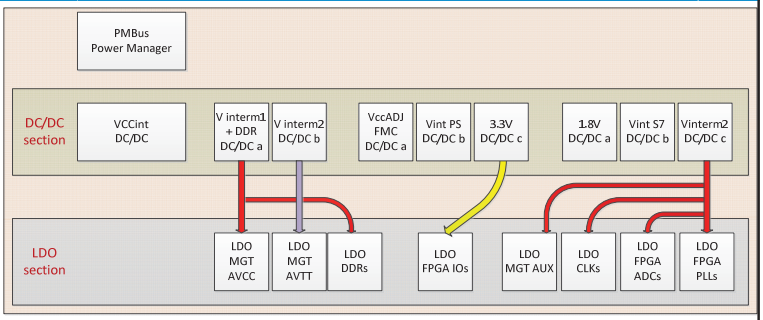


Figure 1-5: **Always On: Cost-Optimized Power Rail Consolidation**

DAMC-FMC2ZUP Power Stages section

Power system manager ensures that:

- All power section stages are enabled/disabled according recommended power-up/down sequences;
- Voltage rails are within specified range;

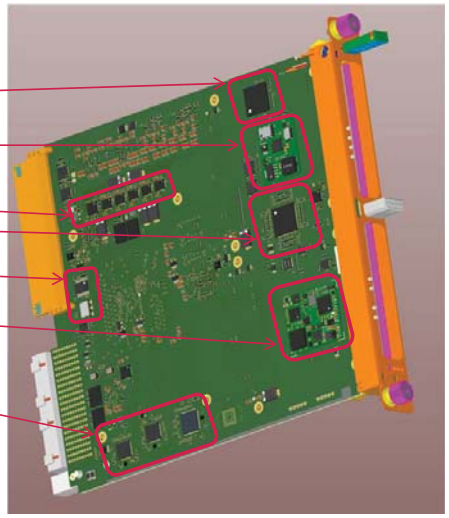


- Voltage trimming to minimize power dissipation in the LDO stages;
- Vadj for FMC modules is set to required value (supported values from 1.2V to 1.8V)

PMBus and the Power System Manager are controlled by the MMC

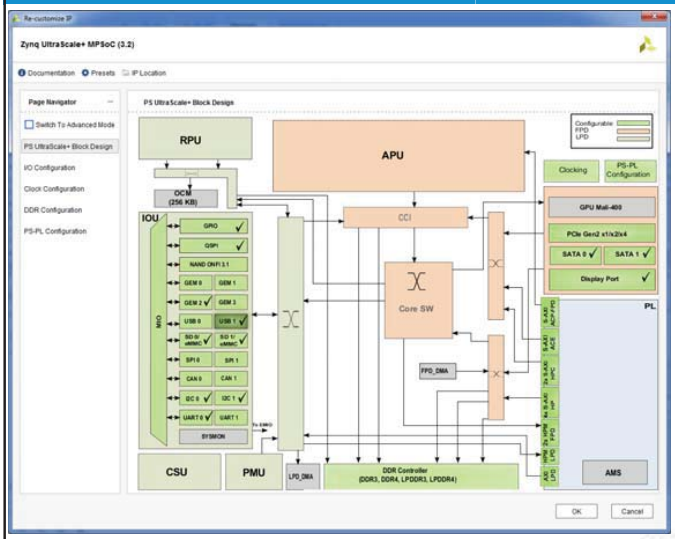
DAMC-FMC2ZUP Components

PMBus controller
White Rabbit SoM
LDOs
CLK Crosspoint Switch
Programmable CLK and CLK buffers
MMC Stamp SoM
PLL/Clock synthesizers



MicroTCA TECHNOLOGY LAB HELMHOLTZ RESEARCH FOR GRAND CHALLENGES DESY.

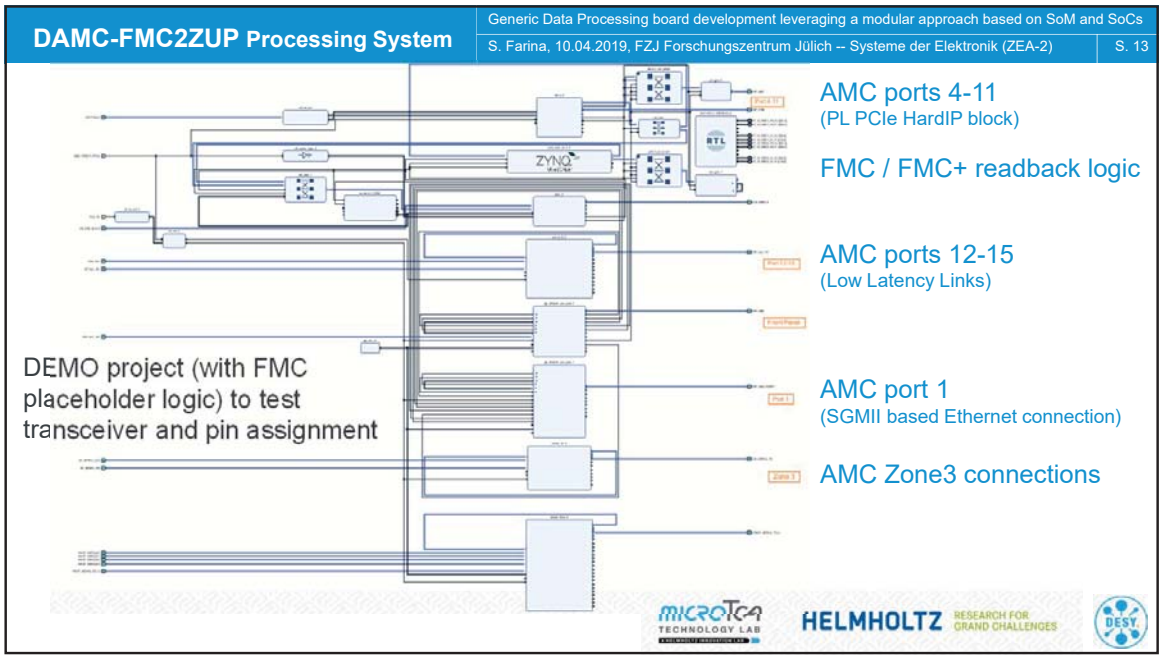
DAMC-FMC2ZUP Processing System

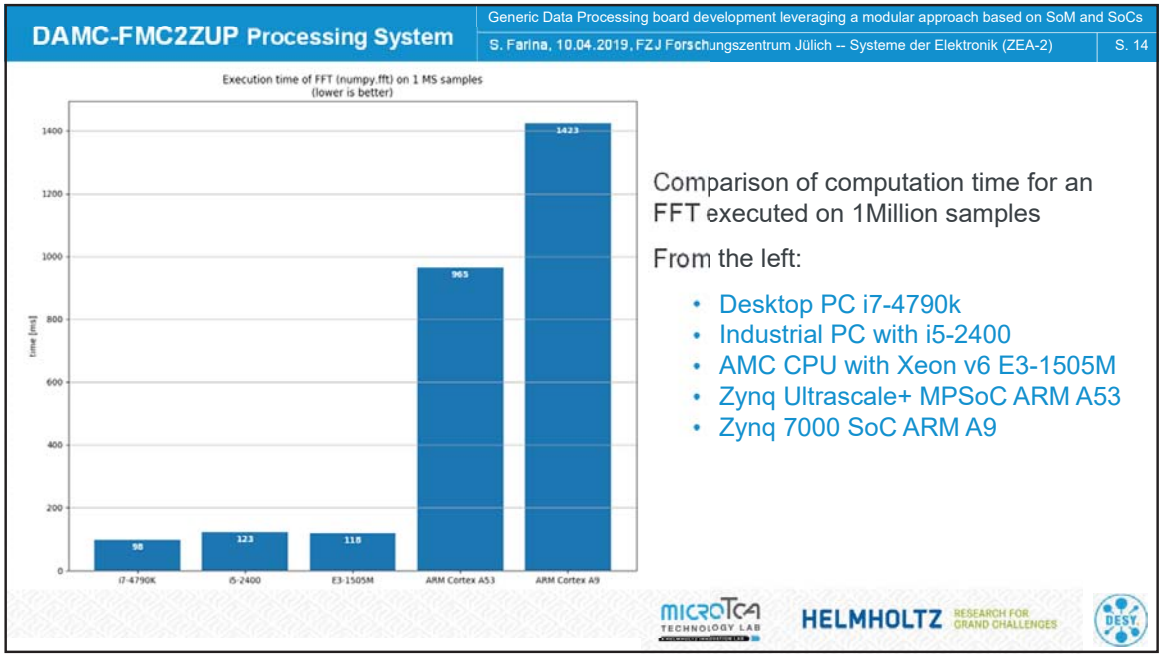


The PS section of the EG family of Zynq Ultrascale+ MPSoC comprises:

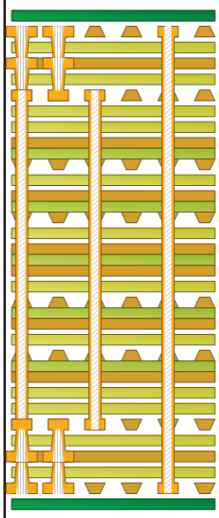
- Application Processing Unit with ARM® Cortex™-A53
- Real-Time Processing Unit with ARM® Cortex™-R5
- Graphics Processing Unit ARM Mali™-400
- High speed connectivity
  - SATA for ports 2 and 3
  - Display Port routed to FMC
- General connectivity (amongst which)
  - Storage SD card and eMMC
  - USB ULPI routed to FMC

MicroTCA TECHNOLOGY LAB HELMHOLTZ RESEARCH FOR GRAND CHALLENGES DESY.


DAMC-FMC2ZUP Processing System
Generic Data Processing board development leveraging a modular approach based on SoM and SoCs
S. Farina, 10.04.2019, FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2)
S. 13
AMC ports 4-11
(PL PCIe HardIP block)
FMC / FMC+ readback logic
AMC ports 12-15
(Low Latency Links)
DEMO project (with FMC placeholder logic) to test transceiver and pin assignment
AMC port 1
(SGMII based Ethernet connection)
AMC Zone3 connections
MicroTCA TECHNOLOGY LAB
HELMHOLTZ RESEARCH FOR GRAND CHALLENGES
DESY.


DAMC-FMC2ZUP Processing System
Generic Data Processing board development leveraging a modular approach based on SoM and SoCs
S. Farina, 10.04.2019, FZJ Forschungszentrum Jülich -- Systeme der Elektronik (ZEA-2)
S. 14
Execution time of FFT (numpy.fft) on 1 MS samples
(lower is better)
Time [ms]
0
200
400
600
800
1000
1200
1400
98
123
118
965
1423
i7-4790K
i5-2400
E3-1505M
ARM Cortex A53
ARM Cortex A9
Comparison of computation time for an FFT executed on 1Million samples
From the left:
Desktop PC i7-4790k
Industrial PC with i5-2400
AMC CPU with Xeon v6 E3-1505M
Zynq Ultrascale+ MPSoC ARM A53
Zynq 7000 SoC ARM A9
MicroTCA TECHNOLOGY LAB
HELMHOLTZ RESEARCH FOR GRAND CHALLENGES
DESY.

DAMC-FMC2ZUP PCB Specification



Polar Samples	SM/001	Liquid PhotoImageable Mask	SolderMask	25,000	4,000		
Polar Samples	FOI/002	Copper Foil	Copper	35,000		Signal	Ω
Panasonic	R-5670 Megtron6	PrePreg 1x1078	Dielectric	77,000	3,225		
Polar Samples	FOI/002	Copper Foil	Copper	35,000		Plane	
Panasonic	R-5670 Megtron6	PrePreg 1x1078	Dielectric	104,000	3,135		
Polar Samples	FOI/002	Copper Foil	Copper	35,000		Signal	Ω
Panasonic	R-5670 Megtron6	PrePreg 1x1078	Dielectric	77,000	3,225		
Panasonic	R-5670 Megtron6	PrePreg 1x1078	Dielectric	77,000	3,225		
				18,000		Plane	
Panasonic	R-5775 Megtron6	Core 1x1078	Dielectric	75,000	3,245		
				18,000		Signal	Ω
Panasonic	R-5670 Megtron6	PrePreg 1x1078	Dielectric	89,000	3,185		
				18,000		Plane	
Panasonic	R-5775 Megtron6	Core 1x1078	Dielectric	65,000	3,320		
				18,000		Signal	Ω
Panasonic	R-5670 Megtron6	PrePreg 1x1078	Dielectric	104,000	3,135		
				18,000		Plane	
Panasonic	R-5775 Megtron6	Core 1x1078	Dielectric	65,000	3,320		
				18,000		Plane	
Panasonic	R-5670 Megtron6	PrePreg 1x1078	Dielectric	104,000	3,135		
				18,000		Signal	Ω
Panasonic	R-5775 Megtron6	Core 1x1078	Dielectric	65,000	3,320		
				18,000		Plane	
Panasonic	R-5670 Megtron6	PrePreg 1x1078	Dielectric	89,000	3,185		
				18,000		Signal	Ω
Panasonic	R-5775 Megtron6	Core 1x1078	Dielectric	75,000	3,245		
				18,000		Plane	
Panasonic	R-5670 Megtron6	PrePreg 1x1078	Dielectric	77,000	3,225		
Panasonic	R-5670 Megtron6	PrePreg 1x1078	Dielectric	77,000	3,225		
Polar Samples	FOI/002	Copper Foil	Copper	35,000		Signal	Ω
Panasonic	R-5670 Megtron6	PrePreg 1x1078	Dielectric	104,000	3,135		
Polar Samples	FOI/002	Copper Foil	Copper	35,000		Plane	
Panasonic	R-5670 Megtron6	PrePreg 1x1078	Dielectric	77,000	3,225		
Polar Samples	FOI/002	Copper Foil	Copper	35,000		Signal	Ω
Polar Samples	SM/001	Liquid PhotoImageable Mask	SolderMask	25,000	4,000		

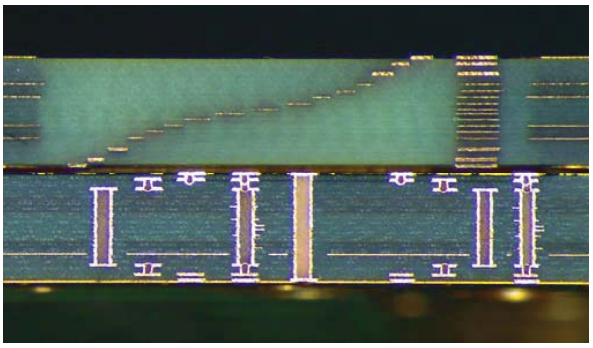
- 16-layer PCB with Blind, Buried and Stacked Vias.
- Via in pad for FPGAs and DDR modules
- 8 signal layers with controlled impedance:
  - 6 outer signal layers (40 and 50 Ω SE , 80 and 100 Ω DIFF)
  - 2 inner signal layers (50 Ω SE and 100 Ω DIFF)

MicroTCA TECHNOLOGY LAB HELMHOLTZ RESEARCH FOR GRAND CHALLENGES DESY.

DAMC-FMC2ZUP PCB Specification

- 16-layer PCB with Blind, Buried and Stacked Vias.

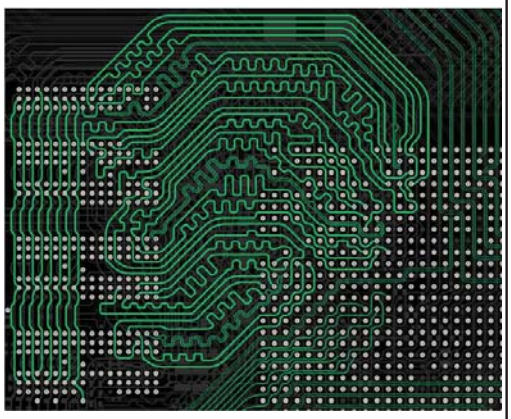
Similar layer stack implementation on technology demo board.



MicroTCA TECHNOLOGY LAB HELMHOLTZ RESEARCH FOR GRAND CHALLENGES DESY.

DAMC-ZUP DDR4 layout with write CRC

- 4GB DDR4 single-rank 64bit data bus (no ECC) to PS running at 2400MT/s
- 1GB DDR4 single-rank 16bit data bus to PL running at 2400 or 2133MT/s
- Support write CRC (~20% overhead)
- Additional restrictions for Write CRC:
  - Rule 1: Bits within a nibble must stay together.
  - Rule 2: Nibbles can be swapped within a byte.



DAMC-FMC2ZUP MMC SoM

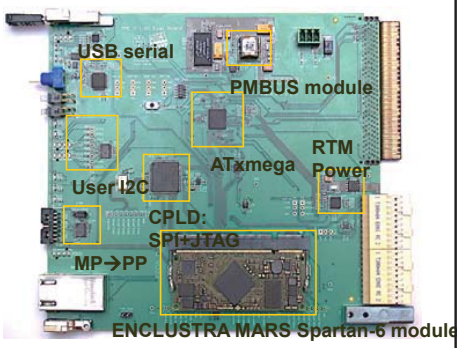
Why?

MTCA management is a challenging part of the development (very often underestimated)

- IPMI via micro controller is necessary
- Allows hot-swap, power control, status information, temperature alerts, etc.
- FPGA control including HPM update, JTAG selection

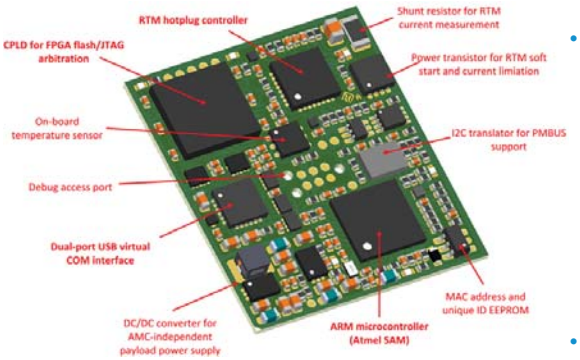
Different solutions are possible:

- Design for reuse with snippets:
  - still prone to mistakes (components spread across the PCB)
  - HW/SW modifications likely required for each AMC
- MMC SoM:
  - Fully integrated solution (only external temperature sensors needed)
  - Software package with all management functions



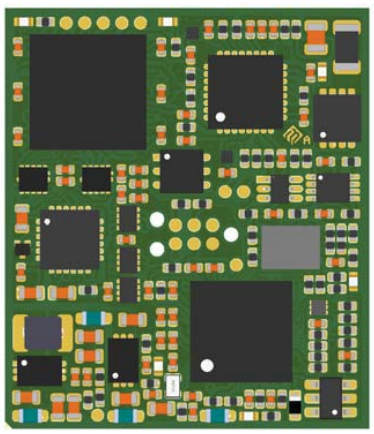
Design: Dariusz Makowski, DMCS

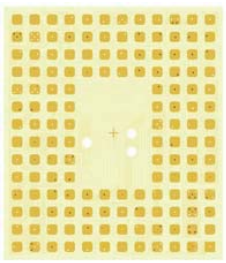
MMC Stamp SoM

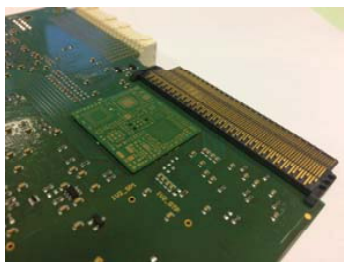


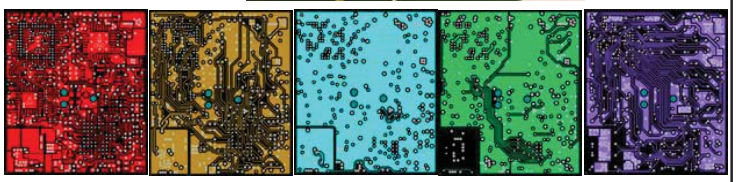
- MTCA management on a single board (SoM), ready-to-use, based on ARM Cortex-M4 (Atmel SAM)
- Developed together with DMCS Group (Dariusz Makowski, University of Technology Lodz)
  - Full IPMI handling (LEDs, Power, PMBUS)
  - Temperature sensors, Unique ID
  - FMC and RTM control (variable current, current readback)
  - Supports 2 FPGAs (JTAG, SPI flash, reset)
  - HPM firmware update: MMC, FPGA flashes
  - USB virtual COM port for MMC and FPGAs
  - JTAG arbitration (backplane/ JSM, Xilinx connector → FPGAs, RTM, FMC)
  - MCU debug access port
- Solder-on component.
- MMC firmware included

MMC Stamp SoM



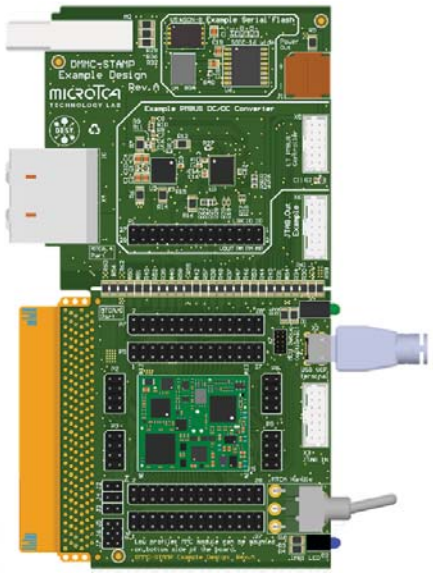






- 25x29mm + bottom-side mount: standard-compliant final height profile
- 6-Layer HDI Board (micro-vias, buried vias)

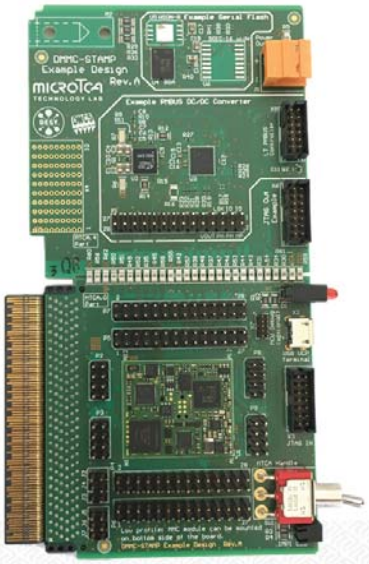
MMC Stamp Evaluation Board



- 1/3 AMC format, incl. Zone 3
- Adaptable to single-width format (MTCA.0)
- No components except handle and LEDs necessary
- basic RTM support (power, management)
- Full JTAG support
- Example PMBUS DC/DC converter
- Example serial flash (image for payload FPGA)
- USB serial terminal connector for debugging
- breakout section – pins for measurement

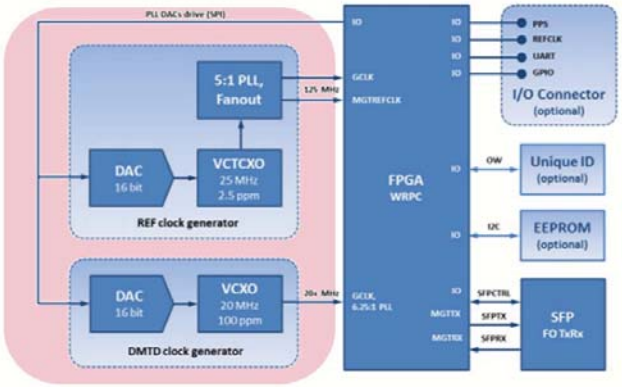
- First batch Q2/2019

MMC Stamp



White Rabbit SoM endpoint

- 125 MHz reference clock
- 62.5 MHz DDMTD clock
- system clock (≤ ref. clock)
- aux clocks



- bottom-side mount: standard-compliant final height profile

Vielen Dank für Ihre Aufmerksamkeit

Thank you for your attention

Karlsruhe Institute of Technology

Application of heterogeneous FPGA architectures in physics experiments

Oliver Sander

Attractivity of heterogeneous FPGAs

FPGAs are commonly used in a plethora of physics experiments

- Enable online processing (through parallelism in HW applications)
- Custom applications possible
- Ease of use (compared to ASICs)
- Huge variety of interfaces (especially to custom ASICs)

However, not everything works well on FPGAs

- Implementing control-flow driven tasks in hardware is tedious and much more efficient in software (e.g. slow control, transport protocols such as TCP/IP, calibration sequences, debug, test, …)
- FPGAs do not offer everything (e.g. floating point)

Why not have a hard IP core processor in an FPGA?

→ Heterogeneous FPGAs (monolithic integration of FPGA & CPU & …)

Ages of FPGA technology

Age of invention
- Xilinx XC2064, 64 FF 64 blocks, 128 LUT3
- Actel Antifuse (largest ~1990)
- No tools, manual P&R
- Multi FPGA Platforms

Age of accumulation
- Communication is main market
- Dedicated logic blocks (e.g. high-speed I/O, multiplier) → platform FPGAs
- Low cost FPGAs
- IP cores for large FPGAs

Age of acceleration
- Domain specific computing
- Specialized architectures
- Specialized computing environments
- …

1984 — 1992 — 2000 — 2008 — 2018

Age of expansion
- Rapidly growing FPGA sizes
- Increasing Demand for Design Automation
- SRAM FPGAs first for new technology – domination

Age of SoC
- Processor systems added
- Peripherals included
- Security functionality
- Platform management
- HLS

Ages are defined in a paper by Stephen Trimberger (2015) and in an interview with Ivo Bolsens (Xilinx CTO) in 2018

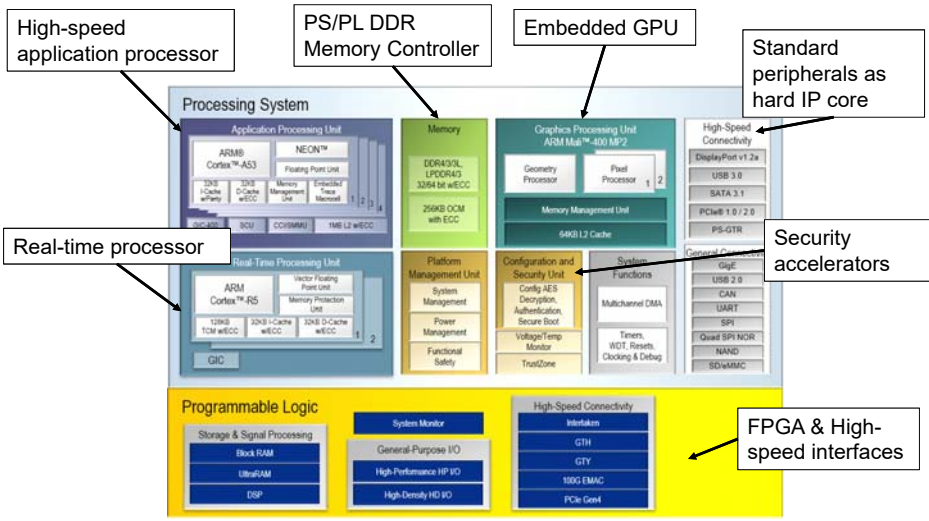
3 17.02.2020 SEI Workshop @ FZJ IPE - EPS

Which heterogeneous architectures do exist?

	Smart Fusion2	Arria 10 SX	Zynq	Stratix 10 SX	Zynq US+
Processors	ARM Cortex M3	2x ARM A9	2x ARM A9	4x ARM A53	4x ARM A53 2x ARM R5
Peripherals (I2C, SPI, ETH)	yes	yes	yes	yes	yes
Neon Extensions	-	yes	yes	yes	yes
Security Ext.	yes	yes	yes	yes	yes
FPGA complexity	146 k LE	660 k LE	444 k LC	2750 k LE	1100 k LC
GPU	-	-	-	-	Mali 400-MP2
High Speed IO	16x 3.2 Gb/s	48x 17.4 Gb/s	16x 16 Gb/s	64x 28.3 Gb/s 32x 17.4 Gb/s	28x 32.75 Gb/s 44x 16.3 Gb/s

4 17.02.2020 SEI Workshop @ FZJ IPE - EPS

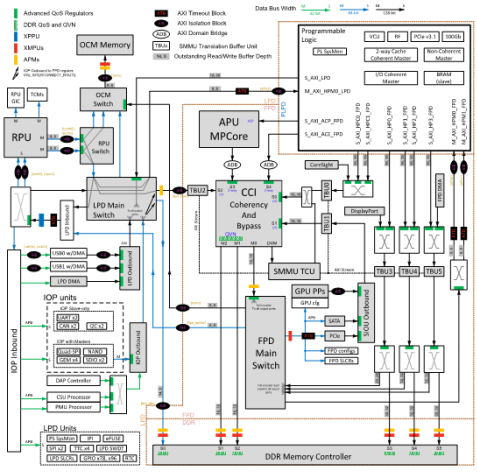
Programmable MPSoC – Zynq Ultrascale+



http://www.xilinx.com/products/silicon-devices/soc/index.htm

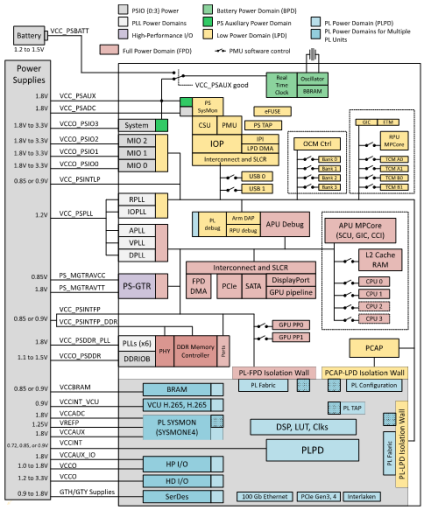
Zynq Ultrascale+ in more detail

Architecture

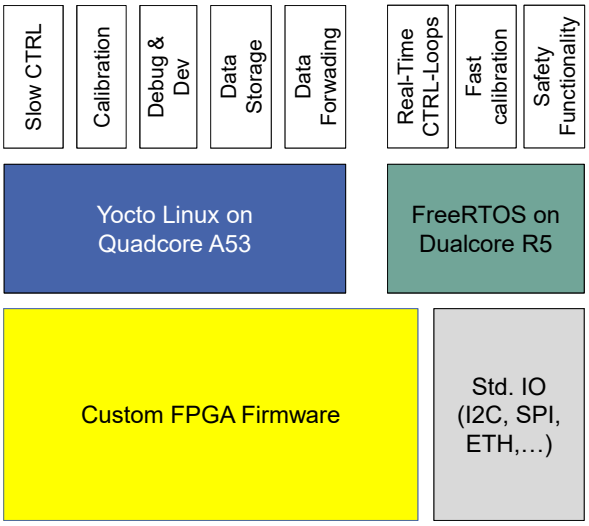


[Xilinx UG1085]

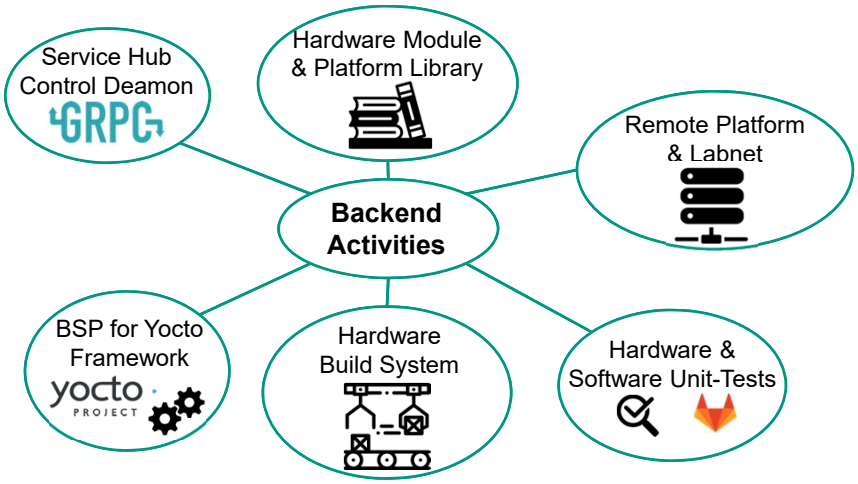
Power Domains



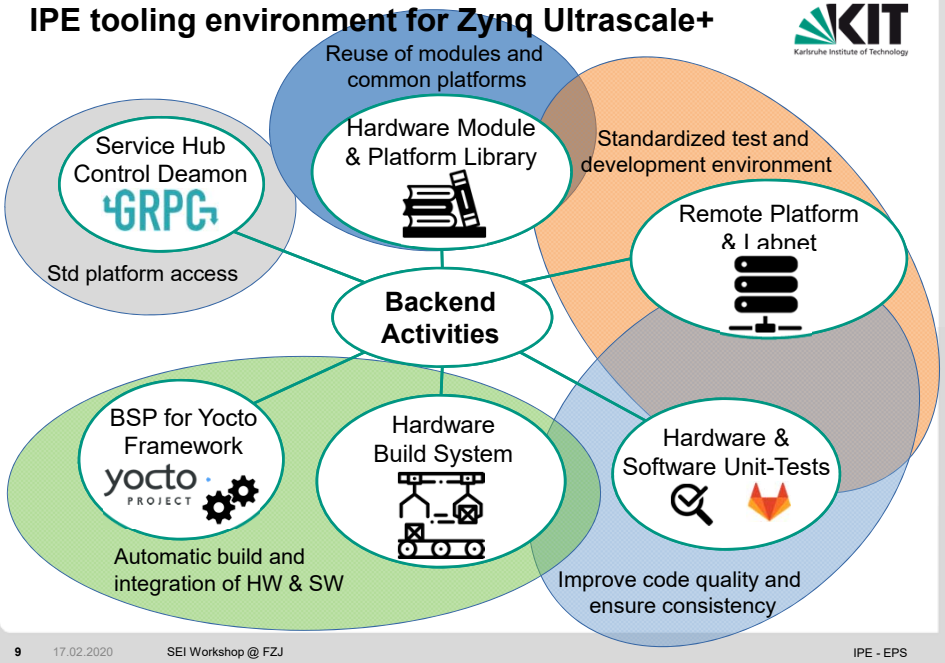
How could a software architecture look like?



IPE tooling environment for Zynq Ultrascale+



IPE tooling environment for Zynq Ultrascale+



Zynq US+ on multi purpose platform HiFlex 2

Photon science

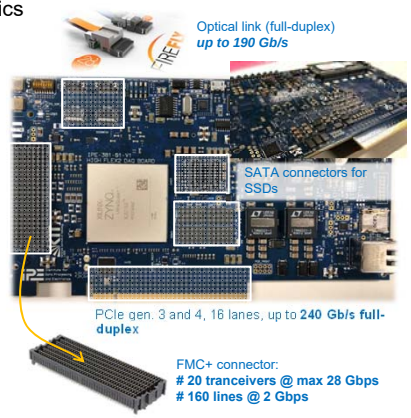
- New generation of detectors for beam diagnostics
- Diagnostics and stabilization of laser systems

Superconducting sensors and quantum technologies

- Readout of superconducting sensor arrays
- Control- and readout of qubits

High Energy Physics (HEP)

- NA62 (SPS-CERN) fast “low-level” trigger system, GPU-based
- High Level Trigger (HLT) based on GPU- FPGAs accelerators



Hardware platform for Artificial Intelligence algorithms

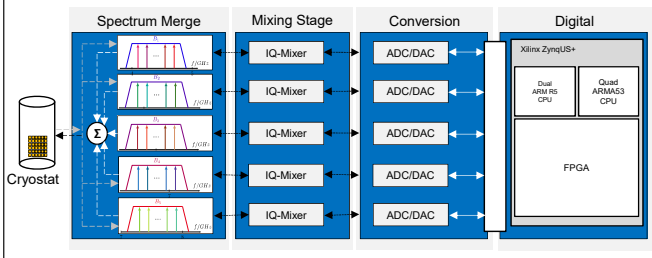
- Heterogeneous FPGA- GPU system based on Machine learning

Application 1 - DAQ for the ECHo experiment

The **E**lectron **C**apture ^{163}**Ho**lmium experiment **ECHo**[1] will measure the electron neutrino mass by analyzing the energy spectrum in the electron capture process of ^{163}Ho.

Technology 15x

- 800 superconducting sensors (MMC)
- 10 events per pixel per second
- 400 channels, one transmission line
- Frequency division multiplexing
- 4-8 GHz, one channel each 10 MHz



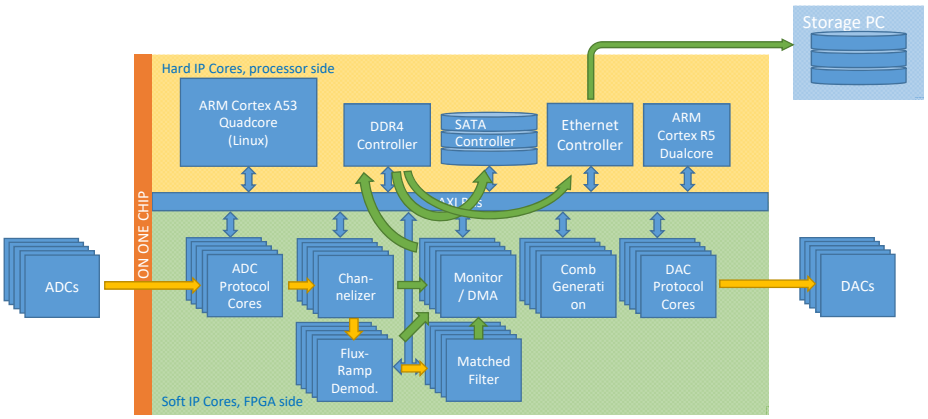
Software-defined Radio (SDR) system architecture

MPSoC / FPGA 15x

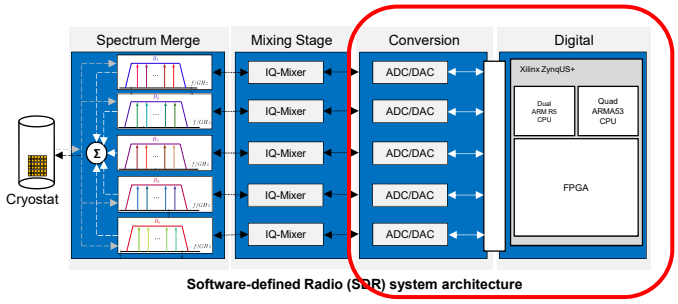
- 160 Gbps Input
- 160 Gbps Output
- < 10 Mb/s to back-end storage server
- Full event processing on FPGA required
- Complex Calibration on processors with FPGA support

Application 1 - DAQ for the ECHo experiment

Coarse architecture overview including firmware blocks



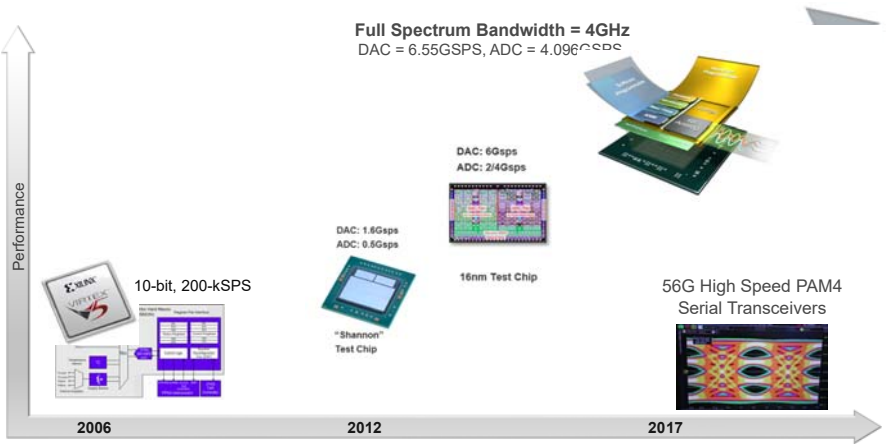
Once more: DAQ for the ECHo experiment



Software-defined Radio (SDR) system architecture

Why not integrate the ADCs/DACs into a heterogeneous MPSoC platform?

Integrating ADC/DAC into FPGAs @ Xilinx



[Xilinx, Glenn Steiner, XDF Talk @ Frankfurt, RF Solutions with Zynq ® UltraScale+TM RFSoC]

Zynq Ultrascale+ becomes more heterogeneous

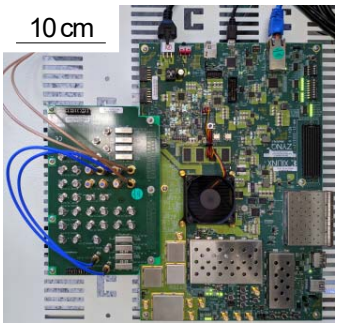
- Xilinx integrated high-performance ADC/DACs → **RFSoC**

		Baseband	Wireless Radio		Backhaul, Remote-PHY	Phased Array Radar / Radio
		ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR
RF Data Converters Soft-decision FEC	12-bit, 4GSPS ADC	–	8	8	8	–
	12-bit, 2GSPS ADC	–	–	–	–	16
	14-bit, 6.4GSPS DAC	–	8	8	8	16
	SD-FEC	8	–	–	8	–
Processing System & Programmable Logic	Application Processor Core	Quad-core ARM Cortex-A53 MPCore up to 1.5GHz				
	Real-Time Processor Core	Dual-core ARM Cortex-R5 MPCore up to 533MHz				
	High Speed Connectivity	DDR4-2600, PCIe Gen3 x16, 100G Ethernet				
	Logic Density (System Logic Cells)	930K	678K	930K	930K	930K
	DSP Slices	4,272	3,145	4,272	4,272	4,272
	33G Transceivers	16	8	16	16	16

[Xilinx, Glenn Steiner, XDF Talk @ Frankfurt, RF Solutions with Zynq ® UltraScale+TM RFSoC]

Gen 1		Gen2		Gen3		
ADC	DAC	ADC	DAC	ADC	DAC	
4.096	6.554	2.275	6.554	5.0	10.0	GSPS

Application 2 - RFSoC for Quantum Computing



Xilinx Zynq UltraScale+ RFSoC ZCU111

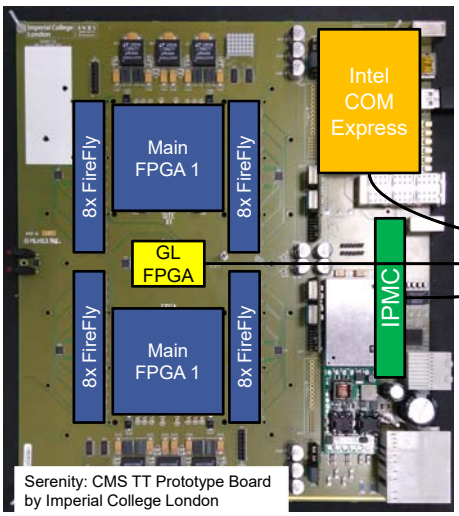
- FPGA + 2 Processors
- Integrated ADC/DAC

Features of Custom Firmware

- 428 ns feedback latency
- Complete experiment flows possible on the platform (pulse sequencing, data collection, averaging, statistics/evaluation...)
- Python drivers & Qkit[1] integration

[1] https://github.com/qkitgroup/qkit

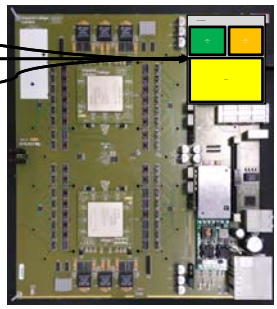
Application 3: Integrated IPMC for HL-LHC CMS L1 Track Trigger



Serenity: CMS TT Prototype Board by Imperial College London

- Intel Atom: High Performance interface to main FPGAs for dev, test, and calibration
- IPMC: Low-level platform management
- GL FPGA: interface conversion, glue logic

Integration into single Zynq US+



Next generation FPGA: Xilinx Versal

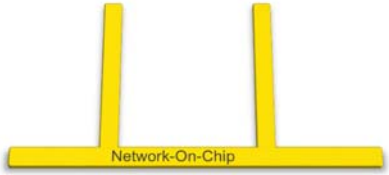
It is Xilinx' newest architecture

- More heterogeneous
- More complex

} Adaptive compute acceleration platform (ACAP)

Key Features

- FPGAs + Processors + AI Engines
- Network on Chip backbone
  - High bandwidth & low latency
  - Guaranteed QoS
  - Memory mapped
  - built in arbitration
- Complex memory hierarchy (LUTRAM, BRAM, UltraRAM, Accelerator RAM, HBM, DDR)
- + optimizations in FPGA components



[XDF Frankfurt]

Versal - AI tile architecture

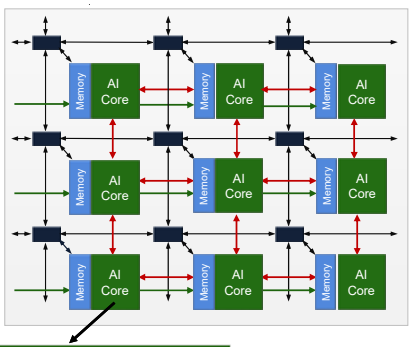
1.3 GHz VLIW / SIMD vector processors

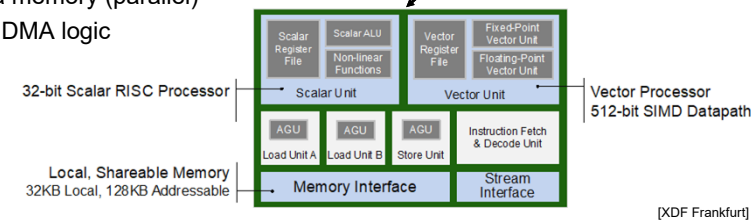
Parallelity

- VLIW: 7+ operations / clock cycle
- SIMD: 512 bit vector datapath (8 / 16 / 32 bit & SPFP operands)
- Up to 128 INT8 MACs / clock cycle / core

Memory

- 16 KB Internal program memory
- 32 KB data memory (parallel)
- Integrated DMA logic

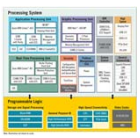




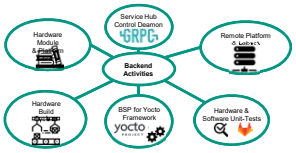
[XDF Frankfurt]

Conclusion

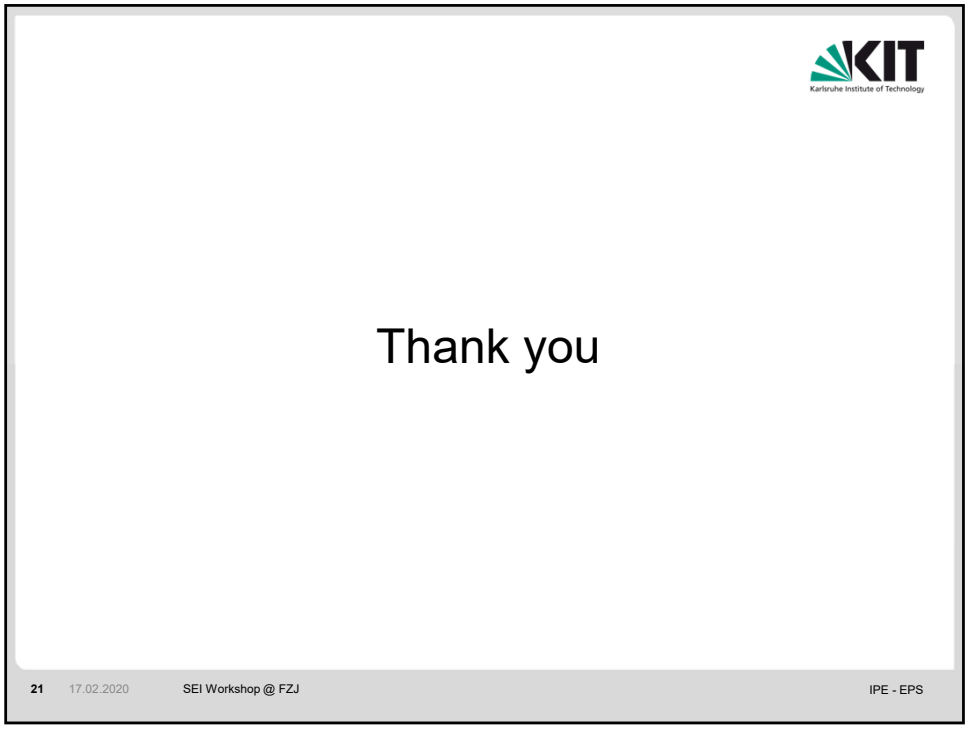
- FPGAs become more and **more heterogeneous** devices
  - Zynq US+: FPGA & **CPU & Peripherals**
  - RFSoC: Zynq US+ & **ADC & DAC**
  - ACAP: FPGA & CPU & Per. & **VLIW/SIMD**



- Enables **high functional integration** (including control, calibration, and test software)



- Giant leaps in **tooling required** to leverage potential
- KIT IPE strongly believes in benefits of heterogeneous architectures → baseline for various projects


Thank you
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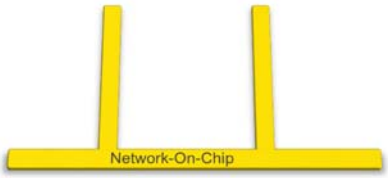
Next generation FPGA: Xilinx Versal

It is Xilinx‘ newest architecture

- More heterogeneous
- More complex

} Adaptive compute acceleration platform (ACAP)



Key Features

- FPGAs + Processors + AI Engines
- Network on Chip backbone
  - High bandwidth & low latency
  - Guaranteed QoS
  - Memory mapped
  - built in arbitration
- Complex memory hierarchy (LUTRAM, BRAM, UltraRAM, Accelerator RAM, HBM, DDR)
- + optimizations in FPGA components

System Logic Cells (K)	540–1,968	352–2,154
Hierarchical Memory (Mb)	68–191	40–324
DSP Engines	928–1,968	472–3,984
AI Engines	128–400	–
Processing System	✓	✓
Serial Transceivers (NRZ, PAM4)	8–44	12–66
Max. Serial Bandwidth (full duplex) (Tb/s)	2.9	4.2
I/O	346–692	238–778
Memory Controllers	2–4	1–6

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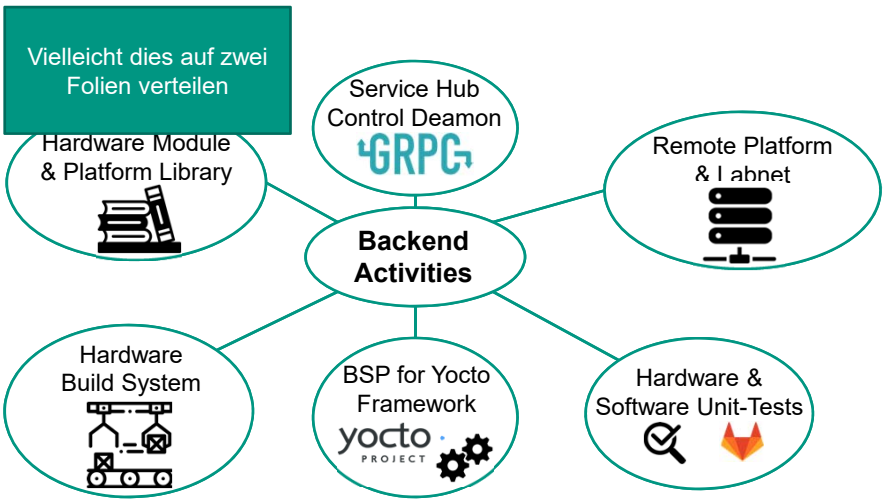
IPE tooling environment for Zynq Ultrascale+

Vielleicht dies auf zwei Folien verteilen



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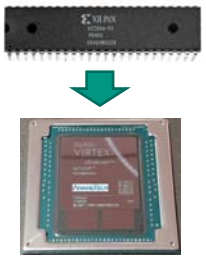
Overview

- Part 1 -
FPGAs
History and Status



- Part 2 -
MPSoC and selected application examples

- Part 3 -
Next generation architecture

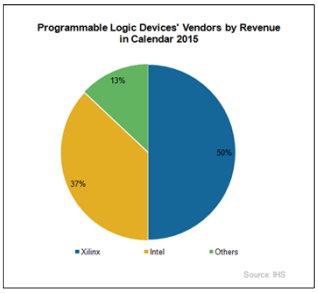
Comments/Disclaimer
(1) Talk content is biased towards Xilinx FPGAs. This is neither a statement nor a recommendation.
(2) Talk focuses on high-end architectures to show technical development.
(3) Content is a personal selection and not exhaustive.
(4) Versal Information comes from XDF Frankfurt (links need to be added)

FPGA market or which vendors did survive?

achronix SEMICONDUCTOR CORPORATION
FPGA IP core for SoC designs

intel FPGA
SRAM based FPGAs Broad range

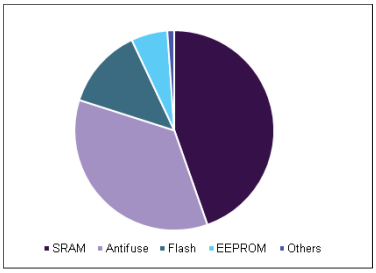
LATTICE SEMICONDUCTOR
Low power & cost efficient FPGAs

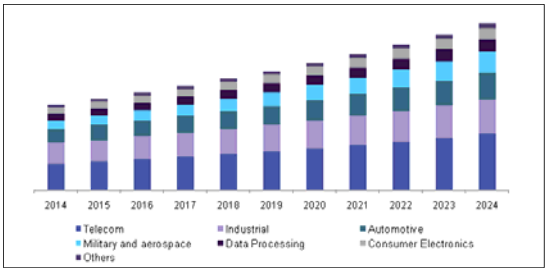


MICROCHIP
2 small SRAM FPGA families

Microsemi
Flash & Antifuse FPGAs

XILINX ALL PROGRAMMABLE
SRAM based FPGAs Broad range



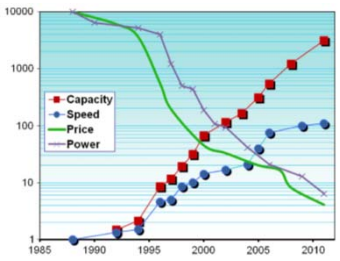


What about Intel vs. Xilinx?

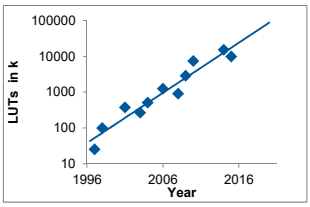
FPGAs for cost sensitive or mid-range products	• focus on logic/money • limited IO bandwidth
High performance FPGAs	• maximum LUTs • maximum DSP slices • maximum internal memory • maximum IO bandwidth (30 Gbps, 58 Gbps)
FPGA + HBM	• derived from HP FPGAs • integration of large memories (GB)
FPGA + Processor System	• derived from HP FPGAs • multiple processors • memory and caches • peripherals
FPGA+Processor+ ADC/DAC	• derived from previous • high performance ADC/DAC

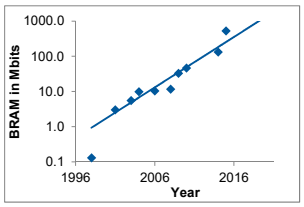
FPGA complexity over the years in numbers

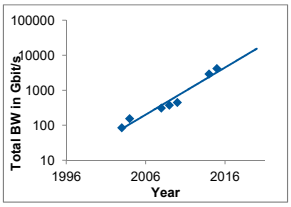
- Limited feature requirements (transistors, wires) of SRAM FPGAs allowed early adoption of new technology nodes
  → front-runner
- Exponential progress in compute power, memory, and bandwidth
- Dramatic increase in power efficiency
- Dramatic decrease of price per logic gate



(S. Trimberger, DOI 10.1109/JPROC.2015.2392104)







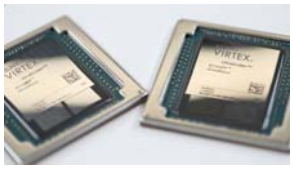
(Dissertation C. Amstutz, 2016)

Features in modern FPGA architectures

	Kintex UltraScale FPGA	Kintex UltraScale+ FPGA	Virtex UltraScale FPGA	Virtex UltraScale+ FPGA	Zynq UltraScale+ MPSoC	Zynq UltraScale+ RFSoC
MPSoC Processing System					✓	✓
RF-ADC/DAC						✓
SD-FEC						✓
System Logic Cells (K)	318–1,451	356–1,143	783–5,541	862–3,780	103–1,143	678–930
Block Memory (Mb)	12.7–75.9	12.7–34.6	44.3–132.9	23.6–94.5	4.5–34.6	27.8–38.0
UltraRAM (Mb)		0–36		90–360	0–36	13.5–22.5
HBM DRAM (GB)				0–8		
DSP (Slices)	768–5,520	1,368–3,528	600–2,880	2,280–12,288	240–3,528	3,145–4,272
DSP Performance (GMAC/s)	8,180	6,287	4,268	21,897	6,287	7,613
Transceivers	12–64	16–76	36–120	32–128	0–72	8–16
Max. Transceiver Speed (Gb/s)	16.3	32.75	30.5	58.0	32.75	32.75
Max. Serial Bandwidth (full duplex) (Gb/s)	2,086	3,268	5,616	8,384	3,268	1,048
Memory Interface Performance (Mb/s)	2,400	2,666	2,400	2,666	2,666	2,666
I/O Pins	312–832	280–668	338–1,456	208–832	82–668	280–408

New Features in Virtex Ultrascale+ (16 nm FinFET+)

- Ultra RAM Memory blocks (4kx72)
- Up to 8 GB HBM integrated DRAM (460 GB/s)
- 58 Gb/s PAM4 transceivers, 32 Gb/s
- PCI GEN3 (6x) and GEN4 (4x)
- 100G ethernet MAC with KR4-FEC & 150 G Interlaken cores



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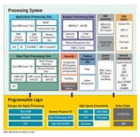
- Part 2 - MPSoC and application examples



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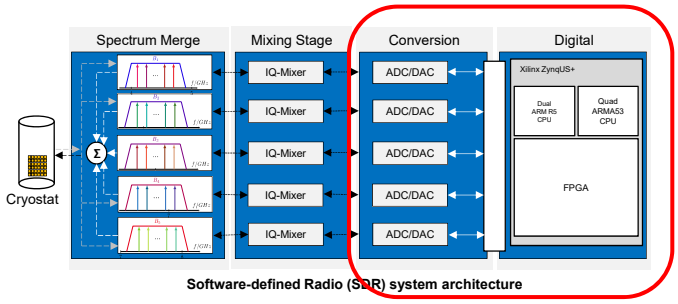
Once more: DAQ for the ECHo experiment



Software-defined Radio (SDR) system architecture

Why not integrate the ADCs/DACs into a heterogeneous MPSoC platform?

- Part 3 -
Next generation FPGA(?) architecture

XILINX VERSAL™

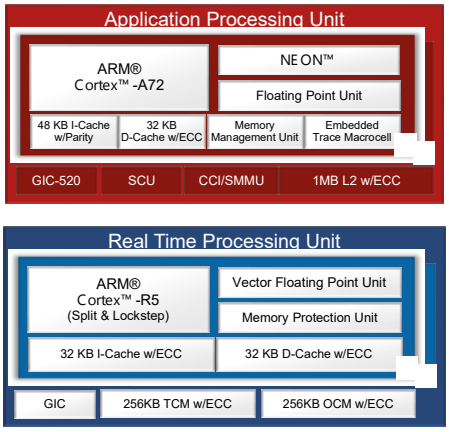
Versal – Scalar Units

Dual-Core ARM Cortex-A72 application processors

- Arm-v8A architecture
- Up to 1.7 GHz
- 2x single-threaded performance (DMIPS Versal vs. Zynq US+)

Dual-Core ARM Cortex-R5 realt-time processors

- Arm-v7R architecture
- Up to 750 MHz
- Low latency and deterministic
- Supports lock-step
- Internal memory



Peripherals

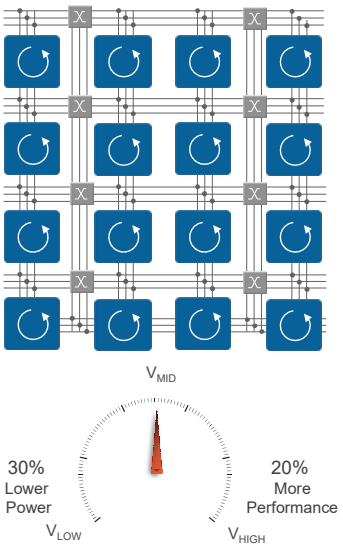
- Ethernet, SPI, I2C, CAN, UART, GPIO, USB, timer-counter, watchdog

Versal – Adaptable Engines

For traditionalists: This is the FPGA part

Some known facts

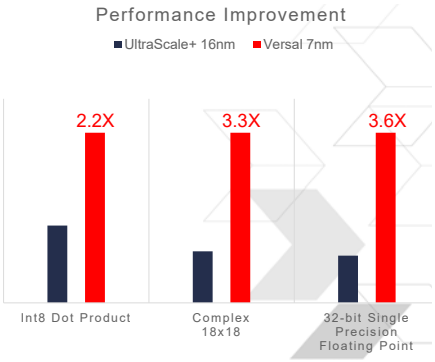
- 6 Input LUTs
- **Each CLB has 32 LUTs and 64 FF (4x density compared to US+)**
- 16 LUTs in a slice can be
  - a 64 bit RAM
  - 32-bit shift registers (SRL32) or two SRL16
- **Internal connection of LUTs possible**
- 4x clock, 4x set/reset, 16 clock enable
- **3 step voltage-scaling supported**



Versal - DSP blocks

New key features

- More than 1 GHz of performance
- Integrated FP32, FP16 floating point
- Integrated complex 18x18 operations
- SIMD support for add/sub/acc (dual 24 bit, quad 12 bit)



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P. Kaever, P.Göttlicher

Arbeitstreffen: Testen

Es wurden die verschiedenen Phasen der Projekte angesprochen.

1. Hardware:

- **Testen während der Entwicklung**. Hier geht es meist mit dedizierten Messaufbauten darum, die Ideen des Designs und deren Umsetzung zu validieren.
    - Es werden didizierte Messgeräte benötigt
    - Es wird Software benötige
    - Es wird Firmware für FPGAs genötigt

  Vielfach ergeben sich in den Instituten oder Gruppen dortige Standard-Instrumente und Softwarepakete

- **Tests der Produktion.**
  Es wurden Standardisierte Testmethoden angesprochen:
    - Flying Probes für Impedanzen aller Netze
    - JTAG basiertes Boundary Scan
    - Optische Kontrollen
    - EMV
    - Kontinuierliche Qualitätssicheruntg der Werkzeuge, e.g. Löten
    -
- **Funktionale Tests** in den entwickelnden gruppen oder zentralen Gruppen in Zusammenarbeit mit den Entwicklern. Hier gelten ähnlich Überlegungen wie zu den Tests während der Entwicklung, allerdings mit einem weiteren Schritt zu einfacher routinierter Bedienung.

2. Software/Firmware

Längere Gespräche ergaben sich zum Test von Software.

Konzept Softwarereview und -test:

Reviewer sind Projektmitarbeiter mit Softwarekenntnissen

- Review- und Testsituation:
- Zu testende Systeme: häufig SPS-Software
- Testcases werden mit Python-Skripten geschrieben
- Falls möglich wird mit Hardware in the Loop getestet - z.B. bei häufig verwendeten Systemen

Tooling im Projekt:

- Redmine für Versionsverwaltung und als Ticketsystem
- Gerith als Review-System
- Jenkins als Buildsystem und für Test Runs

Angestrebt wird eine testgetriebene Entwicklung

- Definition der Testcases
- Codierung der Unit-Tests
- Einbindung in Jenkins
- Codierung der Funktionalität
- Programmierung gegen die Testcases und sukzessive Iteration von Codierung und Test

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